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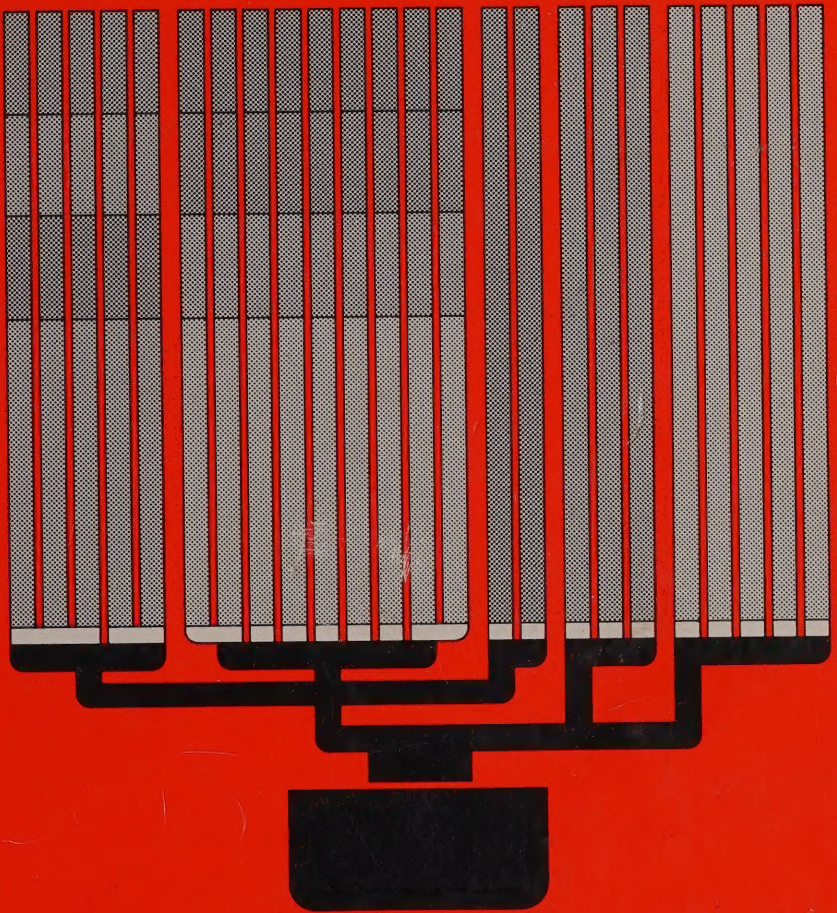
TTL DATA BOOK



MADE IN FAIRCHILD

JUNE 1972

Fairchild Semiconductor TTL Data Book Contents And Section Selector

If you know the correct 5400, 7400, 9300 or 9600 device type number, find the correct page in the Numerical Index.

If you are trying to choose the best device for your application, consult the Selector guides.

If you need the package dimensions for a specific device, see Packaging Information.

If you need the exact, or nearest Fairchild equivalent to another manufacturer's device, consult the Cross Reference Guide.

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The
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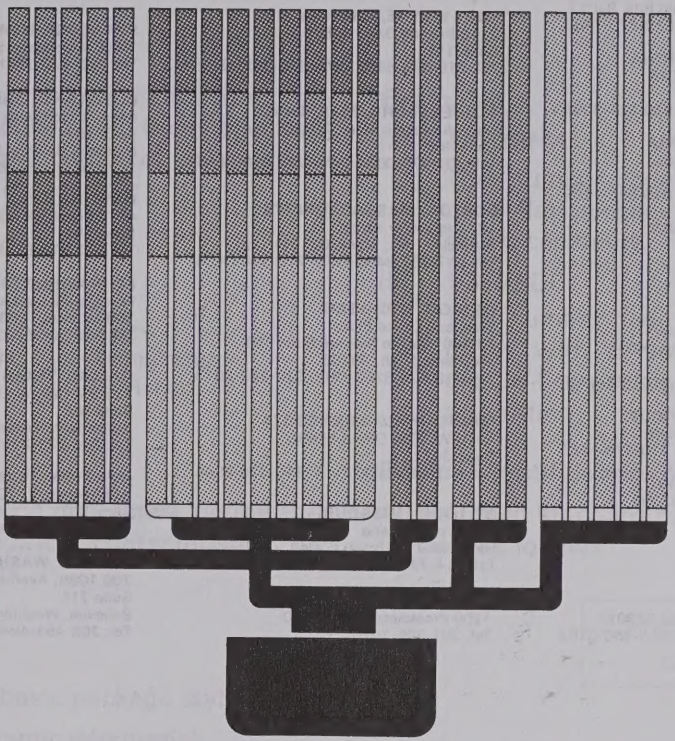
TTL Data Book



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Fairchild's TTL Family is the most complete line of TTL products available today. There are over 250 circuit functions with more than 100 MSI devices from which to choose. The family consists of logic, memory and interface functions, and is a unique blend of Fairchild proprietary circuits and a large number of second source devices which have achieved wide market acceptance.

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9H00	High Speed SSI
9L00	Low Power SSI
9N00	Standard SSI
9S00	Schottky SSI
9300	Standard MSI
93L00	Low Power MSI
93S00	Schottky MSI
9600	Monostable SSI
93400	Memory Elements

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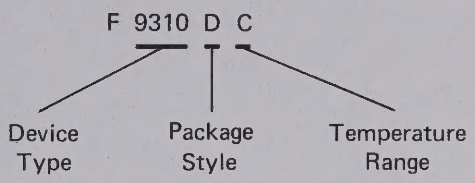
ORDER INFORMATION

A simplified ordering procedure for Fairchild digital integrated circuits is introduced with the publication of this catalog. Three basic units of information are contained in the new order code:



Device Type

Four to seven alpha numeric characters define the device functional and electrical characteristics, as specified in the data sheets.

Package Style

One letter represents the basic package style.

D = Dual In-Line Ceramic (Hermetic)
E = Plastic Can
F = Flat Package (Hermetic)
H = Metal Can
P = Dual In-Line Plastic

Different outlines exist within each package style to accomodate the various die sizes and numbers of leads. Specific dimensions for each package can be found in the "Packaging Information" section.

Temperature Range

Two Basic temperature grades are in common use:

C = Commercial-Industrial, 0°C to +70°C (or 75°C)
M = Military, –55°C to +125°C

Exact values and conditions are indicated on the data sheets.

Examples

(a) 93L28FM

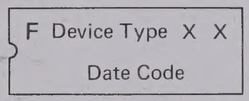
This number code indicates a 93L28 register in a flat package with military temperature rating capability.

(b) 9317BDC

This number code indicates a 9317 decoder/driver with B voltage option in a ceramic dual in-line package with commercial temperature rating.

Device Identification/Marking

All Fairchild standard catalog digital circuits will be marked as follows:



When more than one number is in common use for a device, slash marking with both numbers may be used. Example: 74H04/9H04.

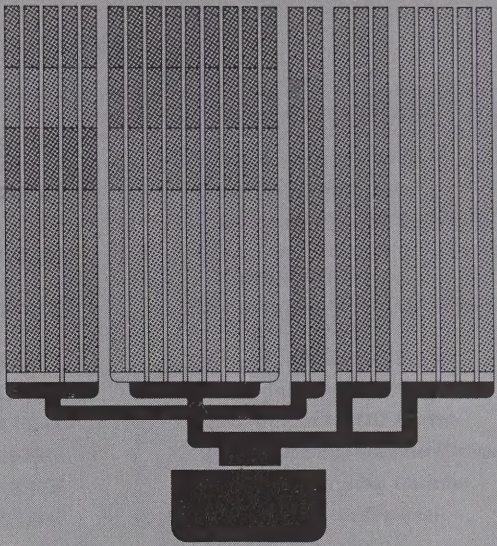
Mil Spec 38510 Processing

Additional processing to Fairchild Unique 38510 specifications is indicated by noting the appropriate requirements after the standard order code.

Detailed ordering procedures are provided in the OEM price list.

Old Order Codes

Devices may continue to be purchased against old order codes (Example: U7B931059X). However, all products will be marked with new order codes unless otherwise specified.



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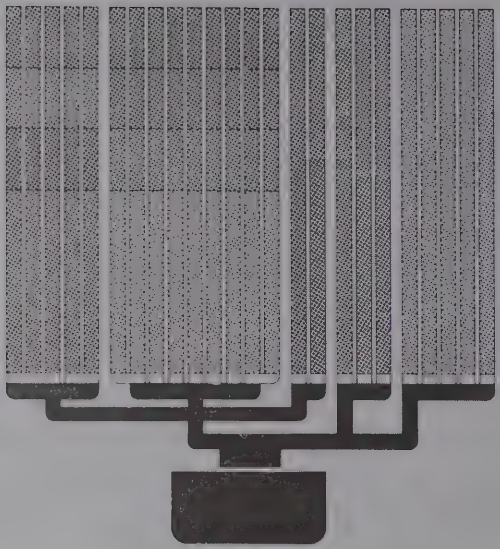

Selector Guide and Functional Index

The following selector guides provide a comparison of the key parameters for all Fairchild TTL devices. They should be used to help determine the most suitable device for a specific application. Final selection should be made using the appropriate data sheet.

Charts are provided covering the following device categories.

SSI

Gates, Buffers and Inverters
Flip-Flops
Monostables
Interface-Drivers
Interface-Receivers
Interface-Level Translators

MSI/MEMORIES

Arithmetic Operators
  —Adders, ALU.S, Comparators,
Multipliers, Parity Checkers.
Counters
Decoders-Display
Decoders/Demultiplexers
Encoders
Latches
Memories [RAM (Read/Write),
                ROM, Associative]
Multiplexers
Registers

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4
5
6
7
8
9
10
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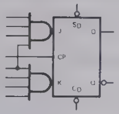
12

SINGLE FLIP-FLOP SELECTOR GUIDE

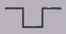
OUTPUT CHANGES ON POSITIVE GOING EDGE

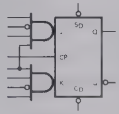
OUTPUT CHANGES ON NEGATIVE GOING EDGE

MASTER/SLAVE

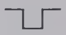


9000/74104
20 MHz/16 ns

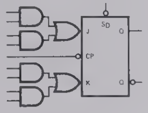


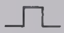


9001/74105
50 MHz/16 ns

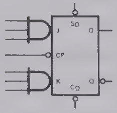


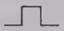
9H71/74H71
30 MHz/22 ns



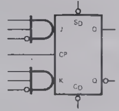


9N72/7472
20 MHz/25 ns
9H72/74H72
30 MHz/22 ns

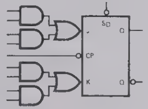




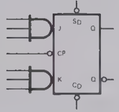
EDGE TRIGGERED



9N70/7470
35 MHz/27 ns



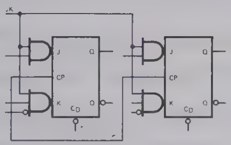
9H101/74H101
50 MHz/16 ns



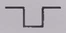
9H102/74H102
50 MHz/16 ns

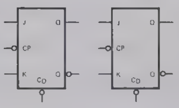
DUAL FLIP-FLOP SELECTOR GUIDE

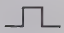
MASTER/SLAVE



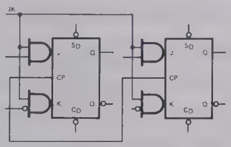
9020
50 MHz/16 ns



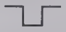


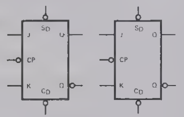


9N73/7473 • 9N107/74107
20 MHz/25 ns
9H73/74H73
30 MHz/22 ns

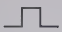


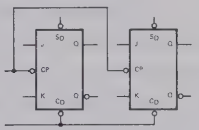
9022
50 MHz/16 ns



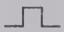


9N76/7476
20 MHz/25 ns
9H76/74H76
30 MHz/22 ns

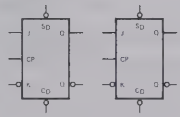




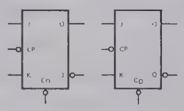
9H78/74H78
30 MHz/22 ns



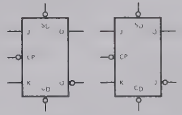
EDGE TRIGGERED



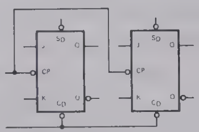
9024
25 MHz/22 ns
9L24
8 MHz/66 ns
9S109
100 MHz/7 ns



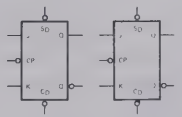
9H103/74H103
50 MHz/16 ns



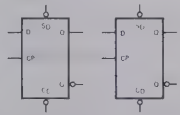
9H106/74H106
50 MHz/16 ns



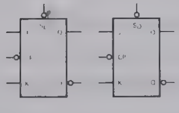
9H108/74H108
50MHz/16 ns



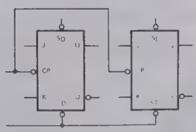
9S112/74S112
125 MHz/5 ns



9N74/7474
25 MHz/20 ns
9H74/74H74
43 MHz/13 ns
9S74/74S74
100 MHz/7 ns



9S113/74S113
125 MHz/5 ns



9S114/74S114
125 MHz/5 ns

MASTER/SLAVE (or "ONES CATCHING" MASTER/SLAVE)—The master is sensitive to input conditions during the active portion of the clock pulse.
EDGE TRIGGERED — Only sensitive to input conditions immediately prior to active clock edge.

SSI • GATES, BUFFERS AND INVERTERS

	LOW POWER	STANDARD	
	t_{pd} = 20 ns P_d = 2 mW per Gate	t_{pd} = 10 ns P_d = 10 mW per Gate	
NAND GATES	0°C to +70°C and −55° to +125°C	0° to +70°C	−55° to +125°C
Quad 2-Input Positive NAND Gate	9L00	9N00/7400	9N00/5400
Quad 2-Input Positive NAND Gate with Open-Collector Output		9N01/7401	9N01/5401
		9N03/7403	9N03/5403
Quad 2-Input Positive NAND Gate (15 Volts)		9N26/7426	9N26/5426
Triple 3-Input Positive NAND Gate		9N10/7410	9N10/5410
Triple 3-Input Positive NAND (Open Collector)		9N12/7412	9N12/5412
Dual 4-Input Positive NAND Gate		9N20/7420	9N20/5420
8-Input Positive NAND Gate		9N30/7430	9N30/5430
NOR GATES			
Quad 2-Input Positive NOR Gate		9N02/7402	9N02/5402
Quad 2-2-2-4-Input Positive NOR Gate			
Triple 3-Input Positive NOR Gate		9N27/7427	9N27/5427
Dual 4-Input Positive NOR Gate (with strobe)		9N23,25/7423,25	9N23,25/5423,25
AND GATES			
Quad 2-Input Positive AND Gate		9N08/7408	9N08/5408
Quad 2-Input Positive AND Gate (Open Collector)		9N09/7409	9N09/5409
Triple 3-Input Positive AND Gate		9N11/7411	9N11/5411
Dual 4-Input Positive AND Gate			
OR GATES			
Quad 2-Input Positive OR Gate		9N32/7432	9N32/5432
EXCLUSIVE-OR GATES			
Quad Exclusive-OR Gate	9L86	9N86/7486	9N86/5486
Quad Exclusive-OR Gate with Inverted Outputs			
AND-OR, AND-OR-INVERT GATES AND EXPANDERS			
Expandable 2-2-2-3 Input AND-OR Gate			
Dual 2-Wide 2-Input AND-OR-INVERT Gate		9N51/7451	9N51/5451
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate		9N50/7450	9N50/5450
Expandable 2-Wide, 4-Input AND-OR-INVERT Gate			
4-Wide 2-Input AND-OR-INVERT Gate	9L54	9N54/7454	9N54/5454
4-2-3-2-Input AND-OR-INVERT Gate			
4-2-3-2-Input AND-OR-INVERT Gate (Open Collector)			
Expandable 4-Wide 2-Input AND-OR-INVERT Gate		9N53/7453	9N53/5453
Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate			
Triple 3-Input Expander			
Dual 4-Input Expander		9N60/7460	9N60/5460
3-2-2-3-Input AND-OR Expander			
INVERTERS AND BUFFERS			
Hex Inverter	9L04	9N04/7404	9N04/5404
Hex Inverter with Open-Collector Output		9N05/7405	9N05/5405
Hex Inverter Buffer/Driver (30 Volts)		9N06/7406	9N06/5406
Hex Inverter Buffer/Driver (15 Volts)		9N16/7416	9N16/5416
Hex Buffer/Drivers (30 Volts)		9N07/7407	9N07/5407
Hex Buffer/Drivers (15 Volts)		9N17/7417	9N17/5417
Quad 2-Input Positive NAND Buffer		9N37/7437	9N37/5437
Quad 2-Input Positive NAND Buffer (Open Collector)		9N38/7438	9N38/5438
Quad 2-Input Positive NAND Buffer (Open Collector - 15 Volts)		9N39/7439	
Dual 4-Input Positive NAND Buffer		9N40/7440	9N40/5440
Dual 4-Input Positive NAND 50 Ω Driver			
SCHMITT TRIGGER			
Dual NAND Schmitt Trigger		9N13/7413	9N13/5413

SSI • GATES, BUFFERS AND INVERTERS

STANDARD	HIGH SPEED		SUPER HIGH SPEED (SCHOTTKY)	
t_{pd} = 8 ns P_d = 10 mW per Gate	t_{pd} = 6 ns P_d = 22 mW per Gate		t_{pd} = 3 ns P_d = 19 mW per Gate	
0°C to +70°C and −55° to +125°C	0° to +70°C	−55° to +125°C	0° to +70°C	−55° to +125°C
9002	9H00/74H00	9H00/54H00	9S00/74S00	9S00/54S00
	9H01/74H01	9H01/54H01		
9012			9S03/74S03	*9S03/54S03
9003	9H10/74H10	9H10/54H10	*9S10/74S10	*9S10/54S10
9004	9H20,22/74H20,22	9H20,22/54H20,22	9S20,22/74S20,22	9S20*, 22/54S20*, 22
9007	9H30/74H30	9H30/54H30		

9015				

	9H08/74H08	9H08/54H08		
	9H11/74H11	9H11/54H11	*9S11/74S11	*9S11/54S11
	9H21/74H21	9H21/54H21		

9014				

	9H52/74H52	9H52/54H52		
	9H51/74H51	9H51/54H51		
9005	9H50/74H50	9H50/54H50		
	9H55/74H55	9H55/54H55		
	*9H54/74H54	*9H54/54H54		
			9S64/74S64	9S64/54S64
			9S65/74S65	*9S65/54S65
	*9H53/74H53	*9H53/54H53		
9008				
	9H61/74H61	9H61/54H61		
9006	9H60/74H60	9H60/54H60		
	*9H62/74H62	*9H62/54H62		

9016	9H04/74H04	9H04/54H04	9S04/74S04, 9S04A	9S04/54S04, 9S04A
9017	9H05/74H05	9H05/54H05	9S05/74S05, 9S05A	*9S05/54S05, *9S05A
9009	9H40/74H40	9H40/54H40	9S40/74S40	9S40/54S40
			9S140/74S140	9S140/54S140

*To be announced.

SELECTOR GUIDE/FUNCTIONAL INDEX

SSI MONOSTABLES

Function	Type No.	Pulse Width Variation (%) vs. Temp	Pulse Width Variation (%) vs. V_{CC}	Number of Inputs Positive	Number of Inputs Negative	Resettable	Min. Output t_{pw} ns	Power Dissipation mW	Page No.
Single Retriggerable	9600	±1.5	±1.5	3	2	x	75	125	7-1
	9601	±2.7	±1.0	2	2		50	125	7-6
Dual Retriggerable	9602	±1.5	±1.5	1	1	x	72	250	7-11
	96L02	±0.4	±1.5	1	1	x	110	50	7-16
Single Non-Retriggerable	9603	±0.2	±0.15	1	2		40	90	7-21

SSI INTERFACE — DRIVERS

Function	Type No.	Companion Receiver	Supply Voltages V	V_{OH} V	V_{OL} V	t_{pd} ns	Power Dissipation mW	Page No.
Single +5 V Operation	9614	9615	+5.0	+3.2	+0.2	16	175	7-25
EIA RS232 Operation	9616	9617	+12 −12	+6	−6	300	250	7-27
	9621	9620 9622	+5 −12	+4.3	+0.2	10	120	7-30
General Purpose	75109	75107	+5 −5	O.C.*	O.C.*	9	180	7-35
	75110	75108	+5 −5	O.C.*	O.C.*	9	180	7-35
High Voltage	9644		+5	30	0.8	50	120	7-33
	75450		+5	30	0.4	20	30	7-36

*Open Collector

SSI INTERFACE — RECEIVERS

Function	Type No.	Companion Driver	Supply Voltages V	V_{TH} V	V_{CM} V	Output Enable	Diff. Inputs	t_{pd} ns	Power Dissipation mW	Page No.
Single +5 V Operation	9615	9614	+5	±0.5	±15	x	x	28	175	7-26
EIA RS-232 Operation	9617	9616	+5	+1.5	±25			50	100	7-28
General Purpose	9620	9621	+5 −12	±0.5	±15		x	30	110	
	9622	9621	+5 −10	±2.0	±10	x	x	35	140	7-31
	75107	75109	±5	±0.25	±3	x	x	19	180	7-34
	75108	75110	±5	±0.25	±3	x	x	19	180	7-34

SSI INTERFACE — LEVEL TRANSLATORS

Function	Type No.	Supply Voltages +V	Supply Voltages −V	V_{OH} V	V_{OL} V	t_{pd} ns	Power Dissipation mW	Page No.
TTL — MOS Dual 2-Input w/Expander	9624	5.0	0 — 30	−0.5	+0.2	120	40	7-32
MOS — TTL Dual Buffer	9625	5.0	0 — 30	+0.4	+2.6	70	60	7-32
*HLL — TTL Hex-Inverter	9109	12—20	0	2.4—5.5	0.4	120	380	**
TTL — *HLL Hex-Inverter	9112	12—20	0	10—18		90	440	**

*HLL = HIGH Level Logic

**For Data Sheet write FSC, P.O. Box 880A, Mt. View, California 94040

MSI ARITHMETIC OPERATORS
ADDERS, A.L.U.'S, COMPARATORS, MULTIPLIERS

Function	Type No.	Description	Number of Bits	t_{pd} ns	Power Dissipation mW	Page No.
Addition	9380	Single 1-Bit Full Adder	1	47	105	8-215
	9304	Dual 1-Bit Full Adder	1	26	150	8-24
	93H183	Dual 1-Bit Full Adder	1	12	250	8-288
	9382	Single 2-Bit Full Adder	2	38	176	8-221
	9383	Single 4-Bit Full Adder	4	39	390	8-225
Arithmetic Logic Units	9340	ALU with Internal CLA	4	24	400	8-148
	9341	ALU with External CLA	4	24	450	8-153
	93S41	ALU with External CLA	4	11	500	8-158
CLA Carry Look-Ahead	9342	For Use with 9341		12	180	8-163
	93S42	For Use with 93S41		7	260	8-167
Multiplication	9344	Binary Full Multiplier	4 x 2	30	550	8-168
Compare	9324	Magnitude Comparator	5	20	210	8-124
	93L24	Magnitude Comparator	5	55	55	8-128
	9386	Identity Comparator (Quad EX—NOR)	4	18	170	8-230
Parity	9348	Parity Checker/Generator	12	40	270	8-177
	93S62	Parity Checker/Generator	9	16	350	8-206
True/Complement Generation	93H87	True/Complement, Zero/One Element	4	14	270	8-232

MSI COUNTERS

Function	Type No.	Parallel Load	Count Enable	Clock Transitions	Async. Clear	Count Rate MHz	t_{pd} ns	Power Dissipation mW	Page No.
Variable Modulo	9305			L—H	L	26	55	195	8-28
	93S05			L—H	L	100	25	400	8-33
Decade Synchronous	9310	S	H	L—H	L	45	15	325	8-54
	93L10	S	H	L—H	L	20	25	75	8-60
	93S10	S	H	L—H	L	90	8	400	8-65
Decade Asynchronous	9350			H—L	H	18	60	160	8-180
	9390			H—L	H	18	60	160	8-236
	93176	A		H—L	L	25	30	185	8-282
	93196	A		H—L	L	70	28	250	8-297
Decade Up/Down	9360	A		L—H	H	30	30	300	8-203
	93190	A	L	L—H		25	37	325	8-292
Binary Synchronous	9316	S	H	L—H	L	45	15	325	8-54
	93L16	S	H	L—H	L	20	25	75	8-60
	93S16	S	H	L—H	L	90	8	400	8-65
Binary Asynchronous	9356			H—L	H	18	75	160	8-188
	9393			H—L	H	18	75	160	8-248
	93177	A		H—L	L	25	30	185	8-282
	93197	A		H—L	L	70	42	250	8-297
Binary Up/Down	9366	A		L—H	H	30	30	300	8-203
	93191	A	L	L—H		25	37	325	8-292
Divide by 12	9392			H—L	H	18	60	160	8-244

S = Synchronous
A = Asynchronous

MSI DECODERS/DEMULTIPLEXERS

Function	Type No.	Active LOW Outputs No.	Separate Enable	Wired-OR Capability	Select Delay ns	Enable Delay ns	Power Dissipation mW	Page No.
Dual 1-of-4 (BCD)	9321	2 x 4	x		22	17	150	8-111
	93L21	2 x 4	x		50	38	45	8-114
1-of-8	9301	8	x		22	22	145	8-15
	9334	8*	x		22	19	280	8-138
	9302	8	x	x	30	30	145	8-21
1-of-10 (BCD)	9301	10			22		145	8-15
	93L01	10			63		45	8-18
	9302	10		x	30		145	8-21
	9345	10		x	50		215	8-173
	9352	10			24		140	8-183
1-of-10 (Excess 3)	9353	10			24		140	8-183
	9354	10			24		140	8-183
1-of-16	9311	16	x		21	17	175	8-66
	93L11	16	x		70	48	58	8-69
Programmable	93402	4**	x	x	25	25	500	9-6

*9334 is an 8-Bit addressable latch which can be used as an active HIGH decoder or demultiplexer.

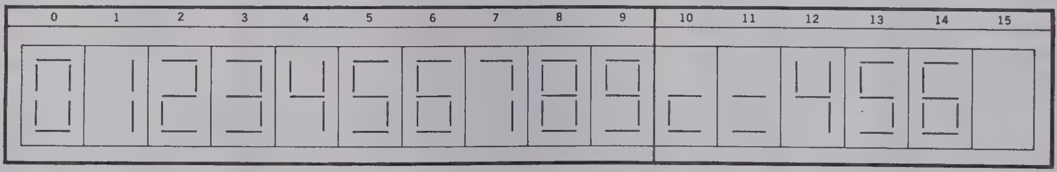
**93402 is a 4x4 content addressable memory which can also be used as a programmable decoder.

MSI DISPLAY DECODER/DRIVERS

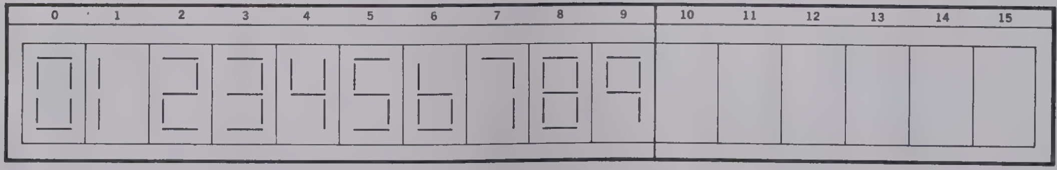
Function	Type No.	Output Sink mA	Output Voltage V	Pull-Up Resistors	Ripple Blanking	Blanking Above BCD 9 Input	Power Dissipation mW	Page No.
1-of-10 (Cold Cathode)	9315	7	55				100	8-95
	93141	7	55			x	105	8-261
1-of-10 (Incandescent, Relays Actuators)	9302	16	5			x		8-21
	9345	80	30			x	215	8-173
	93145	80	15			x	215	8-173
7-Segment (Decoder)	9307	11	5	x	x		165	8-34
	9358	8	5	x	x		265	8-197
	9359	9.6	5				167	8-197
7-Segment (Incandescent or LED)	9317B	40	20		x	x	220	8-98
	9317C	20	30		x	x	220	8-98
	9357A	20	30		x		265	8-191
	9357B	20	15		x		265	8-191

7-SEGMENT DECODING FORMATS

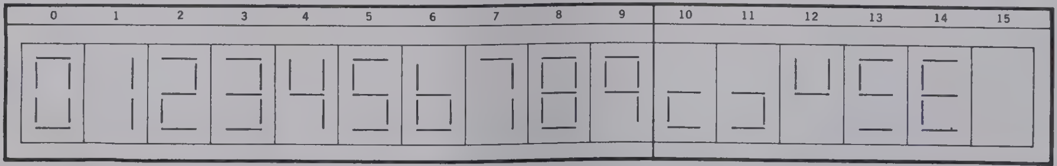
9307



9317



9357A, 9357B, 9358 and 9359



SELECTOR GUIDE/FUNCTIONAL INDEX

MSI ENCODERS

Function	Type No.	Description	t_{pd} ns	Power Dissipation mW	Page No.
Encoders	9318	8-Input Priority Encoder	25	250	8-103
	93L18	8-Input Priority Encoder	55	70	8-107

MSI LATCHES

Function	Type No.	R-S Input	D Input	Enable Active	Clear	Reset	t_{pd} Enable ns	t_{pd} Data ns	Power Dissipation mW	Page No.
4-Bit	9314	x	x	L	x	x	20	10	175	8-85
	93L14	x	x	L	x	x	70	45	50	8-90
	9375		x	H			16	16	160	8-211
	9377		x	H			16	16	160	8-211
Dual 4-Bit	9308		x	L	x	x	20	15	340	8-38
	93L08		x	L	x	x	65	50	90	8-43
Addressable 8-Bit	9334*		x	L	x	x	20	30	280	8-138

*Addressable latch with single D-Input and three address lines.

MEMORIES

Function	Type No.	Organization Words	Organization Bits	Decoding Scheme	Wired-OR Output	Address Access ns	Chip Select Access ns	Power Per Bit mW	Page No.
16-Bit RAM	93407	16	1	1-of-4/1-of-4 Coincident Select	x	15		20	9-23
	93433	16	1		x	15		20	9-23
64-Bit RAM	93403	16	4	Full	x	40	40	8	9-10
	93435	16	4	1-of-16 Select	x	20	20	8	9-38
256-Bit RAM	93400	256	1	3-of-6/3-of-6	x	70	70	2	9-1
	93410	256	1	Full	x	30	20	1.8	9-27
1024-Bit RAM	93415	1024	1	Full	x	75	40	0.5	9-32
256-Bit ROM	93434	32	8	Full	x	40	40	2	9-35
1024-Bit ROM	93406	256	4	Full	x	40	30	0.7	9-13
8-Bit Multiple Port	9338	8	1	Full		25		50	8-142
	93S39	8	1	Full		12		60	8-147
16-Bit Associative	93402	4	4	Linear Select	x	20		25	9-6

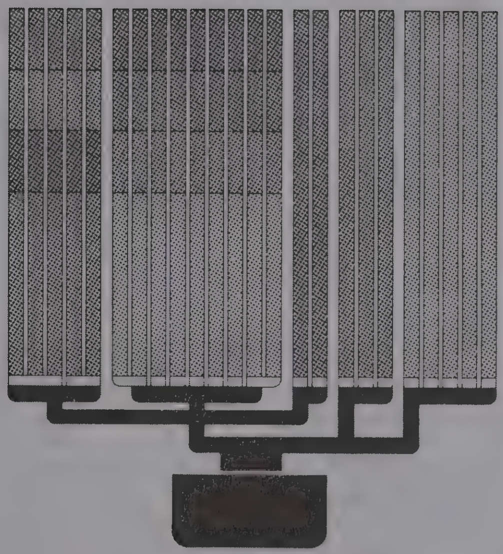
MSI MULTIPLEXERS

Function	Type No.	Enable Input	Complementary Output	Wired-OR Capability	Data Z Delay ns	Data $\overline{Z}$ Delay ns	Select Delay ns	Enable Delay ns	Power Dissipation mW	Page No.
Quad 2-Input	9322	x			10		19	15	125	8-117
	93L22	x			44		38	30	45	8-121
Dual 4-Input	9309		x		17	9	24		150	8-47
	93L09		x		34	18	48		40	8-51
	93153	x			15		22	19	180	8-272
Single 8-Input	9312	x	x		19	9	24	14	135	8-72
	93L12	x	x		80	18	48	28	34	8-76
	93S12	x	x		8	5	12	7	250	8-79
	9313	x	x	x	26	20	30	25	135	8-80
	93151	x	x		18	10	28	18	150	8-265
	93152					10	28		130	8-265
Single 16-Input	93150	x				10	28	18	200	8-265

MSI REGISTERS

Function	Type No.	No. Bits	Serial Data Input	Parallel Data Input	Reset Active	Clock Enable	Shift Frequency MHz	Clock to Output ns	Power Dissipation mW	Page No.
General Purpose	9300	4	J–K	S	L		35		300	8-1
	93L00	4	J–K	S	L		10	55	75	8-10
	93H00	4	J–K	S	L		55	10	375	8-6
	93S00	4	J–K	S	L		100	7	400	8-14
	93H72	4	D	S	L	x	60	10	400	8-207
	9394	4	D	A	H		15	25	175	8-252
	9395	4	D	S			36	21	250	8-254
	9396	5	D	A	L		15	25	240	8-259
	93178	4	D	S		x	22	25	170	8-283
	93179	4	D	S	L	x	22	25	270	8-283
Parallel-In/ Parallel-Out	93198	8	D	S	L	x	35	20	370	8-301
Serial/Parallel Converters	93164	8	D		L		20	20	180	8-276
	93165	8	D	A		x	20	20	230	8-279
Multiple Port	9338	8	D					25	265	8-142
	93S39	8	D					12	400	8-147
Serial-In Serial-Out	9328	16	D		L	x	25	15	300	8-131
	93L28	16	D		L	x	10	50	75	8-135

S = Synchronous
A = Asynchronous



TTL Loading Rules

All devices in the Fairchild TTL family have compatible logic levels. Standard, low power and high speed device, may be mixed in a system to obtain the optimum cost, power, speed combination.

To simplify design calculations the different loading rules of each series have been normalized to one standard set of conditions.

4
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12

TTL LOADING RULES

All Transistor Transistor Logic integrated circuits are derived from the simple gate schematic shown in Figure 1.

The output is LOW (logic "0") only if both inputs A and B are HIGH (logic "1"). This is defined as a positive logic NAND gate.

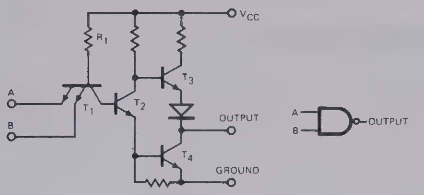


FIGURE 1

Input Characteristics

A low voltage at inputs A or B will cause current to flow out of the forward biased base-emitter diode of the multi-emitter transistor. (T_1). When the voltage level at A or B or both is less than 2 $V_{BE(SAT)}$ levels, the current supplied by R_1 will flow out of the LOW input terminal (see Figure 2) keeping transistors T_2 and T_4 turned off. If both inputs A and B are raised to a HIGH voltage level, the base-emitter diodes of the input transistor (T_1) will be reverse biased. The current supplied by R_1 will then flow through the base-collector diode of T_1 (see Figure 3) turning on transistor T_2 and T_4. The HIGH level input voltage source must be capable of supplying leakage current to the reverse biased input transistor. Because of the NPN action of the input device, this leakage current is referred to as inverse beta current. The value of the input LOW current and input HIGH leakage current is dependent on the value of R_1. The value of this resistor is chosen to optimize the specific speed/power performance characteristics of each device.

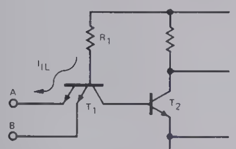


FIGURE 2

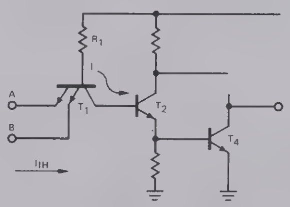


FIGURE 3

Output Characteristics

The fan out or drive capability of a TTL device reflects its ability to sink current in the output LOW (logic "0") state (see Figure 4) and to source or drive current in the output HIGH (logic "1") state (see Figure 5).

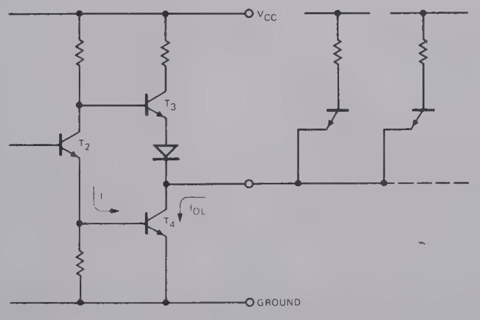


FIGURE 4

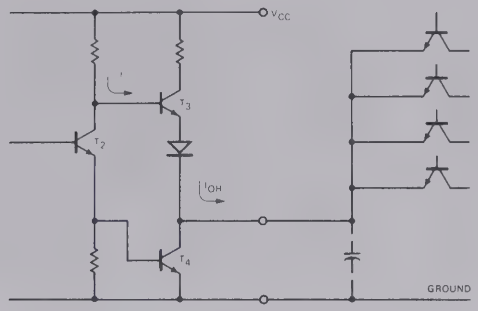


FIGURE 5

In the output LOW state the "phase splitter" transistor T_2 is "on". It supplies base drive to the output pull down transistor (T_4). The amount of base drive required for the pull down transistor is dependent on the worst case beta of the device and the fan out (I_{OL}) sink current requirements of the circuit. The output HIGH drive current (I_{OH}) of the device is supplied from the pull up transistor (T_3). When the phase splitter transistor (T_2) is turned "off", the pull up transistor is turned "on". This presents a low impedance drive source at the output. Although the static I_{OH} requirements of most circuits is less than 0.5 mA, about 35 mA is made available at the instant of LOW to HIGH output transition to charge up the distributed line, board and package capacitances encountered in most system designs. Different types of pull up circuits are used to achieve faster system speeds by minimizing HIGH output impedance and the resulting RC time constant.

Normalized Fan In/Fan Out Rules

In order to simplify designing with Fairchild TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 Unit TTL Load (U.L.) = 40 μA in the HIGH state (logic "1")
= 1.6 mA in the LOW state (logic "0")

Input loading and output drive factors of all products described in this catalog are related to these definitions.

Examples — Input Load

1. A 9N00/7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan in of 1 load.)
2. The 93H72, which has a value of $I_{IL} = 3.2$ mA and I_{IH} of 80 μA on the CP terminal, is specified as having an input load factor of $\frac{3.2\text{ mA}}{1.6\text{ mA}}$ or 2 U.L.

Examples — Output Drive

1. The output of the 9N00/7400 will sink 16 mA in the LOW (logic "0") state and source 800 μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore $\frac{16\text{ mA}}{1.6\text{ mA}} = 10$ U.L. and the output HIGH drive factor is $\frac{800\ \mu\text{A}}{40\ \mu\text{A}} = 20$ U.L.

Relative load and drive factors for the basic TTL gate families specified in this catalog are given in Table 1.

Table I

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9H00/74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
9L00	0.5 U.L.	0.25 U.L.	10 U.L.	2.5 U.L.
9N00/7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9S00/74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

DC Noise Margin

The loading rules defined above have been determined under test conditions chosen to insure useful worst case noise margin values over the full temperature and supply voltage ranges specified for the Fairchild TTL families.

Noise margin is defined in Figure 6 as the difference between the worst case output logic voltage and the worst case input voltage which guarantees the desired output level.

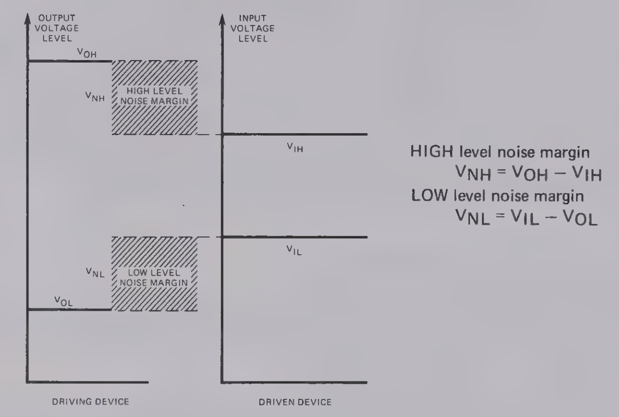


FIGURE 6

Table II below lists the worst case dc logic levels for Fairchild TTL devices.

Table II

PARAMETER	DEFINITION	9300 9N/54, 74 9H/54H, 74H	93L00 9L00	93S00 9S/74S	9S/54S
V_{OH}	Minimum Output Voltage in the HIGH State	2.4 V	2.4 V	2.5 V	2.7 V
V_{OL}	Maximum Output Voltage in the LOW State	0.4 V	0.3 V	0.5 V	0.5 V
V_{IH}	Minimum Voltage Level Which is Guaranteed to be Interpreted as a HIGH at the Input	2.0 V	2.0 V	2.0 V	2.0 V
V_{IL}	Maximum Voltage Level Which is Guaranteed to be Interpreted as a LOW at the Input	0.8 V	0.7 V	0.8 V	0.8 V

Example

1. The worst case guaranteed dc noise margin for a 9300 MSI interfacing with another 9300 MSI is therefore:

$$V_{NH} = 2.4 - 2.0 = 400 \text{ mV}$$
$$V_{NL} = 0.8 - 0.4 = 400 \text{ mV}$$

2. The worst case guaranteed noise margin for a 74S00 gate driving a 7400 gate is therefore:

$$V_{NH} = 2.7 - 2.0 = 700 \text{ mV}$$
$$V_{NL} = 0.8 - 0.5 = 300 \text{ mV}$$

Wired-OR Applications

Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull up resistor.

The value of the pull up resistor is determined by considering the fan out of the OR tie and the number of devices in the OR tie. The pull up resistor value is chosen from a range between a maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan out is not exceeded when only one output is LOW).

Minimum and Maximum Pull Up Values

$$R_X \text{ (Min.)} = \frac{V_{CC} \text{ (max.)} - V_{OL}}{I_{OL} - N_2 I_{IL}}$$

$$R_X \text{ (Max.)} = \frac{V_{CC} \text{ (min.)} - V_{OH}}{N_1 I_{CEX} + N_2 I_{IH}}$$

Where

R_X = External Pull Up Resistor
N_1 = Number of Wired-OR Outputs
N_2 = Number of Input Unit Loads Being Driven
$I_{CEX}(I_{OH})$ = Output HIGH Leakage Current
I_{OL} = LOW Level Fan Out Current of Driving Element
I_{IH} = Input HIGH U.L. (40 μA)
I_{IL} = Input LOW U.L. (1.6 mA)
V_{OL} = Output LOW Voltage Level (0.4 V)
V_{OH} = Output HIGH Voltage Level (2.4 V)
V_{CC} = Power Supply Voltage

Example: Four 9N01/7401 gates driving four other gate or MSI inputs.

$N_1 = 4$
$N_2 = 4$ (U.L.)
$I_{CEX} = 250\ \mu A$
$I_{OL} = 16$ mA
$I_{IH} = 40\ \mu A$
$I_{IL} = 1.6$ mA
$V_{OL} = 0.4$ V
$V_{OH} = 2.4$ V

$$R_X \text{ (min.)} = \frac{5.25 \text{ V} - 0.4 \text{ V}}{16 \text{ mA} - 4(1.6 \text{ mA})} = \frac{4.85 \text{ V}}{9.6 \text{ mA}}$$

$$R_X \geqslant 505\ \Omega$$

$$R_X \text{ (max.)} = \frac{4.75 \text{ V} - 2.4 \text{ V}}{4(0.250 \text{ MA}) + (0.04 \text{ mA})} = \frac{2.35 \text{ V}}{1.16 \text{ mA}}$$

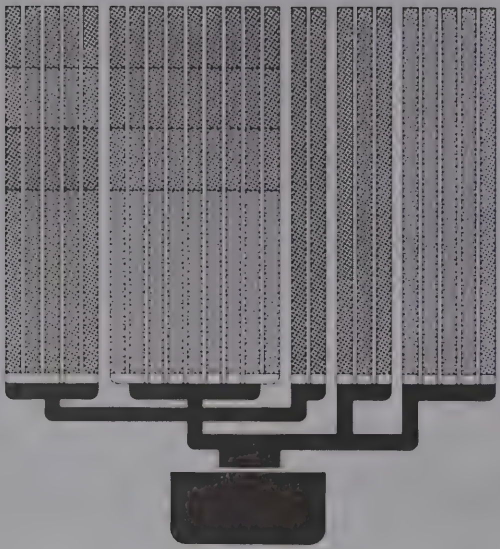
$$R_X \leqslant 2.03 \text{ k}\Omega$$

Unused Inputs

To minimize noise sensitivity and optimize switching times, unused inputs of all TTL circuits should be held between 2.4 V and the absolute maximum 5.5 V. This eliminates the effect of the distributed capacitance associated with the floating input, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect unused inputs to a used input if maximum HIGH level fan out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a HIGH level voltage but adds no loading at a LOW level voltage. The HIGH level fan out for all circuits has been specified at double the LOW level fan out specifically to provide for this method of treating unused inputs.
2. Connect unused inputs to V_{CC} through a 1 kΩ resistor. If a transient exceeding the 5.5 V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1 kΩ resistor.
3. Tie the inputs to the output of an unused gate in the system. The gate must provide a constant HIGH level output.
4. Connect unused inputs to an independent supply voltage in the range of 2.4 V to 3.5 V.



SSI
9000, 9H(54/74H), 9L, 9N(54/74) and 9S(54/74S) Series Data Sheets

This section comprises data sheets on the five basic Fairchild TTL/SSI series.

9000
9H00/54H, 74H00
9L00
9N00/54, 7400
9S00/54S, 74S00

Devices are presented in alpha-numerical sequence, with the exception of the 9000. elements. All 9000 series functions are grouped together at the beginning of this section.

TTL/SSI INTRODUCTION

INTRODUCTION – The Fairchild TTL/SSI line offers the designer a broad selection of gates and flip-flops for use with Fairchild MSI, Interface and Memory products in implementing TTL system designs. These TTL/SSI functions are available for use in military and industrial temperature range applications. These products are available in the popular Dual In-Line package as well as flat packages. All Fairchild TTL products are logic and supply voltage compatible so that circuit families may be mixed within a system for optimum speed, power and economy.

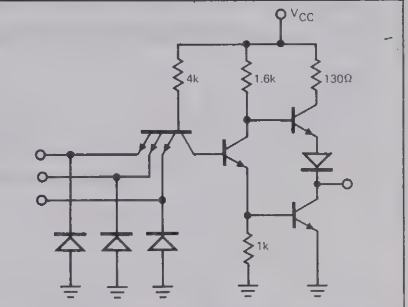
9N/54, 74 SERIES TTL/SSI

FEATURES

- 10 ns Typical Gate Delay
- 10 mW Typical Gate Power Dissipation
- Input Clamp Diodes Minimize Termination Effects
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages

DESCRIPTION

The 9N/54, 74 Series is a broad family of SSI devices which are pin and function identical with the popular 7400 series. These gates and binaries are available in industrial and military temperature ranges in both DIP and Flat packages. The line included NAND gates, NOR gates, Exclusive-OR gates, AND gates, open collector gates as well as single and dual flip-flops.



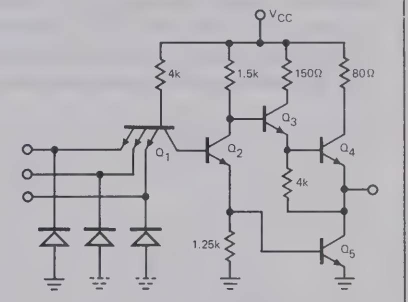
9000 SERIES TTL/SSI

FEATURES

- 8 ns Typical Gate Delay
- 10 mW Typical Gate Power Dissipation
- Input Clamp Diodes Reduce Termination Effects
- Darlington Output Stage Increases Circuit Speed
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages

DESCRIPTION

The 9000 Series of gates and flip-flops offers a family of high speed functions with speed and power specifications in between the 9N/54, 74 Series and the 9H/54H, 74H Series. The Darlington output stage provides faster switching times and increased capacitive drive capability over the 9N/54, 74 Series.



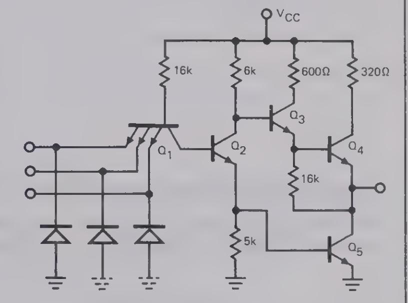
9L SERIES LPTTL/SSI

FEATURES

- 20 ns Typical Gate Delay
- 2 mW Typical Gate Power Dissipation
- Input Clamp Diodes Minimize Termination Effects
- Darlington Output Stage Increases Circuit Speed
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages

DESCRIPTION

The 9L Series of low power TTL gates and flip-flops offers a speed/power trade-off well suited to both industrial and military applications. The power is one fourth that of a standard TTL gate and typical system speeds of up to 10 MHz are possible. The 9L Series TTL/SSI functions are used with the 93L low power TTL/MSI devices to implement low power, moderate speed systems.



9H/54H, 74H SERIES HSTTL/SSI

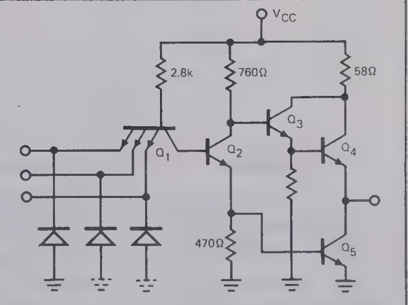
FEATURES

- 6 ns Typical Gate Delay
- 22 mW Typical Gate Power Dissipation
- Input Clamp Diodes to Minimize Termination Effects
- Darlington Output State to Increase Circuit Speed
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages
- 11 Functions Available

DESCRIPTION

The 9H/54H, 74H Series is a line of high speed gates and flip-flops which are pin and function identical with the popular 74H00 Series.

These devices are used with the 9300 and 93H Series of TTL/MSI devices to substantially reduce critical path delay times and enhance overall system speeds.



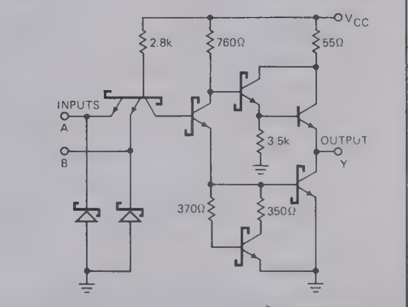
9S/54S, 74S SERIES TTL/SSI

FEATURES

- 3 ns Typical Gate Delay
- 125 MHz Typical Input Clock Frequency for J-K Flip-Flops
- 22 mW Gate Power Dissipation
- Input Clamp Diodes to Minimize Termination Effects
- Low Output Impedance to Drive High Capacitive Loads

DESCRIPTION

The 9S00 Series is a line of super high speed devices featuring Schottky-barrier diode clamping on all normally saturated devices. The result is an overall improvement in propagation delays and greatly reduced sensitivity of delay times to temperature variation. These gate and flip-flop functions can be used with Fairchild's 93S00 Series of MSI Schottky-clamped logic elements to achieve the highest possible system speeds and still maintain typical 1.0 V noise immunity.



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	0.5 V to $+V_{CC}$
Output Current (dc) (Output LOW)	
9N/54,74 and 9L Series	+30 mA
9000, 9H and 9S Series	+50 mA
See Detail Data Sheets for Buffer Drive Capability.	

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

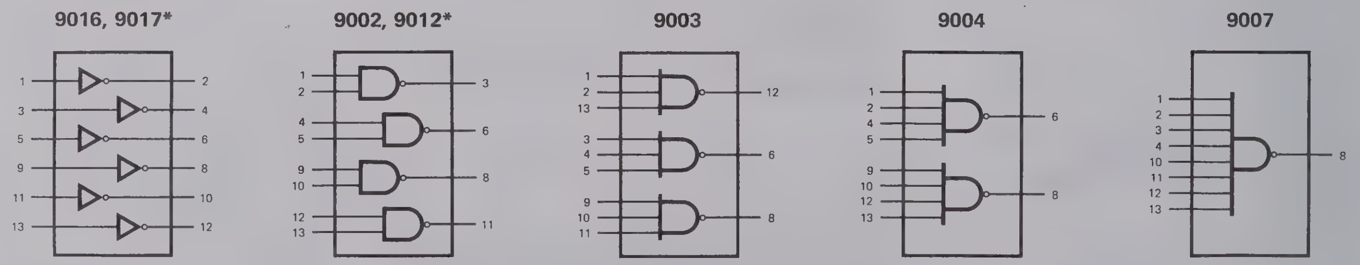
INPUT AND OUTPUT LOAD FACTORS FOR THE 9000 SERIES GATES & FLIP-FLOPS

The test conditions and resulting limits for the input and output levels of the 9000 Series gates and flip-flops differs from the other 9N, 9H, 9L, and 9S series of devices. These 9000 Series levels and conditions are equivalent to the other families for all practical purposes. For instance, an input HIGH level current guaranteed to be 60 μA when measured at 4.5 V, will be less than 40 μA for most operating conditions. Therefore, the load factors for the 9000 Series has been normalized to simplify system design considerations.

NAND GATES – 9002, 9003, 9004, 9007 AND 9012*
HEX INVERTER – 9016 AND 9017*

The 9002, 9003, 9004, 9007 and 9012 are active LOW level output AND gates commonly known as NAND gates. The 9016 and 9017 are hex inverters with input and output characteristics identical to NAND gate. The variety of gate combinations provides the system designer the utmost in logic flexibility and reduces package count.

LOGIC SYMBOL AND PIN CONFIGURATIONS



*Open Collector

V_{CC} = Pin 14,
GND = Pin 7

Fig. 1

BASIC GATE CIRCUIT

Nominal Resistor Values
$R_1 = R_5 = 4.0\ k\Omega$
$R_2 = 1.5\ k\Omega$
$R_3 = 150\ \Omega$
$R_4 = 80\ \Omega$
$R_6 = 1.25\ k\Omega$

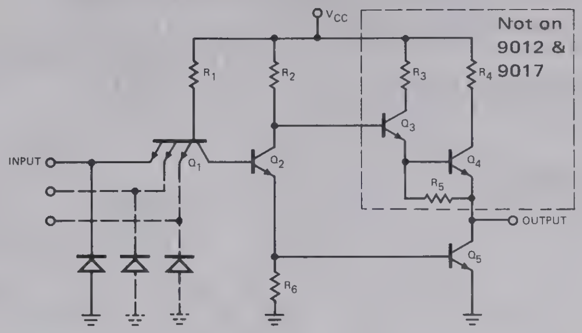


Fig. 2

LOADING FACTORS

PIN NAMES	LOADING
All Inputs	1 U.L.
All Outputs	10 U.L.*

(1 U.L. = 40 µA HIGH/1.6 mA LOW)

*The 9012 & 9017 need external resistors to provide HIGH level drive.

Fig. 3

ELECTRICAL CHARACTERISTICS 9002XC, 9003XC, 9004XC, 9007XC, 9012XC, 9016XC AND 9017XC (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER		LIMITS							UNITS	TEST CONDITIONS	
			0°C		25°C			75°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{IH}	Input HIGH Voltage		1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage (except 9012, 9017)		2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA, Inputs at V_{IL}	
V_{OL}	Output LOW Voltage			0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 16.0 mA, V_{IN} = 5.25 V	
											V_{CC} = 4.75 V, I_{OL} = 14.1 mA, Inputs at V_{IH}	
I_{IH}	Input HIGH Current					10	60		60	µA	V_{CC} = 5.25 V, V_{IN} = 4.5 V GND on Other Inputs	
I_{IL}	Input LOW Current			−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V	V_{IN} = 0.45 V
				−1.41		−0.91	−1.41		−1.41		V_{CC} = 4.75 V	5.25 V on Other Inputs
I_{CEX}	Output Reverse Current 9012, 9017 only					2.0	250		250	µA	V_{CC} = 4.75 V, V_{IN} = V_{IL}, V_{OUT} = 5.5 V	
I_{CC}	V_{CC} Current, Gate On (each gate)			6.1		3.6	6.1		6.1	mA	Inputs HIGH	V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)			1.7		1.07	1.7		1.7		Inputs at GND	
t_{PLH}	Turn OFF Delay Input to Output				3.0		13			ns		V_{CC} = 5.0 V, C_L = 15 pF See Fig. 12
		9012, 9017 only			3.0		45				R_L = 4.0 kΩ	
t_{PHL}	Turn ON Delay Input to Output				3.0		15			ns		
		9012, 9017 only			3.0		15				R_L = 400 Ω	

ELECTRICAL CHARACTERISTICS 9002XM, 9003XM, 9004XM, 9007XM, 9012XM, 9016XM, AND 9017XM (T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%)

SYMBOL	PARAMETER		LIMITS							UNITS	TEST CONDITIONS	
			−55°C		25°C			125°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{IH}	Input HIGH Voltage		2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage (except 9012, 9017)		2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.32 mA, Inputs at V_{IL}	
V_{OL}	Output LOW Voltage			0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 17.6 mA, V_{IN} = 5.5 V	
											V_{CC} = 4.5 V, I_{OL} = 13.6 mA, Inputs at V_{IH}	
I_{IH}	Input HIGH Current					10	60		60	µA	V_{CC} = 5.5 V, V_{IN} = 4.5 V GND on Other Inputs	
I_{IL}	Input LOW Current			−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V	V_{IN} = 0.4 V
				−1.24		−0.87	−1.24		−1.24		V_{CC} = 4.5 V	5.5 V on Other Inputs
I_{CEX}	Output Reverse Current 9012, 9017 only					2.0	250		250	µA	V_{CC} = 4.5 V, V_{IN} = V_{IL}, V_{OUT} = 5.5 V	
I_{CC}	V_{CC} Current, Gate On (each gate)			5.5		3.5	5.5		5.5	mA	Inputs HIGH	V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)			1.6		1.07	1.6		1.6		Inputs at GND	
t_{PLH}	Turn OFF Delay Input to Output				3.0		10			ns		V_{CC} = 5.0 V C_L = 15 pF See Fig. 12
		9012, 9017 only			3.0		45				R_L = 4.0 kΩ	
t_{PHL}	Turn ON Delay Input to Output				3.0		12			ns		
		9012, 9017 only			3.0		15				R_L = 400 Ω	

9002, 9003, 9004, 9007, 9012, 9016 AND 9017 TYPICAL INPUT AND OUTPUT CHARACTERISTICS

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

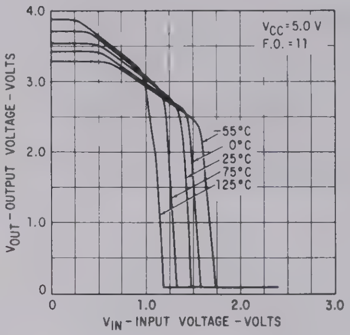


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

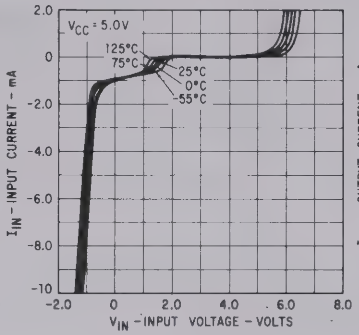


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

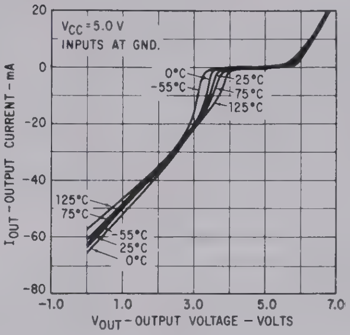


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

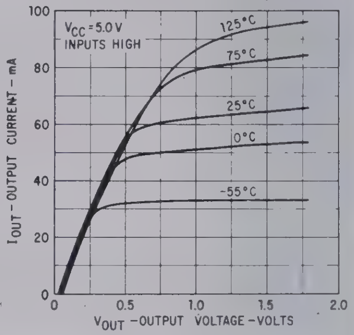


Fig. 7

POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

POWER DISSIPATION VERSUS SUPPLY VOLTAGE

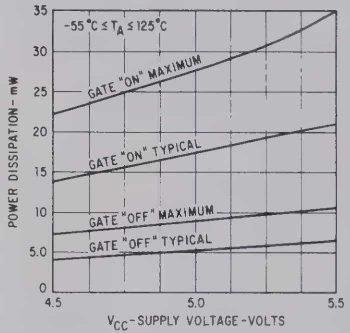


Fig. 8

WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

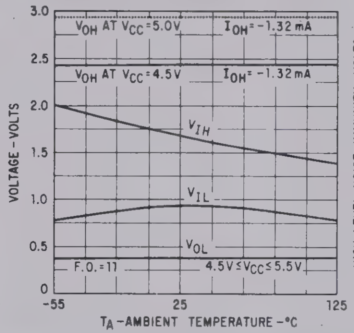


Fig. 9

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

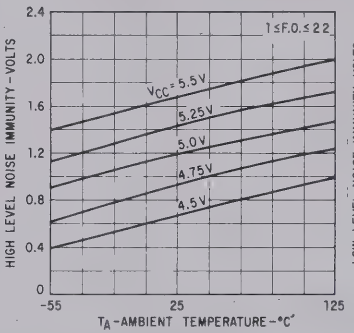


Fig. 10

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

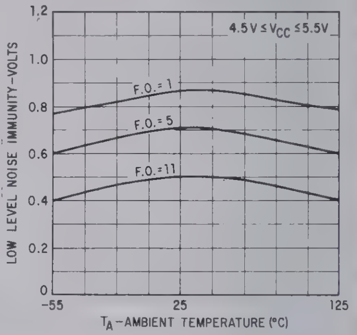
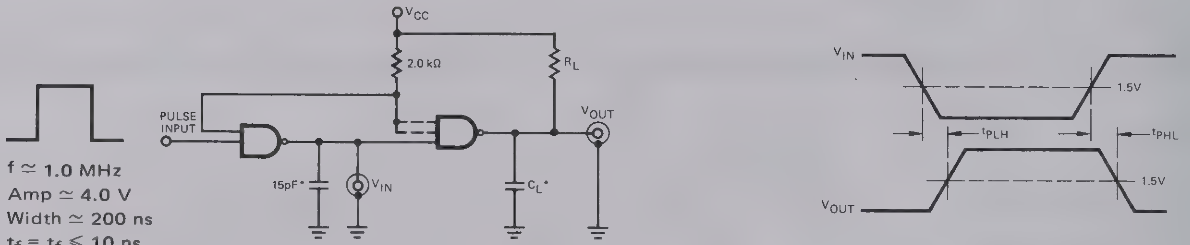


Fig. 11

SWITCHING CHARACTERISTICS

TEST CIRCUIT

WAVEFORM



f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_r = t_f \leqslant 10$ ns

*Includes all probe and jig capacitance

Fig. 12

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

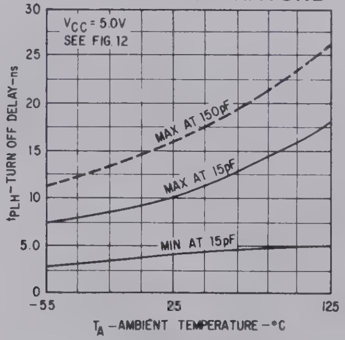


Fig. 13

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

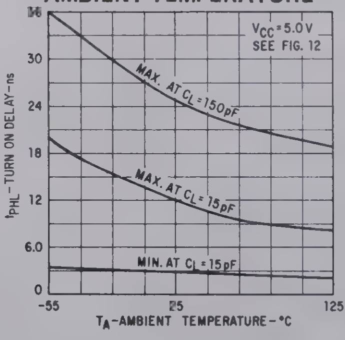


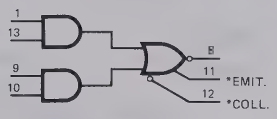
Fig. 14

EXTENDABLE AND-OR-INVERT GATES – 9005, 9008
EXTENDER – 9006

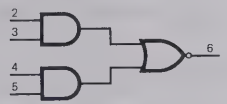
The TTL 9005 and 9008 are AND-OR-INVERT gates which may be OR extended with the use of the 9006. For noise immunity and operating level curves, refer to the gate section.

LOGIC DIAGRAMS

9005
EXTENDABLE GATE


1
13
9
10
8
11
*EMIT.
12
*COLL.

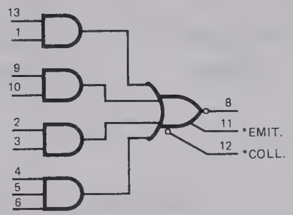
NON-EXTENDABLE GATE



V_{CC} = Pin 14
GND = Pin 7

*Four Extenders (9006) may be tied to these terminals

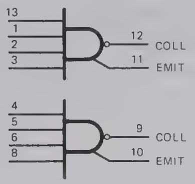
9008


13
1
9
10
2
3
4
5
6
8
11
*EMIT.
12
*COLL.

V_{CC} = Pin 14
GND = Pin 7

*Four Extenders (9006) may be tied to these terminals

9006

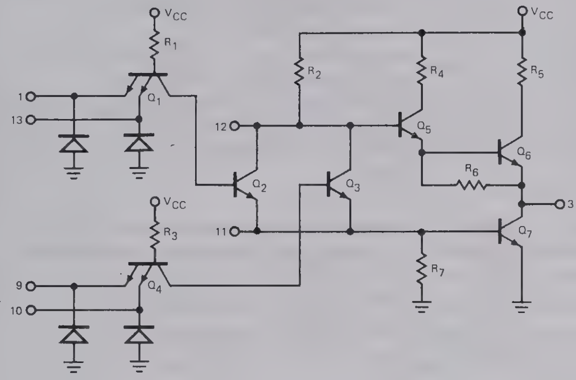

13
1
2
3
12
COLL
11
EMIT
4
5
6
8
9
COLL
10
EMIT

V_{CC} = Pin 14
GND = Pin 7

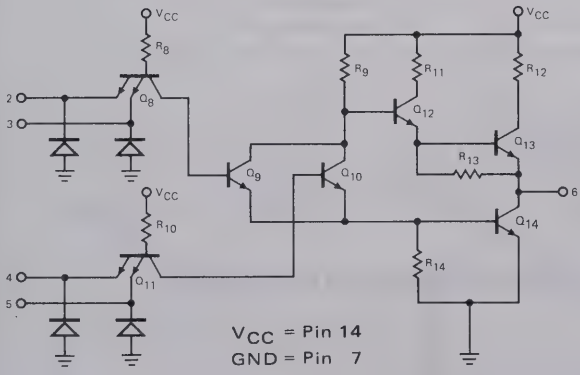
Fig. 1

CIRCUIT DIAGRAMS

9005
EXTENDABLE GATE


VCC
R1
1
13
Q1
VCC
R2
R4
R5
12
Q5
Q6
Q2
Q3
R6
3
VCC
R3
11
Q7
9
Q4
10
R7

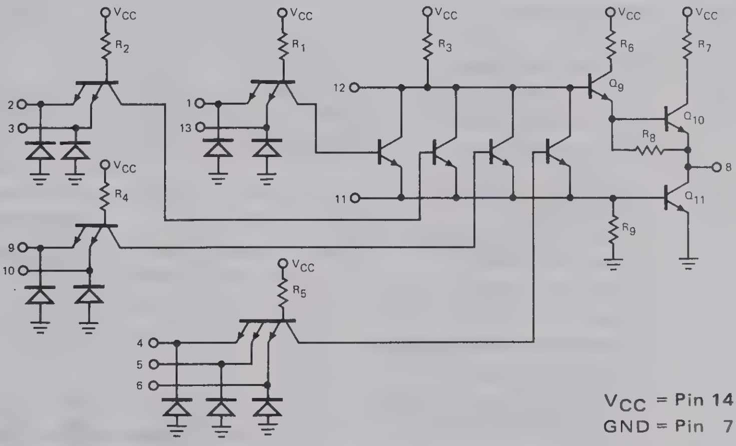
NON-EXTENDABLE GATE


VCC
R8
2
3
Q8
VCC
R9
R11
R12
Q12
Q13
Q9
Q10
R13
6
VCC
R10
Q14
4
Q11
5
R14

V_{CC} = Pin 14
GND = Pin 7

Typical Resistor Values
$R_1 = R_3 = 2.6\ k\Omega$
$R_2 = 800\ \Omega$
$R_4 = R_{11} = 150\ \Omega$
$R_5 = R_{12} = 80\ \Omega$
$R_6 = R_8 = R_{10} = R_{13} \cong 4.0\ k\Omega$
$R_7 = 665\ \Omega$
$R_9 = 1.5\ k\Omega$
$R_{14} = 1.25\ k\Omega$

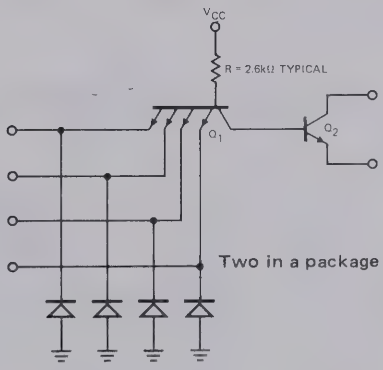
9008


VCC
R2
VCC
R1
VCC
R3
VCC
R6
VCC
R7
2
3
1
13
12
Q9
Q10
R8
8
VCC
R4
11
Q11
R9
9
10
VCC
R5
4
5
6

V_{CC} = Pin 14
GND = Pin 7

Typical Resistor Values
$R_1 = R_2 = R_4 = R_5 = 2.6\ k\Omega$
$R_3 = 800\ \Omega$
$R_6 = 150\ \Omega$
$R_7 = 80\ \Omega$
$R_8 = 4.0\ k\Omega$
$R_9 = 665\ \Omega$

9006


VCC
R = 2.6kΩ TYPICAL
Q1
Q2
Two in a package

V_{CC} = Pin 14
GND = Pin 7

Fig. 2

LOADING FACTORS

9005

PIN NAMES	LOADING
Non-extendable Gate Inputs	1.0 U.L.
Extendable Gate Inputs	1.5 U.L.
All Outputs	10 U.L.

9008

PIN NAMES	LOADING
All Inputs	1.5 U.L.
Outputs	10 U.L.

9006

PIN NAMES	LOADING
All Inputs	1.5 U.L.
Outputs	*

*Outputs on 9006 have open emitter and collector.

(1 U.L. = 40 μA HIGH/1.6 mA LOW)

Fig. 3

ELECTRICAL CHARACTERISTICS 9005XC, 9006XC AND 9008XC (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA V_{IL} = Value indicated on This Table
V_{OL}	Output LOW Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 16.0 mA, V_{IN} = 5.25 V V_{CC} = 4.75 V, I_{OL} = 14.1 mA, Inputs at V_{IL}
I_{IH}	Input HIGH Current 9005 Non-Extendable Gate				5.0	60		60	μA	V_{IN} = 4.5 V V_{CC} = 4.75 V GND on All Other Inputs
	Input HIGH Current Extendable Gates and Extender				7.5	90		90		
I_{IL}	Input LOW Current 9005 Non-Extendable Gate		−1.6		−1.04	−1.6		−1.6	mA	V_{CC} = 5.25 V; V_{IN} = 0.45 V 5.25 V on Other Inputs
			−1.41		−0.79	−1.41		−1.41		V_{CC} = 4.75 V
	Input LOW Current Extendable Gates and Extender		−2.4		−1.56	−2.4		−2.4	mA	V_{CC} = 5.25 V
			−2.12		−1.19	−2.12		−2.12		V_{CC} = 4.75 V
I_{CC}	V_{CC} Current, Gate "ON"								mA	V_{CC} = 5.0 V All Inputs Open
	9005 Non-Extendable Gate		7.7		4.5	7.7		7.7		
	9005 Extendable Gate		13.6		7.6	13.6		13.6		
	9008		17.7		9.3	17.7		17.7		
	V_{CC} Current, Gate "OFF"								mA	V_{CC} = 5.0 V All Inputs Except Extender Inputs GND
	9005 Non-Extendable Gate		3.4		2.2	3.4		3.4		
	9005 Extendable Gate		5.1		3.3	5.1		5.1		
	9008		10.2		6.6	10.2		10.2		
ΔI_{CC}	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "ON"		2.05		1.08	2.05		2.05	mA	V_{CC} = 5.0 V All Inputs HIGH
	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate 'OFF"		2.54		1.65	2.54		2.54	mA	V_{CC} = 5.0 V All Inputs GND

NOTE:
Output characteristics above apply to a 9005 (both gates) or a 9008.
Input characteristics above apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

ELECTRICAL CHARACTERISTICS 9005XM, 9006XM AND 9008XM (T_A = −55°C to 125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.32 mA V_{IL} = Value Indicated on This Table	
V_{OL}	Output LOW Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 17.6 mA, V_{IN} = 5.5 V V_{CC} = 4.5 V, I_{OL} = 13.6 mA, Inputs at V_{IH}	
I_{IH}	Input HIGH Current 9005 Non-extendable Gate				5.0	60		60	µA	V_{CC} = 5.5 V V_{IN} = 4.5 V	GND on All Other Inputs
	Input HIGH Current Extendable Gate and Extender				7.5	90		90			
I_{IL}	Input LOW Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V	V_{IN} = 0.4 V, 5.5 V on Other Inputs
	9005 Non-extendable Gate		−1.24		−0.87	−1.24		−1.24		V_{CC} = 4.5 V	
	Input LOW Current		−2.4		−1.5	−2.4		−2.4	mA	V_{CC} = 5.5 V	
	Extendable Gate and Extender		−1.86		−1.31	−1.86		−1.86		V_{CC} = 4.5 V	
I_{CC}	V_{CC} Current, Gate "ON"								mA	V_{CC} = 5.0 V	All Inputs Open
	9005 Non-extendable Gate		6.5		4.5	6.5		6.5			
	9005 Extendable Gate		11.3		7.6	11.3		11.3			
	9008		12.5		9.3	12.5		12.5			
	V_{CC} Current, Gate "OFF"								mA	V_{CC} = 5.0 V	All Inputs Except Extender Inputs GND
	9005 Non-extendable Gate		3.1		2.1	3.1		3.1			
	9005 Extendable Gate		4.7		3.3	4.7		4.7			
	9008		9.4		6.6	9.4		9.4			
ΔI_{CC}	Extra Current Drain from one 9006 Extender Gate "ON"		1.61		1.08	1.61		1.61	mA	V_{CC} = 5.0 V, All Inputs HIGH 9006 Attached to a 9005	
	Extra Current Drain from one 9006 Extender Gate 'OFF"		2.35		1.65	2.35		2.35	mA	V_{CC} = 5.0 V, All Inputs GND 9006 Attached to a 9005	

NOTE:
Output characteristics apply to a 9005 (both gates) or a 9008.
Input characteristics apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

9005, 9006, 9008
TYPICAL INPUT-OUTPUT CHARACTERISTICS
(EXTENDABLE GATES)

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

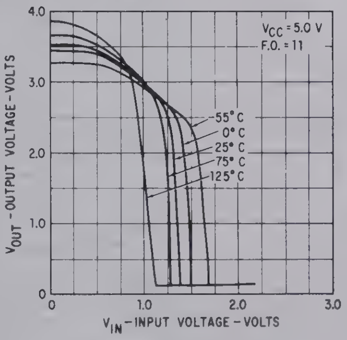


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

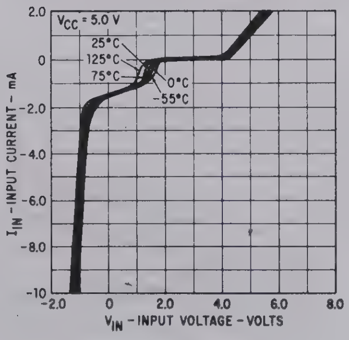


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

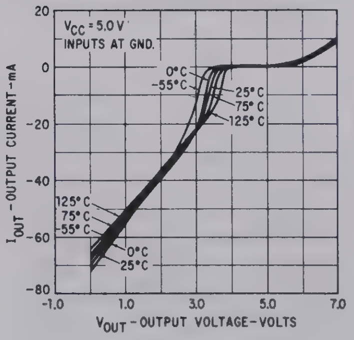


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

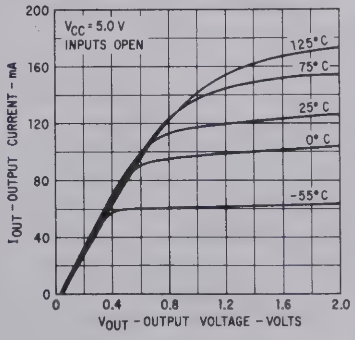
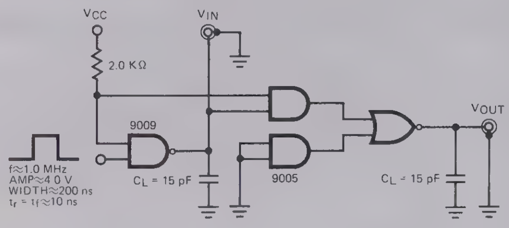


Fig. 7

SWITCHING CHARACTERISTICS

TEST CIRCUITS

9005 NON-EXTENDABLE GATE


VCC
VIN
2.0 KΩ
9009
f≈1.0 MHz
AMP≈4.0 V
WIDTH≈200 ns
tr = tf≈10 ns
CL = 15 pF
9005
CL = 15 pF
VOUT

9005 OR 9008 EXTENDABLE GATE

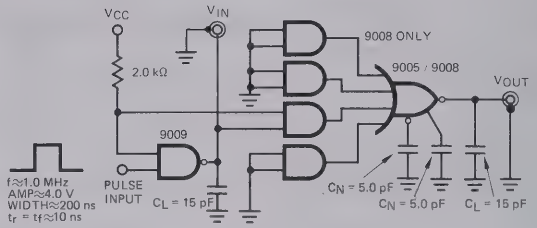
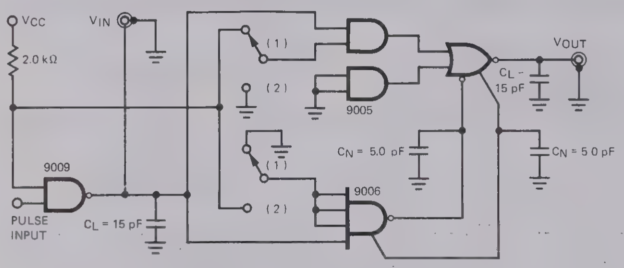

VCC
VIN
2.0 kΩ
9008 ONLY
9005 / 9008
VOUT
9009
f≈1.0 MHz
AMP≈4.0 V
WIDTH≈200 ns
tr = tf≈10 ns
PULSE INPUT
CL = 15 pF
CN = 5.0 pF
CN = 5.0 pF
CL = 15 pF

Fig. 8 Note: Capacitance includes probe and jig capacitance Fig. 9

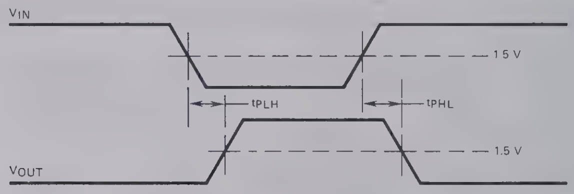
9006 EXTENDER


VCC
VIN
2.0 kΩ
(1)
(2)
9005
VOUT
CL = 15 pF
CN = 5.0 pF
CN = 5.0 pF
(1)
(2)
9006
9009
PULSE INPUT
CL = 15 pF

Note: Capacitance includes probe and jig capacitance

Fig. 10

SWITCHING WAVEFORM


VIN
1.5 V
tPLH
tPHL
VOUT
1.5 V

NOTES:
With switch in position (1) measure delay of 9005. With switch in position (2) measure delay (9005) + Δdelay (9006). Capacitances include probe and jig capacitances.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
t_{PLH}	3.0	12	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	3.0	14		9005 Non-extendable Gate Only, See Figure 8
t_{PLH}	3.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF, C_N = 5.0 pF
t_{PHL}	3.0	12		9005 Extendable Gate and 9008, See Figure 9
Δt_{PLH}	−2.0	4.0	ns	9006 Only
Δt_{PHL}	−2.0	4.0		The 9006 is tested by measuring its propagation time through the 9005. The delay readings shall not exceed the 9005 readings by the specified amount. See Figure 10.

Symbols are defined in the test circuit.

WORST CASE TURN OFF DELAY OF EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

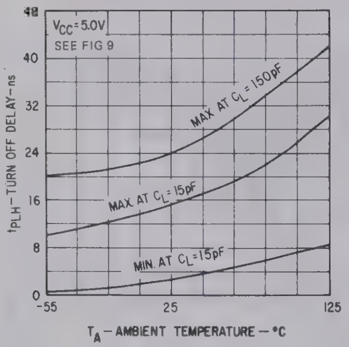


Fig. 11

WORST CASE TURN ON DELAY OF EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

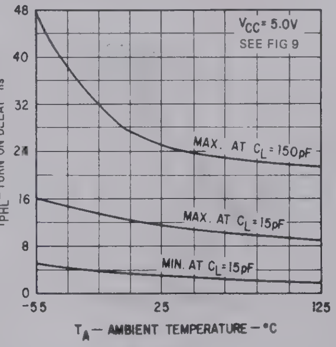


Fig. 12

WORST CASE TURN OFF DELAY OF NON-EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

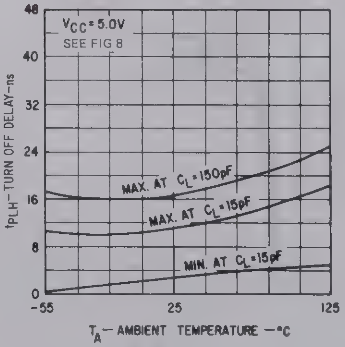


Fig. 13

WORST CASE TURN ON DELAY OF NON-EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE

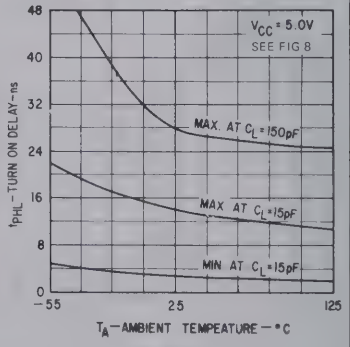
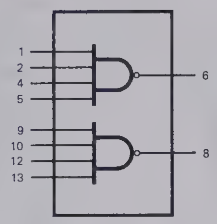


Fig. 14

NAND BUFFER – 9009

The 9009 is a power gate capable of sinking and sourcing large currents for high fan out applications. Logically it is the same as the 9004.

LOGIC DIAGRAM AND PIN CONFIGURATION



V_{CC} = Pin 14
GND = Pin 7

Fig. 1

CIRCUIT DIAGRAM
(One Gate)

Nominal Resistor Values
$R_1 = 2.0\ k\Omega$ $R_4 = 50\ \Omega$
$R_2 = 560\ \Omega$ $R_5 = 4.0\ k\Omega$
$R_3 = 150\ \Omega$ $R_6 = 500\ \Omega$

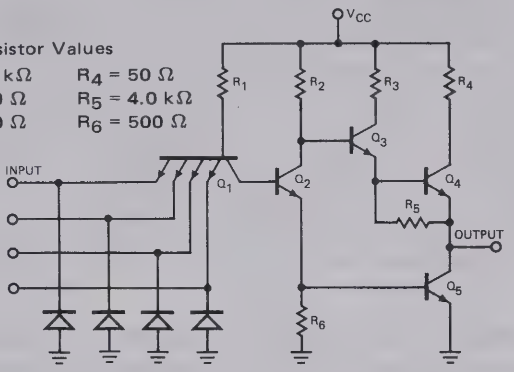


Fig. 2

LOADING FACTORS

PIN NAMES	LOADING
All Inputs	2.0 U.L.
All Outputs	30 U.L. LOW 90 U.L. HIGH

(1 U.L. = 40 μA HIGH/1.6 mA LOW)

Fig. 3

ELECTRICAL CHARACTERISTICS 9009XC (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −3.6 mA, Inputs at V_{IL}	
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 48.0 mA, V_{IN} = 5.25 V	
										V_{CC} = 4.75 V, I_{OL} = 42.3 mA, Inputs at V_{IH}	
I_{IH}	Input HIGH Current				20	120		120	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V GND on Other Inputs	
I_{IL}	Input LOW Current		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.25 V	V_{IN} = 0.45 V 5.25 V on Other Inputs
			−2.82		−1.82	−2.82		−2.82		V_{CC} = 4.75 V	
I_{CC}	V_{CC} Current, Gate On (each gate)		14.6		8.6	14.6		14.6	mA	Inputs HIGH	V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		3.4		2.15	3.4		3.4		Inputs at GND	
t_{PLH}	Turn Off Delay			3.0		17			ns	V_{CC} = 5.0 V, See Figure 12 C_L = 15 pF	
t_{PHL}	Turn On Delay			2.0		13			ns		

ELECTRICAL CHARACTERISTICS 9009XM (T_A = −55°C to 125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −3.96 mA, Inputs at V_{IL}	
V_{OL}	Output LOW Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 52.8 mA, V_{IN} = 5.5 V	
										V_{CC} = 4.5 V, I_{OL} = 40.8 mA, Inputs at V_{IH}	
I_{IH}	Input HIGH Current				20	120		120	μA	V_{CC} = 5.5 V, V_{IN} = 4.5V GND on Other Inputs	
I_{IL}	Input LOW Current		−3.2		−2.2	−3.2		−3.2	mA	V_{CC} = 5.5 V	V_{IN} = 0.4 V 5.5 V on Other Inputs
			−2.48		−1.74	−2.48		−2.48		V_{CC} = 4.5 V	
I_{CC}	V_{CC} Current, Gate On (each gate)		12.9		8.6	12.9		12.9	mA	Inputs HIGH	V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		3.2		2.15	3.2		3.2		Inputs at GND	
t_{PLH}	Turn Off Delay			4.0		15			ns	V_{CC} = 5.0 V, See Figure 12	
t_{PHL}	Turn On Delay			3.0		10			ns	C_L = 15 pF	

9009
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

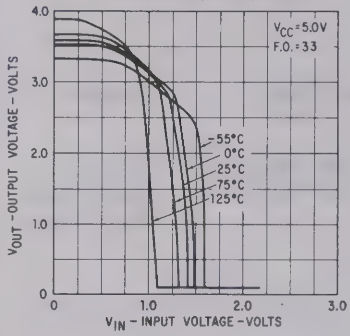


Fig. 4

INPUT CURRENT VERSUS INPUT VOLTAGE

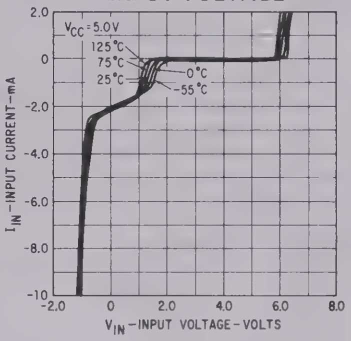


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

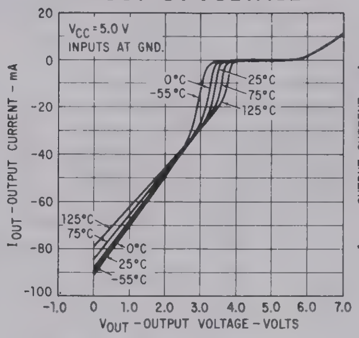


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

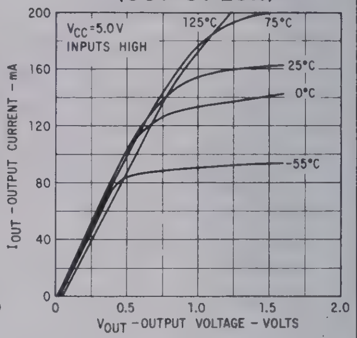


Fig. 7

POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

POWER DISSIPATION VERSUS SUPPLY VOLTAGE

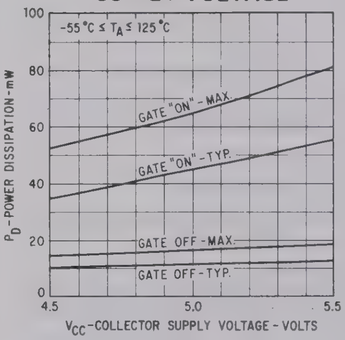


Fig. 8

WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

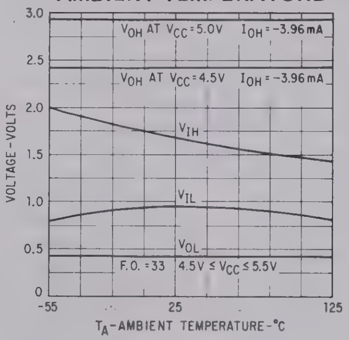


Fig. 9

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

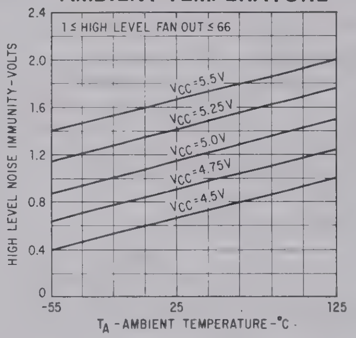


Fig. 10

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

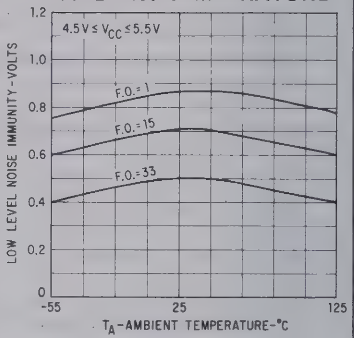
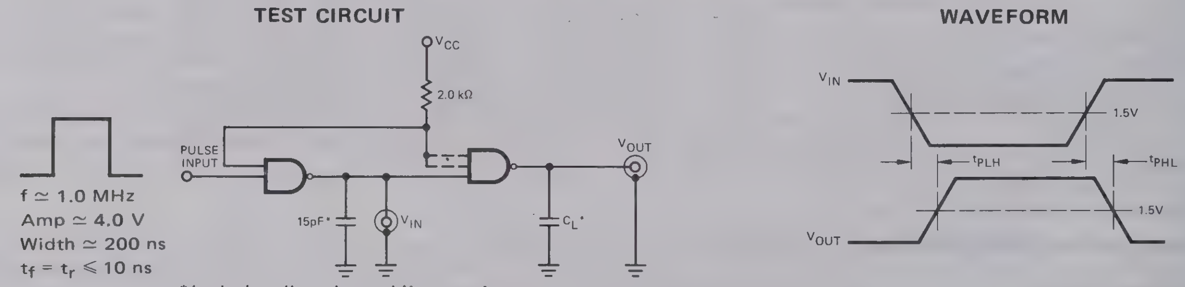


Fig. 11

SWITCHING CHARACTERISTICS



f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_f = t_r \leqslant 10$ ns

*Includes all probe and jig capacitance

Fig. 12

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

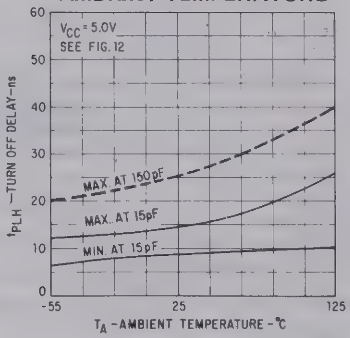


Fig. 13

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

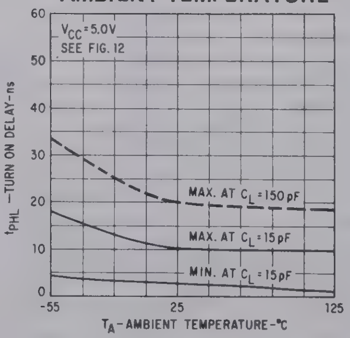
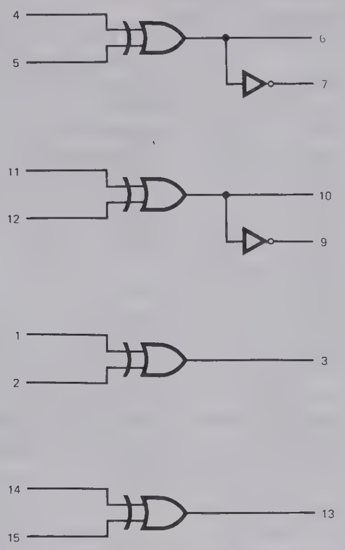


Fig. 14

QUAD EXCLUSIVE OR GATE – 9014

The 9014 consists of four exclusive OR gates, useful in a large number of code conversion, parity generation/checking, and comparison applications. Two of the gates have an additional complemented output for greater system flexibility. The 9014 has high speed, high fanout capabilities and is compatible with all members of the Fairchild TTL family.

LOGIC DIAGRAM


4
5
6
7
11
12
10
9
1
2
3
14
15
13

V_{CC} = PIN 16
GND = PIN 8

Fig. 1

CIRCUIT DIAGRAM

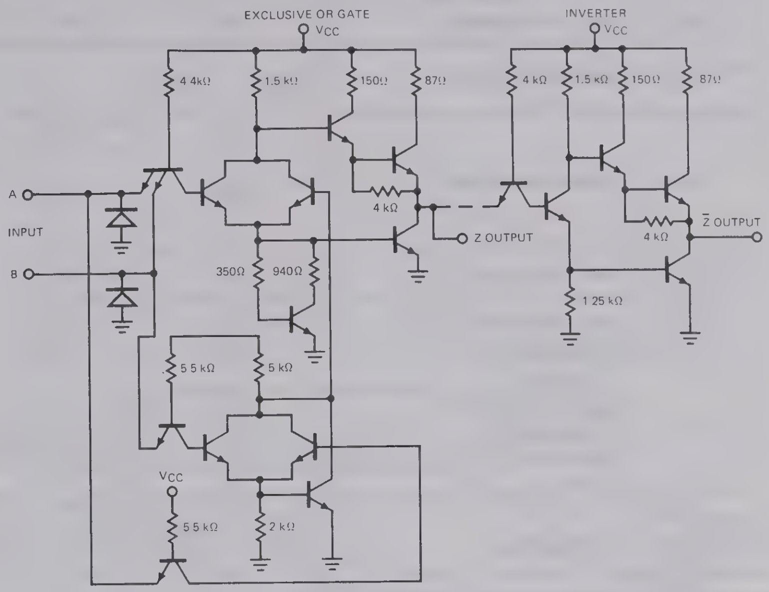

EXCLUSIVE OR GATE
VCC
4.4kΩ
1.5 kΩ
150Ω
87Ω
4 kΩ
A
INPUT
B
350Ω
940Ω
5.5 kΩ
5 kΩ
VCC
5.5 kΩ
2 kΩ
Z OUTPUT
INVERTER
VCC
4 kΩ
1.5 kΩ
150Ω
87Ω
4 kΩ
Z̄ OUTPUT
1.25 kΩ

Fig. 2

LOADING FACTORS

PIN NAMES	LOADING (Note a)
All Inputs	1.5 U.L.
Outputs	
3, 7, 9, 13 (Note b)	10 U.L.
6, 10 (Note c)	9 U.L.

NOTES:

a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.
c. 9 U.L. is the output LOW drive factor and 19 U.L. is the output HIGH drive factor.

Fig. 3

FUNCTIONAL DESCRIPTION – The exclusive OR gate produces an output when the inputs are complementary. Two gates have an additional inverted output which provides directly a compare capability. The Boolean expessions for the gates are: $Z = A\overline{B} + \overline{A}B$; $\overline{Z} = AB + \overline{AB}$.

TRUTH TABLE

A	B	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

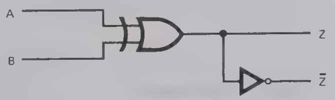
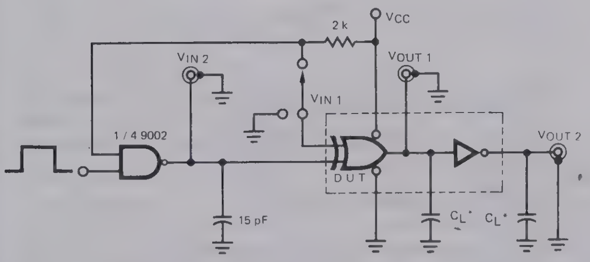


Fig. 4

SWITCHING TEST CIRCUIT


VCC
2 k
VIN 2
VOUT 1
VIN 1
1/4 9002
DUT
VOUT 2
15 pF
CL*
CL*

f ≃ 1 MHz
Amp. ≃ 4.0 V
Pulse Width = 200 ± 20 ns
$t_r = t_f \leqslant 10$ ns

Fig. 5

*C_L includes probe and jig capacity

WAVEFORMS

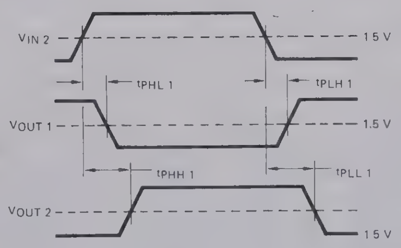

VIN 2
1.5 V
tPHL 1
tPLH 1
VOUT 1
1.5 V
tPHH 1
tPLL 1
VOUT 2
1.5 V

Fig. 6

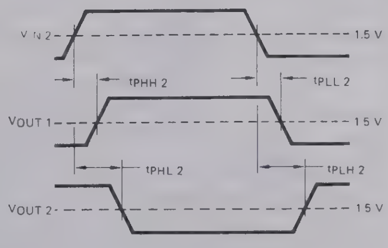

VIN 2
1.5 V
tPHH 2
tPLL 2
VOUT 1
1.5 V
tPHL 2
tPLH 2
VOUT 2
1.5 V

Fig. 7

ELECTRICAL CHARACTERISTICS 9014XC (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	3.1		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.20 mA I_{OH} = −1.14 mA (Pins 6 & 10) Inputs at V_{IL} & V_{IH} per Truth Table
V_{OL}	Output LOW Voltage		0.45		0.29	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 16.0 mA I_{OL} = 14.4 mA (Pins 6 & 10) Inputs = 5.25 V or 0 V per Truth Table
			0.45			0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA I_{OL} = 12.7 mA (Pins 6 & 10) Inputs = 5.25 V or 0 V per Truth Table
I_{IH}	Input HIGH Current				15	90		90	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V Other Inputs = GND
I_{IL}	Input LOW Current		−2.4		−1.54	−2.4		−2.4	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
			−2.1			−2.1		−2.1	mA	V_{CC} = 4.75 V, Other Inputs = 5.25 V
I_{CC}	V_{CC} Current, Gate On (each gate)		4.5		3.15	4.5		4.5	mA	V_{CC} = 5.0 V, One Input = 5.5 V, One Input = GND
	V_{CC} Current, Gate Off (each gate)		8.7		6.06	8.7		8.7	mA	V_{CC} = 5.0 V, Inputs = GND
			7.6		5.38	7.6		7.6	mA	V_{CC} = 5.0 V, Inputs = 5.5 V
	V_{CC} Current Per Inverter On		6.1		3.6	6.1		6.1	mA	V_{CC} = 5.0 V, Input Node HIGH
	V_{CC} Current Per Inverter Off		1.7		1.07	1.7		1.7	mA	V_{CC} = 5.0 V, Input Node LOW
t_{PLH} 1	Switching Tests			3.0	8.0	13			ns	V_{CC} = 5.0 V, V_{IN1} = 5.0 V C_L = 15 pF See Figures 5 & 6 on previous page
t_{PHL} 1				3.0	11	15			ns	
t_{PHH} 1				6.0	16	28			ns	
t_{PLL} 1				6.0	16	28			ns	
t_{PHH} 2	Switching Tests			7.0	11	17			ns	V_{CC} = 5.0 V, V_{IN1} = 0 V C_L = 15 pF See Figures 5 & 7 on previous page
t_{PLL} 2				7.0	15	19			ns	
t_{PLH} 2				10	21	32			ns	
t_{PHL} 2				10	20	32			ns	

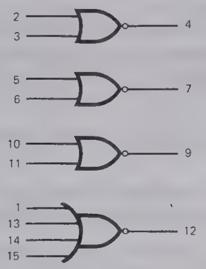
ELECTRICAL CHARACTERISTICS 9014XM (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	125°C MIN.	125°C MAX.	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.32 mA I_{OH} = −1.20 mA (Pins 6 & 10) Inputs at V_{IL} & V_{IH} per Truth Table
V_{OL}	Output LOW Voltage		0.4		0.27	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 17.6 mA I_{OL} = 16 mA (Pins 6 & 10) Inputs = 5.5 V or 0 V per Truth Table
			0.4			0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 13.6 mA I_{OL} = 12.4 mA (Pins 6 & 10) Inputs = 5.5 V or 0 V per Truth Table
I_{IH}	Input HIGH Current				10	90		90	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V Other Inputs = GND
I_{IL}	Input LOW Current		−2.4		−1.65	−2.4		−2.4	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
			−1.86			−1.86		−1.86	mA	V_{CC} = 4.5 V, Other Inputs = 5.5 V
I_{CC}	V_{CC} Current, Gate On (each gate)		4.2		3.15	4.2		4.2	mA	V_{CC} = 5.0 V, One Input = 5.5 V One Input = GND
	V_{CC} Current, Gate Off (each gate)		8.1		6.06	8.1		8.1	mA	V_{CC} = 5.0 V, Inputs = GND
			7.2		5.38	7.2		7.2	mA	V_{CC} = 5.0 V, Inputs = 5.5 V
	V_{CC} Current Per Inverter On		5.5		3.5	5.5		5.5	mA	V_{CC} = 5.0 V, Input Node HIGH
	V_{CC} Current Per Inverter Off		1.6		1.07	1.6		1.6	mA	V_{CC} = 5.0 V, Input Node LOW
t_{PLH} 1	Switching Tests			3.0	7.0	10			ns	V_{CC} = 5.0 V, V_{IN1} = 5.0 V C_L = 15 pF See Figures 5 & 6 on previous page
t_{PHL} 1				3.0	8.0	12			ns	
t_{PHH} 1				6.0	14	22			ns	
t_{PLL} 1				6.0	14	22			ns	
t_{PHH} 2	Switching Tests			7.0	10	14			ns	V_{CC} = 5.0 V, V_{IN1} = 0 V C_L = 15 pF See Figures 5 & 7 on previous page
t_{PLL} 2				7.0	12	16			ns	
t_{PLH} 2				10	18	26			ns	
t_{PHL} 2				10	17	26			ns	

QUAD NOR GATE – 9015

The TTL 9015 consists of three 2-input and one 4-input NOR gates. The NOR gate produces a LOW output if any of the inputs are HIGH.

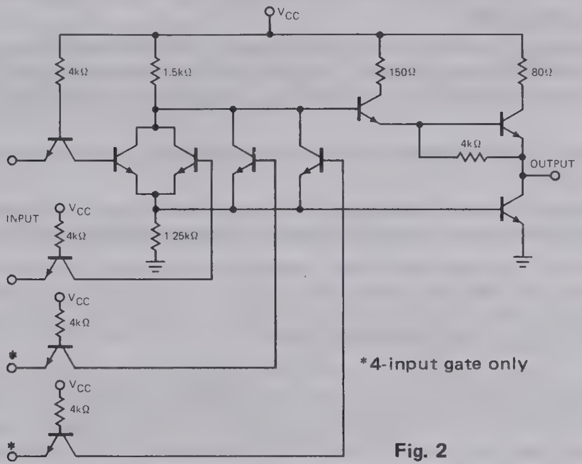
LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

Fig. 1

CIRCUIT DIAGRAM



*4-input gate only

Fig. 2

LOADING FACTORS

PIN NAMES	LOADING
All Inputs	1 U.L.
All Outputs	10 U.L.

(1 U.L. = 40 µA HIGH/1.6 mA LOW)

Fig. 3

SWITCHING WAVEFORMS

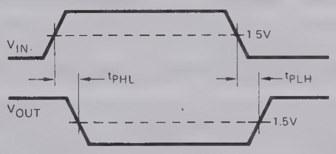


Fig. 4

ELECTRICAL CHARACTERISTICS 9015XC (0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA, Inputs = V_{IL}	
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 16.0 mA, Inputs = 5.25 V	
			0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA, Inputs = V_{IH}	
I_{IH}	Input HIGH Current				10	60		60	µA	V_{CC} = 5.25 V, GND on Other Inputs	
I_{IL}	Input LOW Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V	V_{IN} = 0.45 V
			−1.41		−0.91	−1.41		−1.41		V_{CC} = 4.75 V	5.25 V on Other Inputs
I_{CC}	V_{CC} Current, Gate On (each gate)		6.55		4.25	6.55		6.55	mA	Inputs HIGH	V_{CC} = 5.0 V
			8.75		5.7	8.75		8.75		Inputs HIGH (4-Input Gate Only)	
	V_{CC} Current, Gate Off (each gate)		3.38		2.2	3.38		3.38		Inputs LOW	
			6.77		4.4	6.77		6.77		Inputs LOW (4-Input Gate Only)	
t_{PLH}	Turn Off Delay			3.0	7.0	13			ns	V_{CC} = 5.0 V, C_L = 15 pF	
t_{PHL}	Turn On Delay			3.0	9.0	15			ns	(See Figure 4)	

ELECTRICAL CHARACTERISTICS 9015XM (−55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.32 mA, Inputs = V_{IL}	
V_{OL}	Output LOW Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V, Inputs = 5.5 V, I_{OL} = 17.6 mA	
			0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5 V, V_{IN} = V_{IH}, I_{OL} = 13.6 mA	
I_{IH}	Input HIGH Current				10	60		60	µA	V_{CC} = 5.5 V, V_{IN} = 4.5 V GND on Other Inputs	
I_{IL}	Input LOW Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V	V_{IN} = 0.4 V
			−1.24		−0.87	−1.24		−1.24		V_{CC} = 4.5 V	5.5 V on Other Inputs
I_{CC}	V_{CC} Current, Gate On (each gate)		6.07		4.25	6.07		6.07	mA	Inputs HIGH	V_{CC} = 5.0 V
			8.14		5.7	8.14		8.14		Inputs HIGH (4-Input Gate Only)	
	V_{CC} Current, Gate Off (each gate)		3.2		2.2	3.2		3.2		Inputs LOW	
			6.4		4.4	6.4		6.4		Inputs LOW (4-Input Gate Only)	
t_{PLH}	Turn Off Delay			3.0	6.0	10			ns	V_{CC} = 5.0 V, C_L = 15 pF	
t_{PHL}	Turn On Delay			3.0	8.0	12			ns	(See Figure 4)	

JK FLIP-FLOPS – 9000, 9001
DUAL JK FLIP-FLOPS – 9020, 9022

DESCRIPTION – The TTL 9000 series has four flip-flops to satisfy the storage requirements of a logic system. All are master/slave JK designs and have the same high speed and high noise immunity as the rest of the 9000 series. As with the gates, all inputs have diode clamps to reduce ringing caused by long lines and impedance mismatches.

The JK type flip-flop was chosen for all flip-flop elements in this family because of its inherent logic power. The input function required to produce a given sequence of states for a JK flip-flop will, in general, contain more "don't care" conditions than the corresponding function for an RS flip-flop. These additional "don't care" conditions will, in most cases, reduce the amount of gating elements required to implement the input function.

The master/slave design offers the advantage of a dc threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

Data is accepted by the master while the clock is in the LOW state. Refer to the truth table for definition of HIGH and LOW data. Transfer from the master to the slave occurs on the LOW to HIGH transition of the clock. When the clock is HIGH, the J and K inputs are inhibited.

A joint (JK) input is provided for all flip-flops in this family. This common input removes the necessity of gating the clock signal with an external gate in many applications. This not only reduces package count, but also reduces the possibility of clock skew problems, since with internal gating provided, all flip-flops may be driven from a common clock line. Several TTL drivers may be used in parallel to drive this common clock line if the load exceeds the F.O. capability of the 9009 buffer.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided on all flip-flops except the 9020, which because of a logic trade-off has only clear inputs. The set or clear pin being LOW absolutely guarantees that one output will be HIGH, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the LOW output may momentarily spike HIGH synchronous with a positive transition of the clock. If the LOW output of the flip-flop is connected to other flip-flop inputs clocked from the same line, the spike will be masked by the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur. When the spikes can cause problems, a simple solution is to common the joint JK inputs with the synchronous set or reset signal.

LOGIC DIAGRAMS

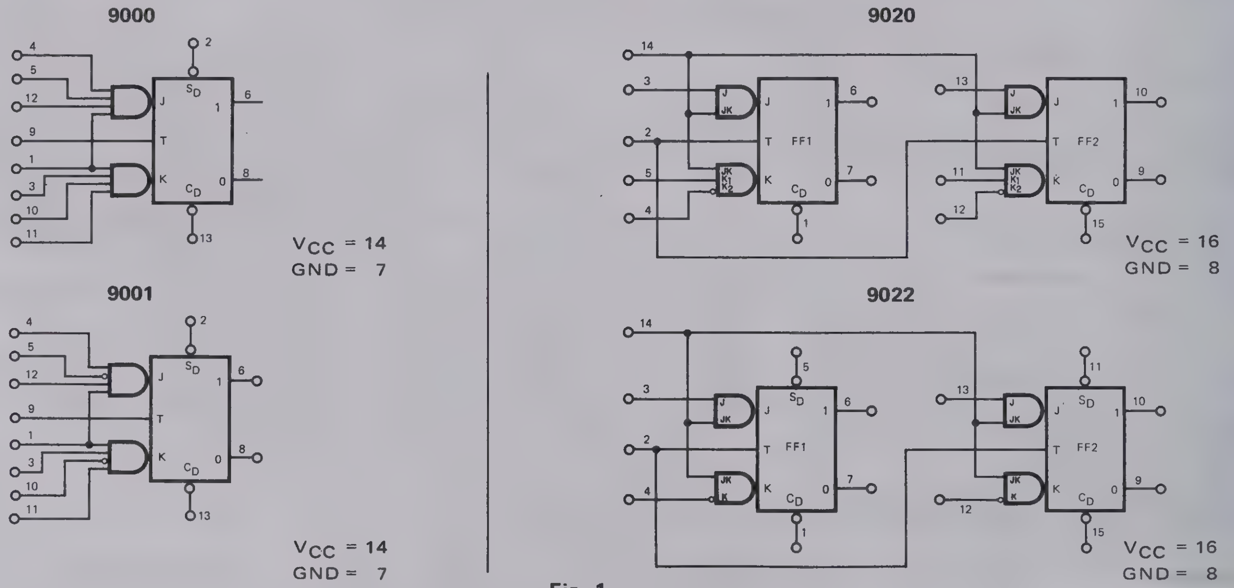


Fig. 1

FUNCTIONAL LOGIC DIAGRAMS

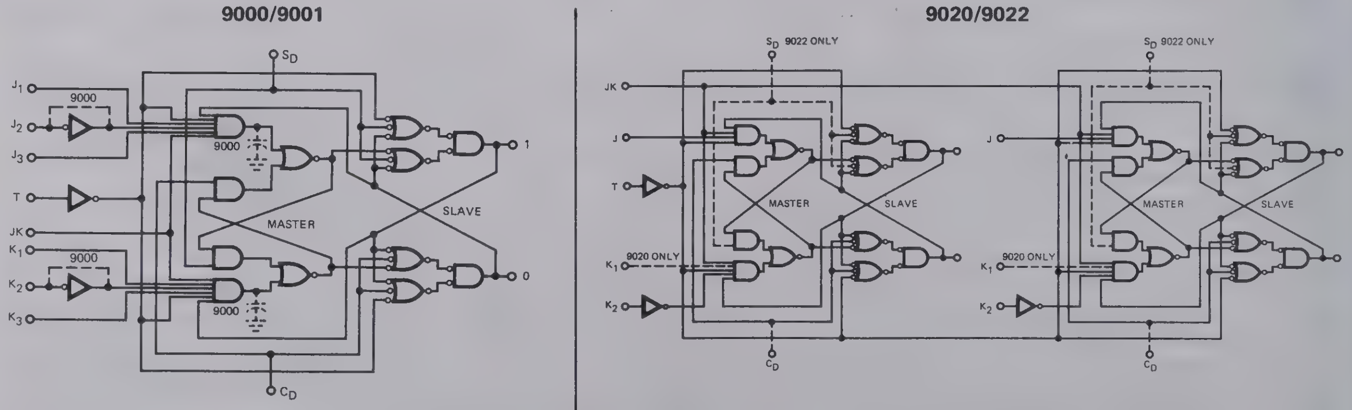


Fig. 2

TRUTH TABLES

SYNCHRONOUS OPERATION

BEFORE CLOCK				AFTER CLOCK	
OUTPUTS		INPUTS		OUTPUTS	
ONE	ZERO	J	K	ONE	ZERO
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
S_D	C_D	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	SYNCHRONOUS INPUTS CONTROL	

SYNCHRONOUS OPERATION — The truth table defines the next state of the flip-flop after a LOW to HIGH transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table.

The J and K inputs in the table refer to the basic flip-flop J and K inputs as indicated on the logic diagrams. These internal inputs are for every flip-flop the result of a logic operation on the external J and K inputs. This operation is represented symbolically by AND gates in the logic diagram for each flip-flop. Logic diagrams are in accordance with MIL Standard 806B.

The L* symbol in the J and K input column is defined as meaning that **input does not go HIGH at any time while the clock is LOW.**

The H* symbol in the J or K input column is defined as meaning that the **input is HIGH at some time while the clock is LOW.**

The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state HIGH and LOW voltage levels, respectively.

UNUSED INPUTS — The 9001, 9020 and 9022 all have active level LOW synchronous inputs. When not in use they must be grounded. All other unused inputs, including asynchronous, should be tied HIGH for maximum operating speed.

ELECTRICAL CHARACTERISTICS 9000XC, 9001XC, 9020XC AND 9022XC (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	PARAMETER	LIMITS							UNITS	TEST CONDITIONS	
		0°C		25°C			75°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA	
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16 mA	
I_{IH}	Input HIGH Current All J, K Inputs T Inputs 9000, 9001				5.0	60		60	µA	V_{CC} = 5.25 V, V_{IN} = 4.5 V GND on Other Inputs	
	JK Inputs 9000, 9001 T Inputs 9020, 9022				10	120		120			
	JK Inputs 9020, 9022				20	240		240			
	S_D, C_D (all Flip-Flops)				14	160		160			
I_{IL}	Input LOW Current All J, K Inputs T Inputs 9000, 9001		−1.60		−1.0	−1.60		−1.60	mA	V_{CC} = 5.25 V	V_{IN} = 0.45 V 5.25 V on Other Inputs
	JK Inputs 9000, 9001 T Inputs 9020, 9022		−3.20		−2.0	−3.20		−3.20			
	JK Inputs 9020, 9022		−6.40		−4.0	−6.40		−6.40			
	S_D, C_D (all Flip-Flops)		−4.32		−2.7	−4.32		−4.32			
	Input LOW Current All J, K Inputs T Inputs 9000, 9001		−1.41		−0.94	−1.41		−1.41	mA	V_{CC} = 4.75 V	
	JK Inputs 9000, 9001 T Inputs 9020, 9022		−2.82		−1.88	−2.82		−2.82			
	JK Inputs 9020, 9022		−5.64		−3.76	−5.64		−5.64			
	S_D C_D (all Flip-Flops)		−3.78		−2.54	−3.78		−3.78			
I_{CC}	V_{CC} Current 9000		28			28		28	mA	S_D at GND	V_{CC} = 5.0 V
	9001		33			33		33		S_D at GND	
	9020, 9022 each Flip-Flop		30			30		30		C_{D1}, C_{D2} at GND	

LOADING FACTORS

9000

PIN NAMES	LOADING (Note a)
JK	2 U.L.
$J_1, J_2, J_3, K_1, K_2, K_3$, T	1 U.L.
S_D, C_D	3 U.L.
Outputs (Note b)	10 U.L.

9001

PIN NAMES	LOADING (Note a)
JK	2 U.L.
$J_1, J_2, J_3, K_1, K_2, K_3$, T	1 U.L.
S_D, C_D	3 U.L.
Outputs (Note b)	10 U.L.

9020

PIN NAMES	LOADING (Note a)
JK	4 U.L.
J, K_1, K_2	1 U.L.
T	2 U.L.
C_D	3 U.L.
Outputs (Note b)	10 U.L.

9022

PIN NAMES	LOADING (Note a)
JK	4 U.L.
J, K	1 U.L.
T	2 U.L.
C_D	3 U.L.
Outputs (Note b)	10 U.L.

NOTES:

a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW; the HIGH load factor of 40 μA measured at 2.4 V is considered equivalent to 60 μA measured at 4.5 V for purposes of system loading calculations.

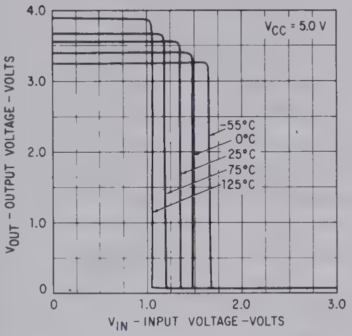
b. 10 U.L. is the LOW drive factor and 30 U.L. is the HIGH drive factor.

Fig. 3

ELECTRICAL CHARACTERISTICS 9000XM, 9001XM, 9020XM AND 9022XM (T_A = −55°C to 125°C, V_{CC} = 5.0 V ±10%)

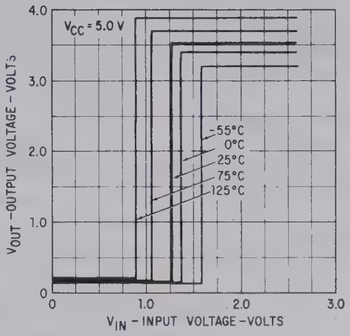
SYMBOL	PARAMETER	LIMITS							UNITS	TEST CONDITIONS	
		−55°C		25°C			125°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.2 mA	
V_{OL}	Output LOW Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 12.4 mA V_{CC} = 5.5 V, I_{OL} = 16.0 mA	
I_{IH}	Input HIGH Current All J, K Inputs T Inputs 9000, 9001				5.0	60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V GND on Other Inputs	
	JK Inputs 9000, 9001 T Inputs 9020, 9022				10	120		120			
	JK Inputs 9020, 9022				20	240		240			
	S_D, C_D (all Flip-Flops)				14	160		160			
I_{IL}	Input LOW Current All J, K Inputs T Inputs 9000, 9001		−1.60		−1.1	−1.60		−1.60	mA	V_{CC} = 5.5 V	V_{IN} = 0.4 V 5.5 V GND on Other Inputs
	JK Inputs 9000, 9001 T Inputs 9020, 9022		−3.20		−2.2	−3.20		−3.20			
	JK Inputs 9020, 9022		−6.40		−4.4	−6.40		−6.40			
	S_D, C_D (all Flip-Flops)		−4.32		−2.97	−4.32		−4.32			
	Input LOW Current All J, K Inputs T Inputs 9000, 9001		−1.24		−0.87	−1.24		−1.24	mA	V_{CC} = 4.5 V	
	JK Inputs 9000, 9001 T Inputs 9020, 9022		−2.48		−1.74	−2.48		−2.48			
	JK Inputs 9020, 9022		−4.96		−3.48	−4.96		−4.96			
	S_D, C_D (all Flip-Flops)		−3.35		−2.35	−3.75		−3.35			
I_{CC}	V_{CC} Current 9000		24		13	24		24	mA	S_D at GND	V_{CC} = 5.0 V
	9001		28		14	28		28		S_D at GND	
	9020, 9022 each Flip-Flop		27		14	27		27		C_{D1}, C_{D2}, at GND	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9000, 9001, 9020 AND 9022



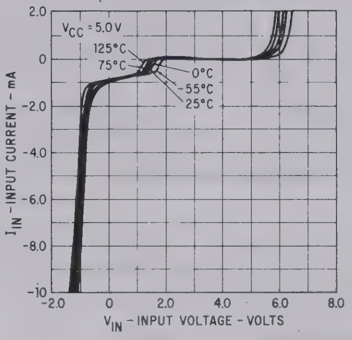
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS

Fig. 4



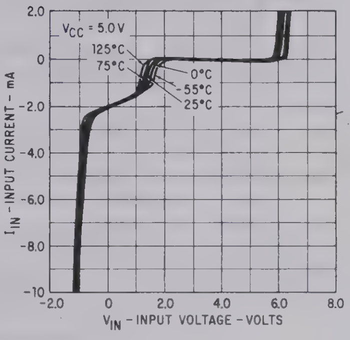
CLOCK OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

Fig. 5



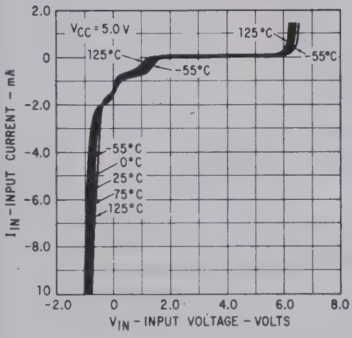
INPUT CURRENT VERSUS INPUT VOLTAGE 9004

Fig. 6



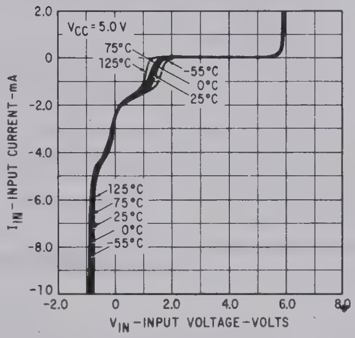
INPUT CURRENT VERSUS INPUT VOLTAGE 9009

Fig. 7



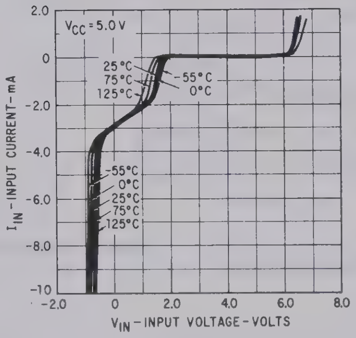
INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9000, 9001

Fig. 8



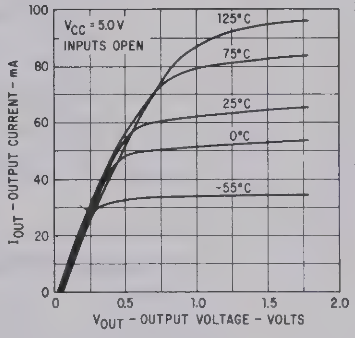
INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9020, 9022

Fig. 9



INPUT CURRENT VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS – ALL FLIP-FLOPS

Fig. 10



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

Fig. 11

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = C_1 = 15$ pF of all flip-flops unless otherwise noted)

SYMBOL	PARAMETER			LIMITS			UNITS	FIGURES
				MIN.	TYP.	MAX.		
t_{PLH}	Clock to Output				12	20	ns	17, 18, 19
	S_D or C_D to Output				12	20	ns	17, 18, 19
t_{PHL}	Clock to Output				20	30	ns	17, 18, 19
	S_D or C_D to Output				25	35	ns	17, 18, 19
$t_{set\text{-}up}$	J, K or JK	9000XM		30	22		ns	17, 19
		9000XC		35	22			
		9001XM, 9020XM, 9022XM		10	8		ns	17, 18, 19
		9001XC, 9020XC, 9022XC		15	8			
	$\overline{J}$ or $\overline{K}$ Data Entry			17	12			
$t_{release}$	J, K or JK	9000 only			18	10	ns	17, 19
		9001, 9020, 9022			7	1.0	ns	17, 18, 19
	$\overline{J}$ or $\overline{K}$ Data Entry				11	4.0		
Pulse Widths	Clock	9000 only	Positive		20		ns	17, 19
			Negative		25		ns	17, 19
		9001, 9020, 9022	Positive		8.0		ns	17, 18, 19
			Negative		10		ns	17, 18, 19
	S_D or C_D		Negative		25		ns	17, 18, 19
Toggle Frequency			9000 only		20		MHz	17, 19
			9001, 9020, 9022		50		MHz	17, 18, 19

MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE T TO OUTPUT

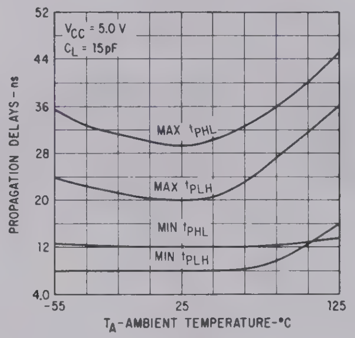


Fig. 12

MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE ASYNCHRONOUS INPUTS TO OUTPUTS

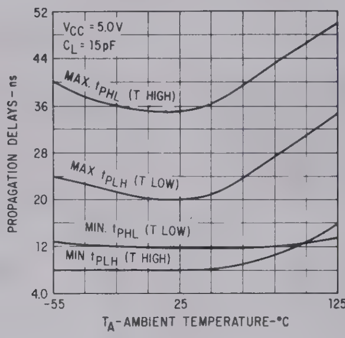


Fig. 13

INCREASE IN ASYNCHRONOUS OR CLOCK INPUT DUE TO OUTPUT CAPACITANCE

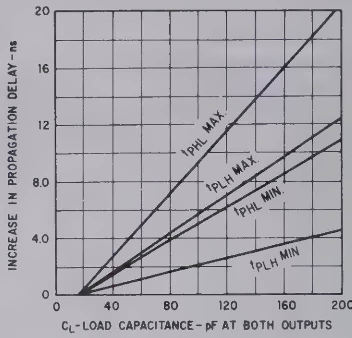


Fig. 14

9001 – 9020 – 9022 SET-UP/RELEASE TIME AND NEGATIVE CLOCK PULSE WIDTH VERSUS AMBIENT TEMPERATURE

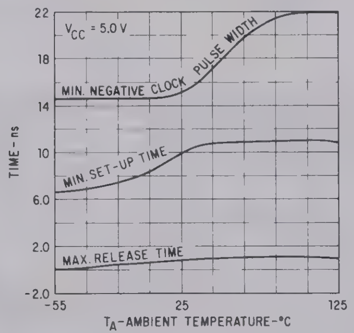


Fig. 15

9000 NEGATIVE CLOCK PULSE WIDTH SET-UP/RELEASE TIME VERSUS AMBIENT TEMPERATURE

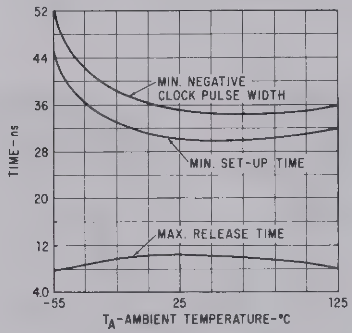
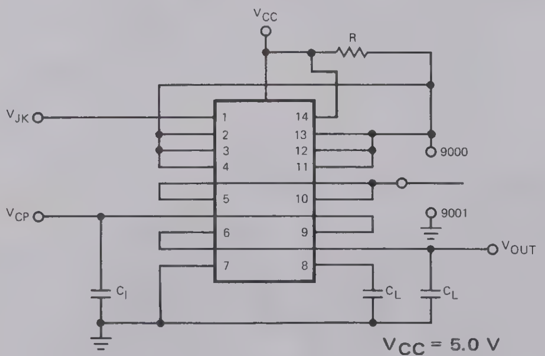


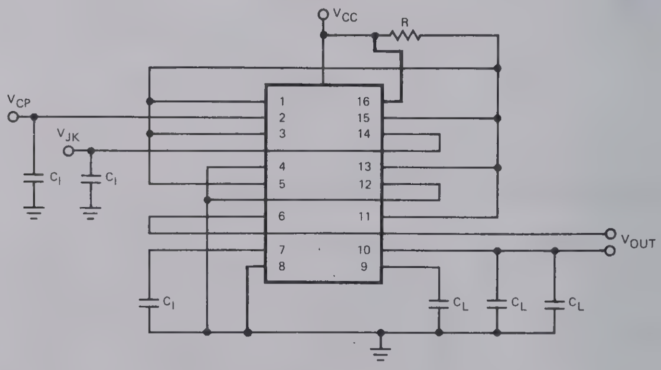
Fig. 16

SWITCHING TEST CIRCUITS

9000/9001


V_{CC}
R
V_{JK}
V_{CP}
1
2
3
4
5
6
7
14
13
12
11
10
9
8
9000
9001
V_{OUT}
C_I
C_L
C_L

9020/9022


V_{CC}
R
V_{CP}
V_{JK}
C_I
C_I
C_I
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V_{OUT}
C_L
C_L
C_L

V_{CC} = 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

Fig. 17

Fig. 18

WAVEFORMS

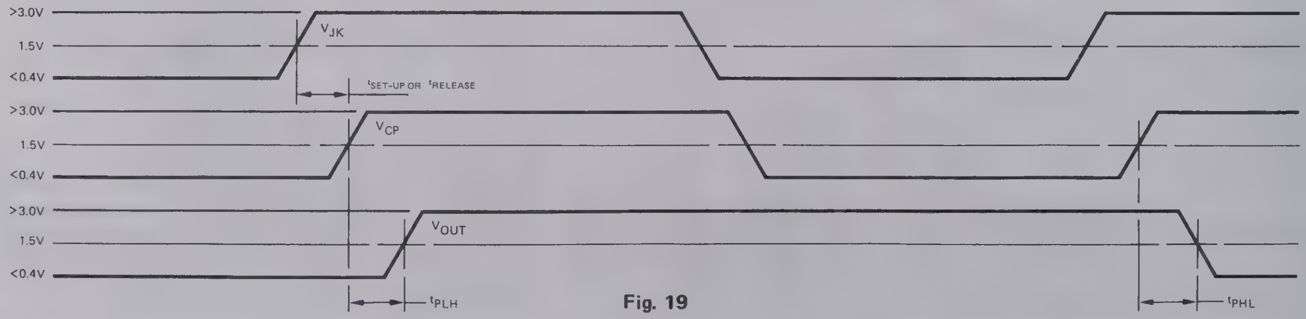

>3.0V
1.5V
<0.4V
V_{JK}
t_{SET-UP} OR $t_{RELEASE}$
>3.0V
1.5V
<0.4V
V_{CP}
>3.0V
1.5V
<0.4V
V_{OUT}
t_{PLH}
t_{PHL}

Fig. 19

SWITCHING TEST NOTES

t_{PLH} and t_{PHL}

1. V_{JK} should be kept at the HIGH logic level when performing t_{PLH}/t_{PHL} tests.
2. Drive the clock pulse input with a suitable pulse source. t_{PLH} and t_{PHL} delays are as defined in the waveforms.

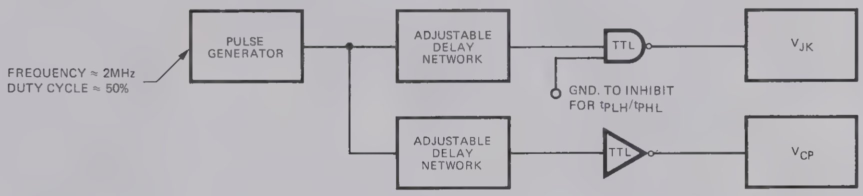
$t_{set\text{-}up}$

1. $t_{set\text{-}up}$ is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the LOW state of the clock in order for the flip-flop to respond to the data.
2. The test for $t_{set\text{-}up}$ is performed by adjusting the timing relationship between the V_{CP} and V_{JK} inputs to the $t_{set\text{-}up}$ minimum value. A device that passes the test will have the output waveform shown. The output of a device that does not pass the $t_{set\text{-}up}$ test will remain at a static logic level (no switching will occur).

$t_{release}$

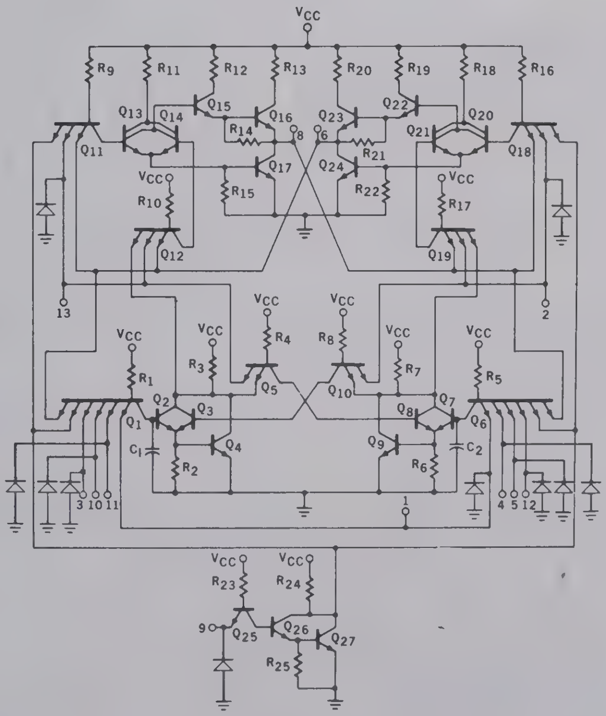
1. $t_{release}$ is defined as the maximum time allowed for a HIGH to be present at a synchronous logic input at any time during the LOW state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

RECOMMENDED INPUT PULSE SOURCES

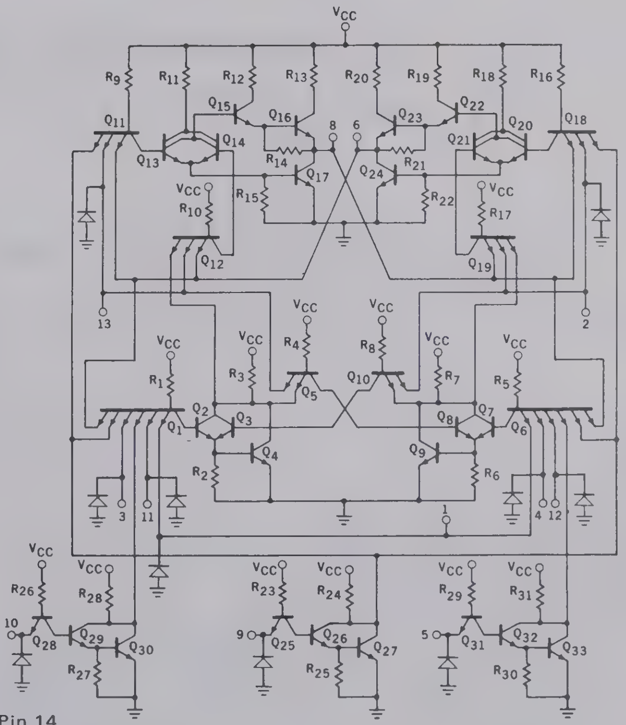

FREQUENCY ≈ 2MHz
DUTY CYCLE ≈ 50%
PULSE GENERATOR
ADJUSTABLE DELAY NETWORK
TTL
GND. TO INHIBIT FOR t_{PLH}/t_{PHL}
V_{JK}
ADJUSTABLE DELAY NETWORK
TTL
V_{CP}

DTL9932 gates with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

9000 SCHEMATIC DIAGRAM

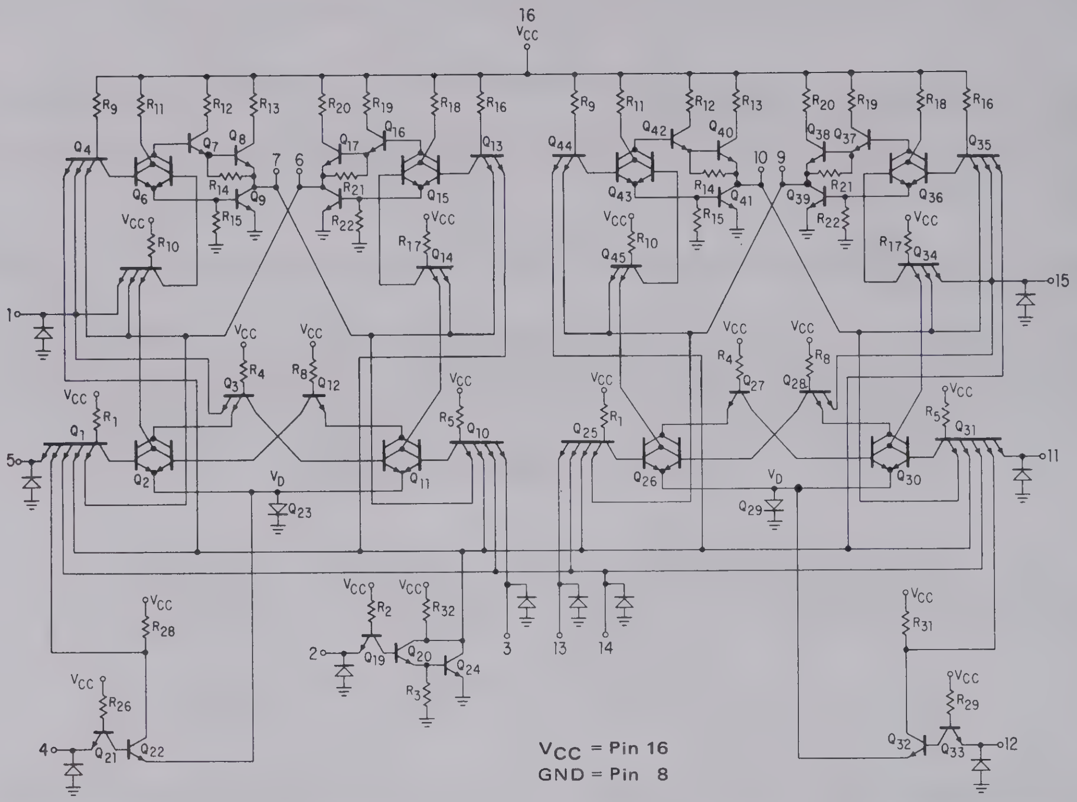

V_{CC}
R9 R11 R12 R13 R20 R19 R18 R16
Q13 Q14 Q15 Q16 Q23 Q22 Q20 Q21
Q11 R14 8 6 R21 Q18
Q17 Q24
R10 R15 R22 R17
Q12 Q19
13 2
R1 R3 R4 R8 R7 R5
Q2 Q3 Q5 Q10 Q8 Q7
Q1 Q4 Q9 Q6
C1 R2 R6 C2
3 10 11 1 4 5 12
R23 R24
9 Q25 Q26 Q27
R25

9001 SCHEMATIC DIAGRAM


V_{CC}
R9 R11 R12 R13 R20 R19 R18 R16
Q15 Q16 Q23 Q22
Q11 Q14 8 6 Q21 Q20 Q18
Q13 R14 R21
Q17 Q24
R10 R15 R22 R17
Q12 Q19
13 2
R4 R8
R1 R3 Q5 Q10 R7 R5
Q2 Q3 Q8 Q7
Q1 Q4 Q9 Q6
R2 R6
3 11 1 4 12
R26 R28 R23 R24 R29 R31
10 Q28 Q29 Q30
9 Q25 Q26 Q27
5 Q31 Q32 Q33
R27 R25 R30

V_{CC} = Pin 14
GND = Pin 7

9020 SCHEMATIC DIAGRAM

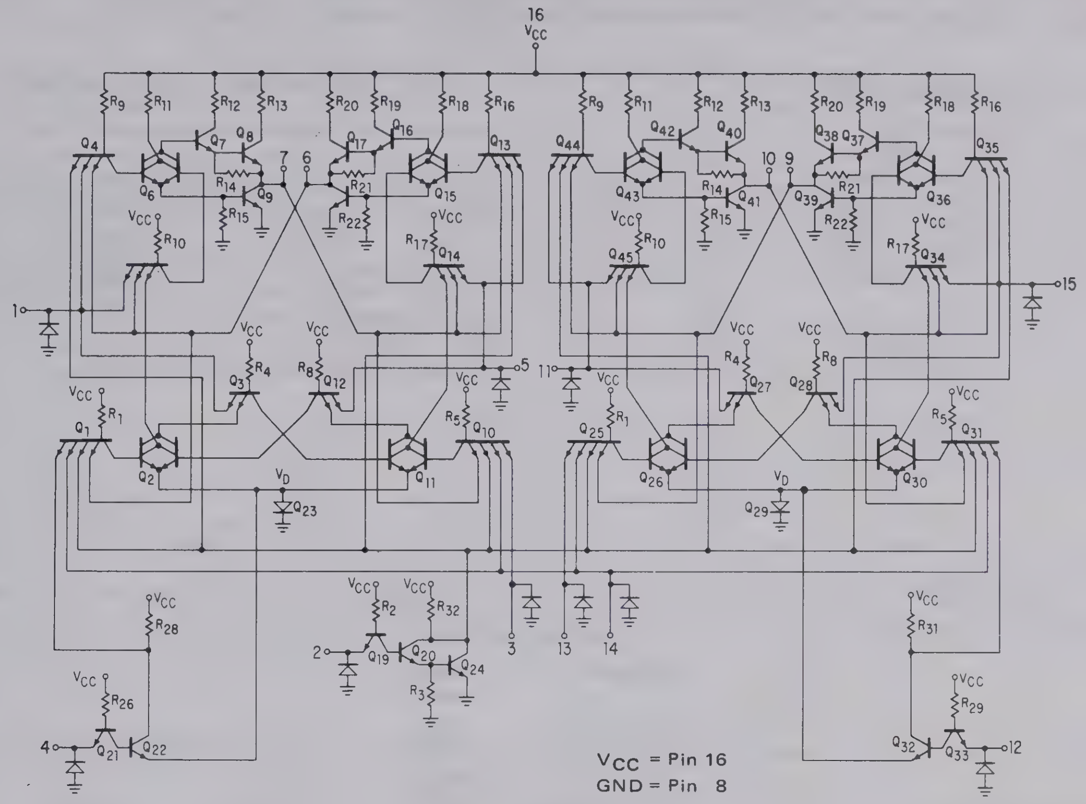

16
V_{CC}
1
2
3
4
5
6
7
9
10
11
12
13
14
15
V_D
R_1 R_2 R_3 R_4 R_5 R_8 R_9 R_{10} R_{11} R_{12} R_{13} R_{14} R_{15} R_{16} R_{17} R_{18} R_{19} R_{20} R_{21} R_{22} R_{26} R_{28} R_{29} R_{31} R_{32}
Q_1 Q_2 Q_3 Q_4 Q_6 Q_7 Q_8 Q_9 Q_{10} Q_{11} Q_{12} Q_{13} Q_{14} Q_{15} Q_{16} Q_{17} Q_{19} Q_{20} Q_{21} Q_{22} Q_{23} Q_{24} Q_{25} Q_{26} Q_{27} Q_{28} Q_{29} Q_{30} Q_{31} Q_{32} Q_{33} Q_{34} Q_{35} Q_{36} Q_{37} Q_{38} Q_{39} Q_{40} Q_{41} Q_{42} Q_{43} Q_{44} Q_{45}

V_{CC} = Pin 16
GND = Pin 8

NOMINAL COMPONENT VALUES (ALL FLIP-FLOPS)

R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4.0 kΩ
R_2, R_3, R_6, R_7 = 2.0 kΩ
R_9, R_{16}, R_{28}, R_{31} = 6.0 kΩ
R_{11}, R_{18} = 1.5 kΩ
R_{12}, R_{19} = 150 Ω
R_{13}, R_{20} = 80 Ω
R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25 kΩ
R_{32} = 1.0 kΩ
C_1, C_2 = 10 pF

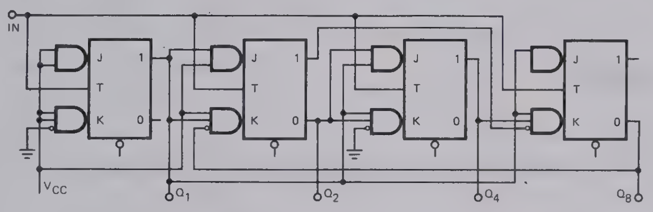
9022 SCHEMATIC DIAGRAM


16
VCC
R9
R11
R12
R13
R20
R19
R18
R16
Q4
Q6
Q7
Q8
Q9
R14
R15
7
6
Q17
Q16
R21
R22
Q15
Q13
R17
Q14
R10
Q44
Q43
Q42
Q40
Q41
10
9
Q38
Q37
Q39
Q36
Q35
Q34
Q45
15
1
Q3
R4
R8
Q12
5
11
Q27
Q28
Q1
R1
Q2
Q11
R5
Q10
Q25
Q26
Q30
Q31
VD
Q23
Q29
R28
R2
R32
Q19
Q20
Q24
R3
2
3
13
14
R31
R29
R26
4
Q21
Q22
Q32
Q33
12

VCC = Pin 16
GND = Pin 8

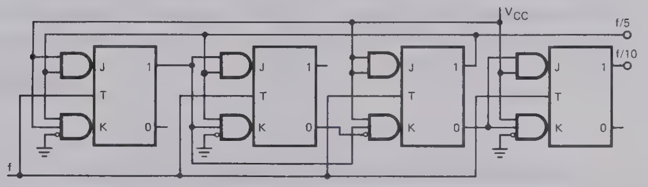
APPLICATIONS

SYNCHRONOUS BDC COUNTER


IN
J
T
K
1
0
VCC
Q1
Q2
Q4
Q8

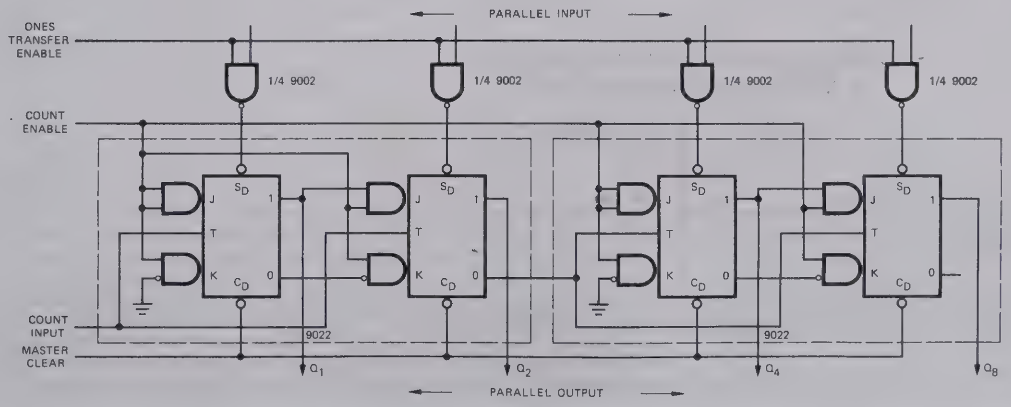
Two TTL 9020 Dual Flip-Flops require no additional gating to produce a fully synchronous 8421 code BCD Counter.

DIVIDE BY TEN COUNTER


VCC
f/5
f/10
J
T
K
1
0
f

Two TTL 9020 Dual Flip-Flops require no additional gating elements to produce divide by ten circuit with a square wave divide by ten output and a divide by five output.

BINARY COUNTER WITH ASYNCHRONOUS PARALLEL LOAD AND CLEAR


PARALLEL INPUT
ONES TRANSFER ENABLE
1/4 9002
1/4 9002
1/4 9002
1/4 9002
COUNT ENABLE
SD
J
T
K
CD
1
0
9022
9022
COUNT INPUT
MASTER CLEAR
Q1
Q2
Q4
Q8
PARALLEL OUTPUT

Binary counter using synchronous 2-bit stages with trickle down between stages illustrates method of utilizing dual JK flip-flops having common clocks in counter applications.

DUAL J$\overline{K}$ (OR D) FLIP-FLOP — 9024

The 9024 consists of two high speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

LOGIC DIAGRAM

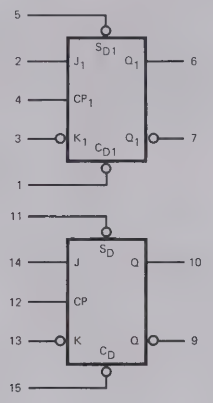


Fig. 1

FUNCTIONAL LOGIC DIAGRAM

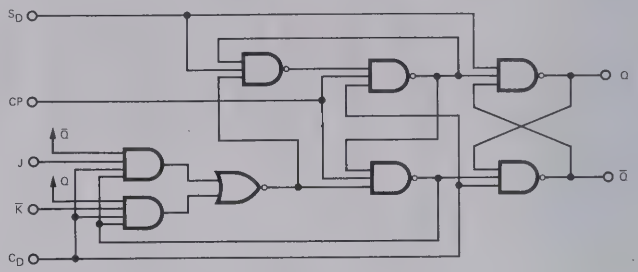


Fig. 2

LOADING FACTORS

PIN NAMES	LOADING (Note a)
J, $\overline{K}$	1 U.L.
Clock, S$_D$	2 U.L.
C$_D$	3 U.L.
Outputs (Note b)	10 U.L.

Fig. 3

NOTES:

a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW; the HIGH load factor of 40 μA measured at 2.4 V is considered equivalent to 60 μA measured at 4.5 V for purposes of system loading calculations.

b. 10 U.L. is the LOW drive factor and 30 U.L. is the HIGH drive factor.

TRUTH TABLES

SYNCHRONOUS ENTRY J-$\overline{K}$ MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
S$_D$	C$_D$	Q	$\overline{Q}$
5(11)	1(15)	6(10)	7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

L = LOW Logic Level
H = HIGH Logic Level

ELECTRICAL CHARACTERISTICS 9024XC (T_A = 0°C to 75°C, V_{CC} = 5 V ±5%) (Note 3)

SYMBOL	PARAMETER	LIMITS							UNITS	TEST CONDITIONS	
		0°C		25°C			75°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{IH}	Input HIGH Voltage	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −1.2 mA	
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16 mA	
I_{IH}	Input HIGH Current								μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V GND on Other Inputs	
	J, $\overline{K}$				5.0	60		60			
	Clock Input, S_D				10	120		120			
	C_D				20	240		240			
I_{IL}	Input LOW Current								mA	V_{CC} = 5.25 V	V_{IN} = 0.45 V 4.5 V on Other Inputs
	J, $\overline{K}$		−1.6		−1.0	−1.6		−1.6			
	Clock Input, S_D		−3.2		−2.0	−3.2		−3.2			
	C_D (Note 4)		−4.8		−3.0	−4.8		−4.8			
	J, $\overline{K}$		−1.41		−0.94	−1.41		−1.41	mA	V_{CC} = 4.75 V	
	Clock Input, S_D		−2.82		−1.88	−2.82		−2.82			
	C_D (Note 4)		−4.23		−2.82	−4.23		−4.23			
I_{SC}	Output HIGH Short Circuit Current	−30	−100	−30	−65	−100	−30	−100	mA	V_{CC} = 5.25 V, V_{OUT} = 0.0 V	
I_{CC}	Current Drain				9.0	14			mA	Per Flip-Flop in Worst Logic State	

ELECTRICAL CHARACTERISTICS 9024XM (T_A = −55°C to 125°C, V_{CC} = 5 V ±10%) (Note 3)

SYMBOL	PARAMETER	LIMITS							UNITS	TEST CONDITIONS	
		−55°C		25°C			125°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{IH}	Input HIGH Voltage	2.0		1.7			1.4		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage		0.8			0.9		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{OH}	Output HIGH Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −1.2 mA	
V_{OL}	Output LOW Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 12.4 mA	
			0.4		0.25	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 16 mA	
I_{IH}	Input HIGH Current								μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V GND on Other Inputs	
	J, $\overline{K}$				5.0	60		60			
	Clock Input, S_D				10	120		120			
	C_D				20	240		240			
I_{IL}	Input LOW Current								mA	V_{CC} = 5.5 V	V_{IN} = 0.4 V 4.5 V on Other Inputs
	J, $\overline{K}$		−1.6		−1.1	−1.6		−1.6			
	Clock Input, S_D		−3.2		−2.2	−3.2		−3.2			
	C_D (Note 4)		−4.8		−3.3	−4.8		−4.8			
	J, $\overline{K}$		−1.24		−0.91	−1.24		−1.24	mA	V_{CC} = 4.5 V	
	Clock Input, S_D		−2.48		−1.82	−2.48		−2.48			
	C_D (Note 4)		−3.72		−2.73	−3.72		−3.72			
I_{SC}	Output HIGH Short Circuit Current	−30	−100	−30	−65	−100	−30	−100	mA	V_{CC} = 5.5 V, V_{OUT} = 0.0 V	
I_{CC}	Current Drain				9.0	14			mA	Per Flip-Flop in Worst Logic State	

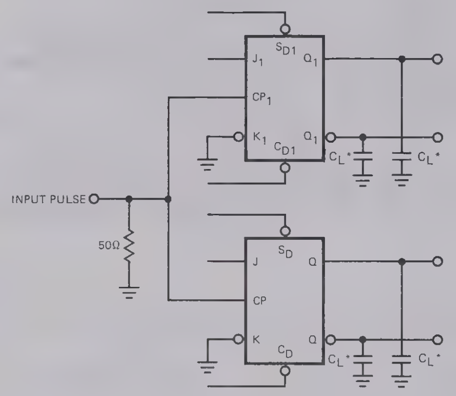
NOTES:

1. The maximum V_{CC} value of 8.0 V is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a HIGH output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 V.
2. Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.
3. Postive current is into device and negative current is out of device.
4. Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, $\overline{K}$ = HIGH and S_D = LOW.

SWITCHING CHARACTERISTICS ($T_A = 25^oC$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
			25°C			
		MIN.	TYP.	MAX.		
t_{PLH}	Clock to Q or $\overline{Q}$		12	20	ns	V_{CC} = 5.0 V C_L = 15 pF Each Flip-Flop
t_{PHL}	Clock to Q or $\overline{Q}$		22	33	ns	
$t_{release}$			2.0		ns	
t_{set-up}		20	15	1.0	ns	
t_{PLH}	S_D to Q, C_D to $\overline{Q}$		8.0	12	ns	
t_{PHL}	S_D to $\overline{Q}$, C_D to Q		20	25	ns	
	Toggle Frequency	25	30		MHz	

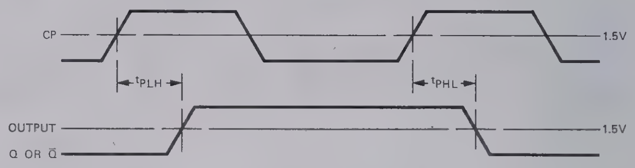
SWITCHING TEST CIRCUIT



S_{D1}
J_1
Q_1
CP_1
K_1
C_{D1}
$\overline{Q}_1$
C_L*
C_L*
INPUT PULSE
50Ω
S_D
J
Q
CP
K
C_D
$\overline{Q}$
C_L*
C_L*

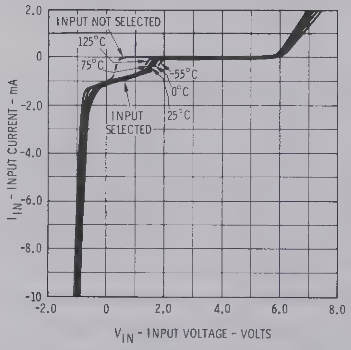
*C_L includes probe and jig capacitance

WAVEFORMS

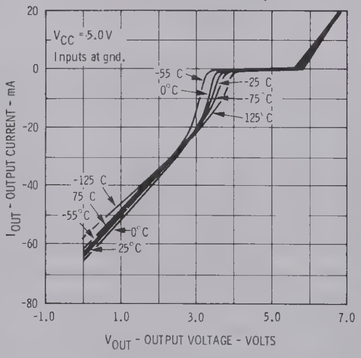


CP
1.5V
t_{PLH}
t_{PHL}
OUTPUT
Q OR $\overline{Q}$
1.5V

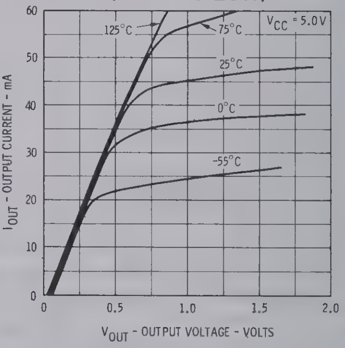
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



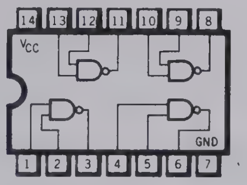
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



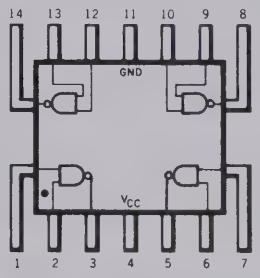
QUAD 2-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

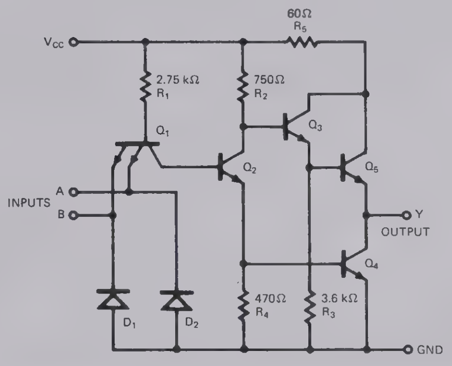


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H00XM/54H00XM			9H00XC/74H00XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., $I_{OH} = -0.5$ mA, $V_{IN} = 0.8$ V		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., $I_{OL} = 20$ mA, $V_{IN} = 2.0$ V		1
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., $V_{IN} = 2.4$ V	Each Input	4
				1.0	mA	V_{CC} = MAX., $V_{IN} = 5.5$ V		
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., $V_{IN} = 0.4$ V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX.		5
I_{CCH}	Supply Current HIGH		10	16.8	mA	V_{CC} = MAX., $V_{IN} = 0$ V		6
I_{CCL}	Supply Current LOW		26	40	mA	V_{CC} = MAX., $V_{IN} = 4.5$ V		6

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		5.9	10	ns	$V_{CC} = 5.0$ V $C_L = 25$ pF $R_L = 280Ω$	T
t_{PHL}	Turn On Delay Input to Output		6.2	10	ns		

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at $V_{CC} = 5.0$ V, 25°C.

(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

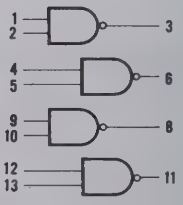
LPTTL/SSI 9L00

LOW POWER QUAD 2-INPUT NAND GATE

DESCRIPTION – The low power TTL/SSI 9L00 consists of four NAND gates. Each gate has two inputs and performs positive logic. The 9L00 is designed for low power and medium speed operation.

- TYPICAL PROPAGATION DELAY OF 20 ns
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 14-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

LOGIC SYMBOL



1
2
3
4
5
6
9
10
8
12
13
11

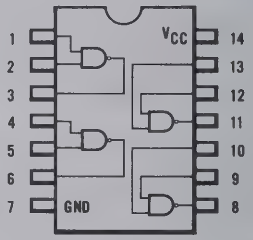
V_{CC} = PIN 14
GND = PIN 7

PIN NAMES

PIN NAMES	LOADING HIGH	LOADING LOW
INPUTS (Pins 1, 2, 4, 5, 9, 10, 12, 13)	0.5 U.L.	0.25 U.L.
OUTPUTS (Pins 3, 6, 8, 11)	10 U.L.	2.5 U.L.

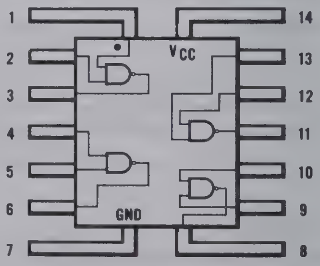
1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.

CONNECTION DIAGRAM
DIP (TOP VIEW)



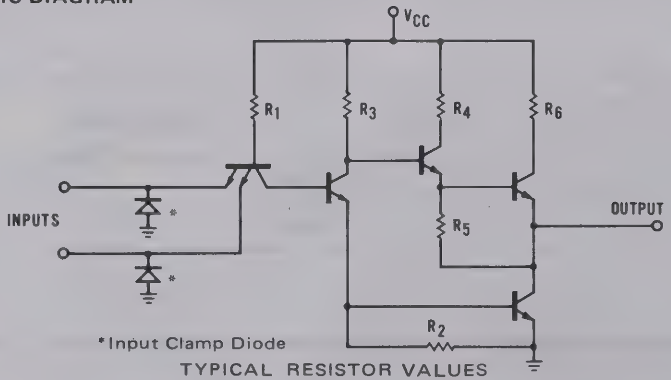
V_{CC}
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8

FLATPAK (TOP VIEW)



V_{CC}
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8

SCHEMATIC DIAGRAM



V_{CC}
R_1
R_3
R_4
R_6
R_5
R_2
INPUTS
OUTPUT
*
*

*Input Clamp Diode

TYPICAL RESISTOR VALUES

R_1 = 16 kΩ
R_2 = 5 kΩ
R_3 = 6 kΩ
R_4 = 600 Ω
R_5 = 16 kΩ
R_6 = 320 Ω

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L00XM	4.5 V	5.0 V	5.5 V	–55°C to 125°C
9L00XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted) (See Notes 1, 2)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP. Note 3	MAX.			
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = V_{IL}	
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, V_{IN} = V_{IH}	
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input LOW threshold voltage for all inputs	
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input HIGH threshold voltage for all inputs	
I_{IL}	Input LOW Current		–0.25	–0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V, Other Input = 4.5V	
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Other Input = 0.0V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{SC} (Note 4)	Output Short Circuit Current	–10	–22	–40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V, Inputs Grounded	
I_{CC}	Power Supply Current per Gate		0.9	1.56	mA	V_{CC} = MAX., Inputs HIGH	
			0.28	0.41	mA	V_{CC} = MAX., Inputs LOW	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
4. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		15		ns	V_{CC} = 5.0V See Fig. 1
t_{PHL}	Turn On Delay Input to Output		25		ns	C_L = 15 pF

SWITCHING TIME WAVEFORMS

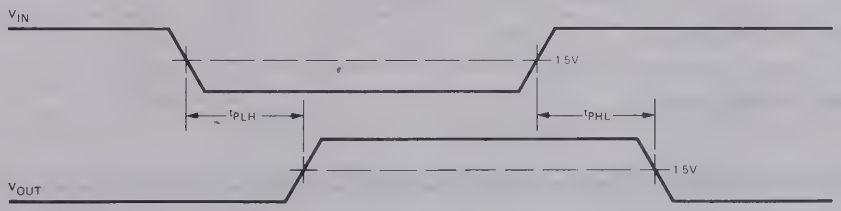
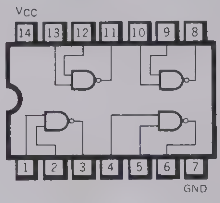


Fig. 1

QUAD 2-INPUT NAND GATE

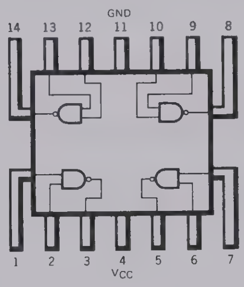
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

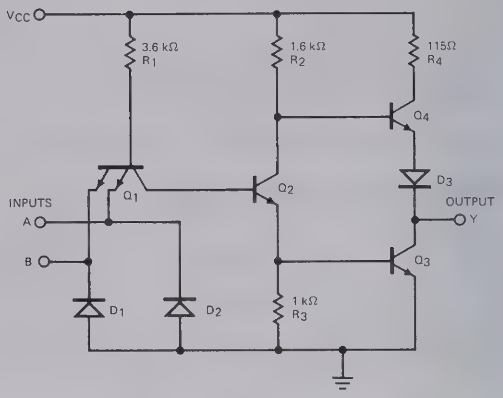


Positive logic: $Y = \overline{AB}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N00XM/5400XM			9N00XC/7400XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = 0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	3
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N00/5400	V_{CC} = MAX.	5
		−18		−55	mA	9N00/7400		
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0V		6
I_{CCL}	Supply Current LOW		12	22	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

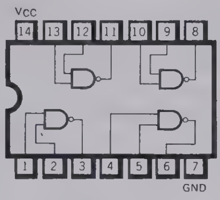
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		11	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		7.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Note more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

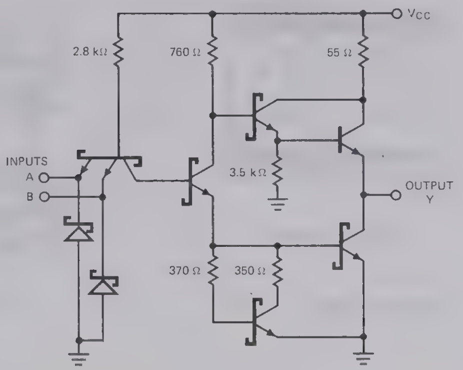
DIP (TOP VIEW)



Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S00XM/54S00XM			9S00XC/74S00XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = -1.0mA, V_{IN} = 0.8V	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current			1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current			−1.4	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V	Each Input
I_{OS}	Output Short Circuit Current (Note 3)		−40	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0V	
I_{CCH}	Supply Current HIGH			10.8	16.0	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW			25.2	36.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

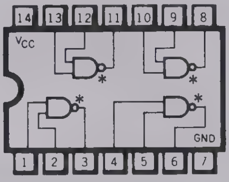
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	3.0	4.5	ns	V_{CC} = 5.0V	DD
t_{PHL}	Turn On Delay Input to Output	2.0	3.0	5.0	ns	C_L = 15pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

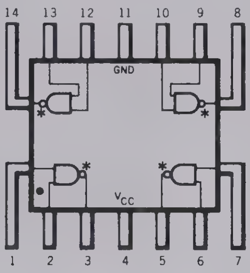
DIP (TOP VIEW)



*Open collector

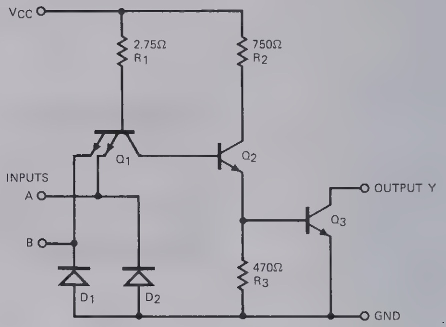
Positive logic: $Y = \overline{AB}$

FLATPAK (Top View)



*Open collector

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H01XM/54H01XM			9H01XC/74H01XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V		7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{CCH}	Supply Current HIGH		6.8	10	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		26	40	mA	V_{CC} = MAX., V_{IN} = 4.5 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

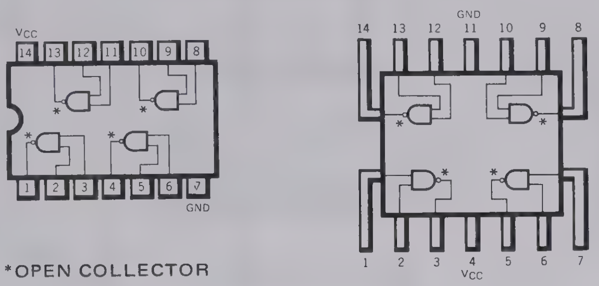
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		7.5	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

QUAD 2-INPUT NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW) **FLATPAK** (TOP VIEW)

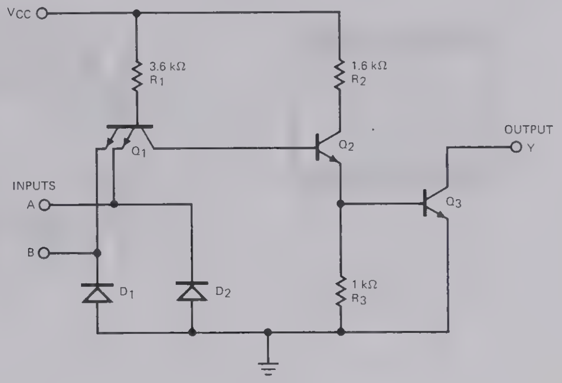


*OPEN COLLECTOR

Positive logic: $Y = \overline{AB}$

*OPEN COLLECTOR

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N01XM/5401XM			9N01XC/7401XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IL} = 0.8 V		7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V (On Level)		1
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	3
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		12	22	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

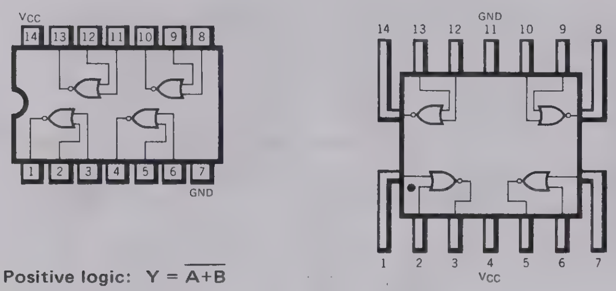
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay Input to Output		35	45	ns	R_L = 4.0 kΩ	V_{CC} = 5.0 V C_L = 15 pF	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	R_L = 400Ω		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

QUAD 2-INPUT NOR GATE

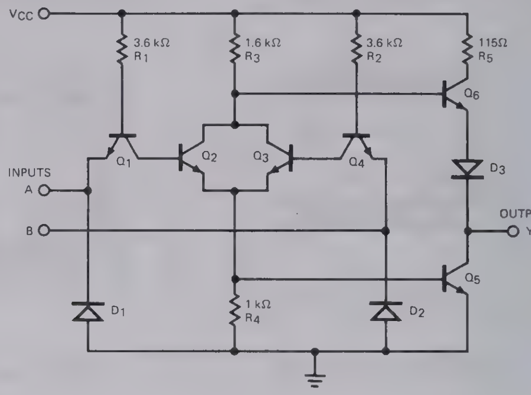
LOGIC AND CONNECTION DIAGRAM


DIP (TOP VIEW)

FLATPAK (TOP VIEW)

Positive logic: $Y = \overline{A+B}$

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N02XM/5402XM			9N02XC/7402XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		8
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		9
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V		9
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		10
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	12
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		11
I_{OS}	Output Short Circuit Current	–20		–55	mA	9N02/5402	V_{CC} = MAX.	13
	(Note 3)	18		–55	mA	9N02/7402		
I_{CCH}	Supply Current HIGH		8.0	16	mA	V_{CC} = MAX., V_{IN} = 0 V		14
I_{CCL}	Supply Current LOW		14	27	mA	V_{CC} = MAX., V_{IN} = 5.0 V		14

SWITCHING CHARACTERISTICS (T_A = 25°C)

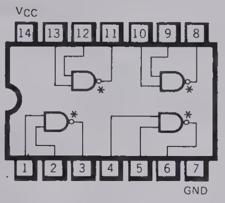
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		12	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

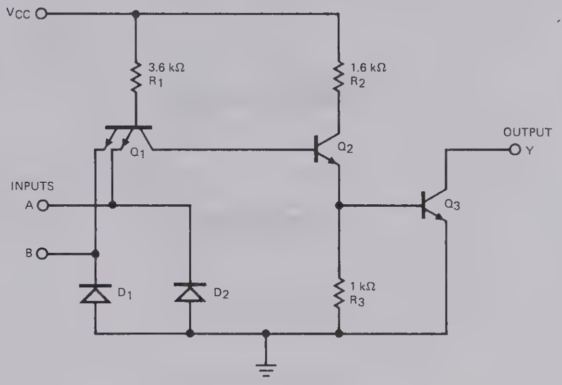
DIP (TOP VIEW)



*OPEN COLLECTOR

Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N03XM/5403XM			9N03XC/7403XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V		7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V (On Level)		1
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0V		6
I_{CCL}	Supply Current LOW		12	22	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

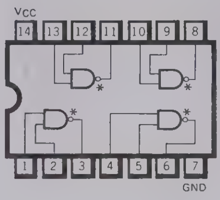
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay Input to Output		35	45	ns	R_L = 4.0 kΩ	V_{CC} = 5.0 V	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	R_L = 400Ω	C_L = 15 pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

QUAD 2-INPUT NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

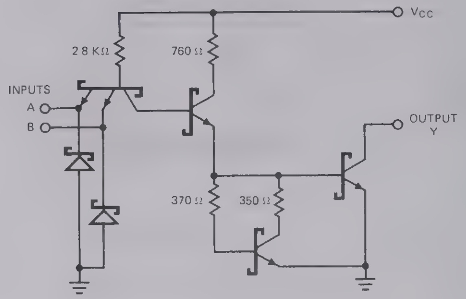


* OPEN COLLECTOR

Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	† 9S03XM/54S03XM			9S03XC/74S03XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X= package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage		–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
I_{OH}	Output HIGH Current		0.1	250	µA	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = 0.8V	
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current		1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V	Each Input
I_{CCH}	Supply Current HIGH		6.0	13.2	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW		25.2	36.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0V	EE
t_{PHL}	Turn On Delay Input to Output	2.0	4.5	7.0	ns	C_L = 15pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.

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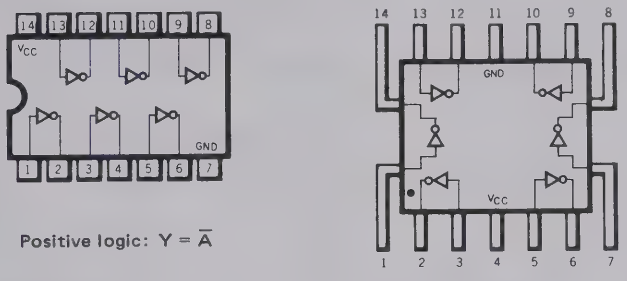
† To be announced 1972

HEX INVERTER

LOGIC AND CONNECTION DIAGRAM

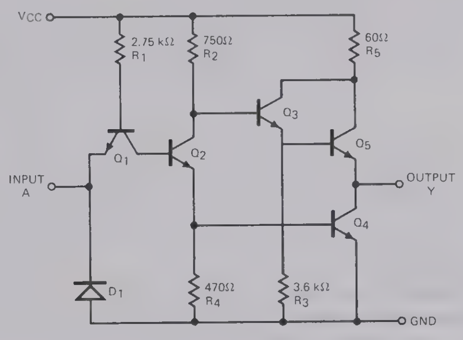


DIP (TOP VIEW)

FLATPAK (TOP VIEW)

Positive logic: $Y = \overline{A}$

SCHEMATIC DIAGRAM
(EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H04XM/54H04XM			9H04XC/74H04XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	15
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	16
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA, V_{IN} = 0.8 V	16
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0V	15
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	18
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	18
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX.	19
I_{CCH}	Supply Current HIGH		16	26	mA	V_{CC} = MAX., V_{IN} = 0 V	20
I_{CCL}	Supply Current LOW		40	58	mA	V_{CC} = MAX., V_{IN} = 4.5 V	20

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.5	10	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		9.0	13	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

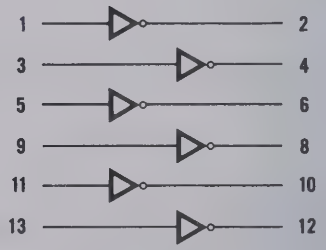
LPTTL/SSI 9L04

LOW POWER HEX INVERTER

DESCRIPTION — The low power TTL/SSI 9L04 consists of six TTL gates, each performing a single inversion function. Designed for low power, medium speed operation, the 9L04 is very useful where a number of complement signals are desired simultaneously.

- TYPICAL PROPAGATION DELAY OF 20 ns
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 14-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

LOGIC SYMBOL


1
2
3
4
5
6
9
8
11
10
13
12

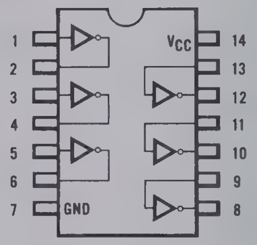
V_{CC} = Pin 14
GND = Pin 7

PIN NAMES	LOADING HIGH	LOADING LOW
INPUTS (Pins 1, 3, 5, 9, 11, 13)	0.5 U.L.	0.25 U.L.
OUTPUTS (Pins 2, 4, 6, 8, 10, 12)	10 U.L.	2.5 U.L.

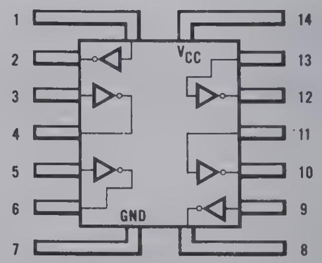
1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.

CONNECTION DIAGRAMS

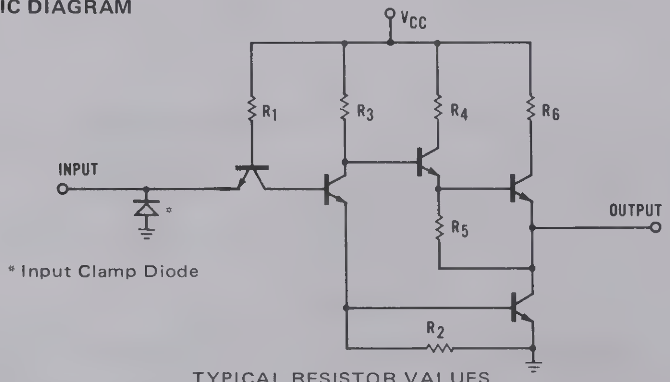
DIP (Top View)


1
2
3
4
5
6
7
GND
VCC
14
13
12
11
10
9
8

FLATPAK (Top View)


1
2
3
4
5
6
7
GND
VCC
14
13
12
11
10
9
8

SCHEMATIC DIAGRAM


VCC
R1
R3
R4
R6
R5
R2
INPUT
OUTPUT
*

* Input Clamp Diode

TYPICAL RESISTOR VALUES

R_1 = 16 kΩ R_3 = 6 kΩ R_5 = 16 kΩ
R_2 = 5 kΩ R_4 = 600 Ω R_6 = 320 Ω

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L04XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9L04XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (UNLESS OTHERWISE NOTED) (See Notes 1 & 2)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. Note 3	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, $V_{IN} = V_{IL}$
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, $V_{IN} = V_{IH}$
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 4)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.00 V, Inputs grounded
I_{CC}	Power Supply Current per Gate		0.9	1.56	mA	V_{CC} = MAX., Input HIGH
			0.28	0.45	mA	V_{CC} = MAX., Input LOW

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
4. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		15		ns	V_{CC} = 5.0V See Fig. 1
t_{PHL}	Turn On Delay Input to Output		25		ns	C_L = 15 pF

SWITCHING TIME WAVEFORM

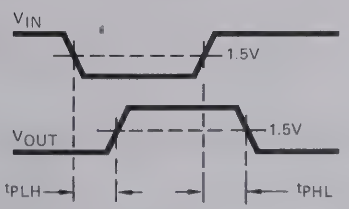
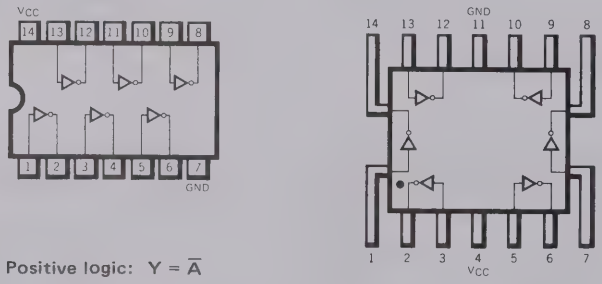


Fig. 1

HEX INVERTER

LOGIC AND CONNECTION DIAGRAM

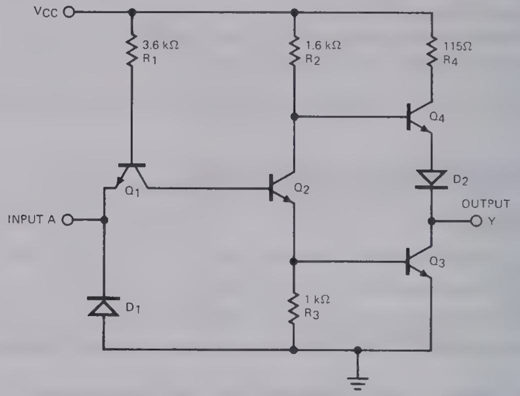


DIP (TOP VIEW)

FLATPAK (TOP VIEW)

Positive logic: $Y = \overline{A}$

SCHEMATIC DIAGRAM (EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N04XM/5404XM			9N04XC/7404XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		15
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		16
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V		16
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		15
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V		18
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		18
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N04/5404	V_{CC} = MAX.	19
		–18		–55	mA	9N04/7404		
I_{CCH}	Supply Current HIGH		6.0	12	mA	V_{CC} = MAX., V_{IN} = 0 V		20
I_{CCL}	Supply Current LOW		18	33	mA	V_{CC} = MAX., V_{IN} = 5.0 V		20

SWITCHING CHARACTERISTICS (T_A = 25°C)

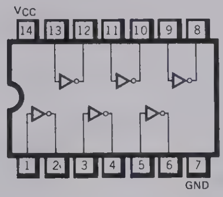
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		12	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

FAIRCHILD SUPER HIGH SPEED TTL/SSI • 9S04/54S04, 74S04 • 9S04A

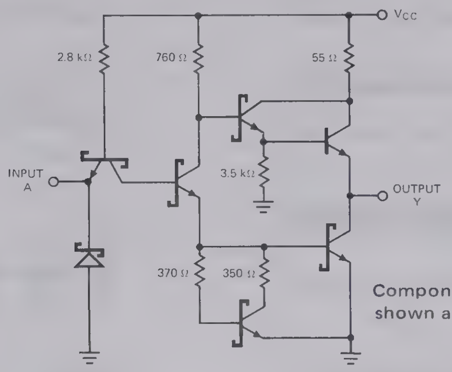
HEX INVERTER

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: $Y = \overline{A}$

SCHEMATIC DIAGRAM
(EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S04XM/54S04XM 9S04AXM			9S04XC/74S04XC 9S04AXC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA, V_{IN} = 0.8 V
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current			–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			16.2	24.0	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCL}	Supply Current LOW			37.8	54.0	mA	V_{CC} = MAX., Inputs Open

SWITCHING CHARACTERISTICS (T_A = 25°C)

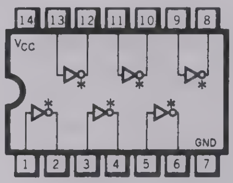
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
			MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	9S04	2.0	3.0	4.5	ns	V_{CC} = 5.0 V	DD
		9S04A	1.0	2.5	3.5			
t_{PHL}	Turn On Delay Input to Output	9S04	2.0	3.0	5.0	ns	C_L = 15 pF	
		9S04A	1.0	2.5	4.0			

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

HEX INVERTER (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

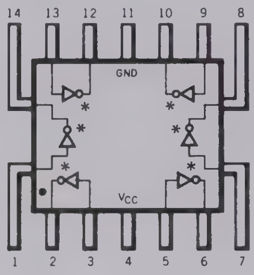
DIP (TOP VIEW)



*OPEN COLLECTOR

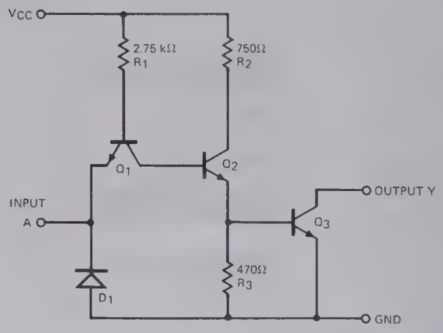
Positive logic: $Y = \overline{A}$

FLATPAK (TOP VIEW)



*OPEN COLLECTOR

SCHEMATIC DIAGRAM (EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H05XM/54H05XM			9H05XC/74H05XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	15
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	17
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V	17
V_{OL}	Output LOW Voltage (On Level)			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V	15
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	18
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	18
I_{CCH}	Supply Current HIGH		16	26	mA	V_{CC} = MAX., V_{IN} = 0 V	20
I_{CCL}	Supply Current LOW		40	58	mA	V_{CC} = MAX., V_{IN} = 4.5 V	20

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	18	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		10	15	ns		

NOTES:

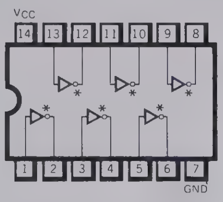
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

HEX INVERTER
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

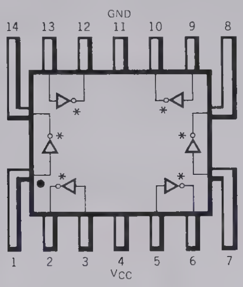
DIP (TOP VIEW)



*OPEN COLLECTOR

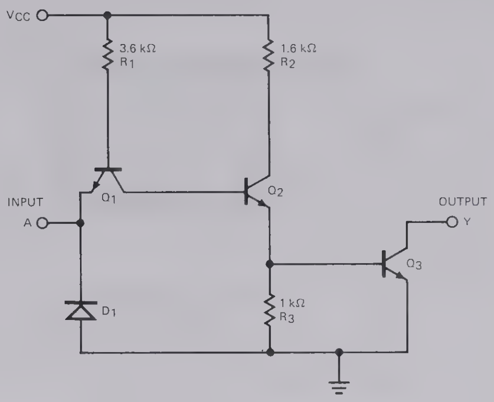
Positive logic: Y = $\overline{A}$

FLATPAK (TOP VIEW)



*OPEN COLLECTOR

SCHEMATIC DIAGRAM
(EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N05XM/5405XM			9N05XC/7405XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		15
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		17
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V		17
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V (On Level)		15
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V		18
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		18
I_{CCH}	Supply Current HIGH		6	12	mA	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = 25°C	20
I_{CCL}	Supply Current LOW		18	33	mA	V_{IN} = 5 V		20

SWITCHING CHARACTERISTICS (T_A = 25°)

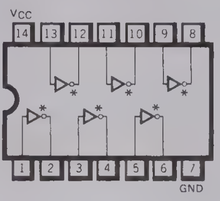
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay Input to Output		40	55	ns	R_L = 4kΩ	V_{CC} = 5.0 V	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	R_L = 400Ω	C_L = 15 pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

HEX INVERTER
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

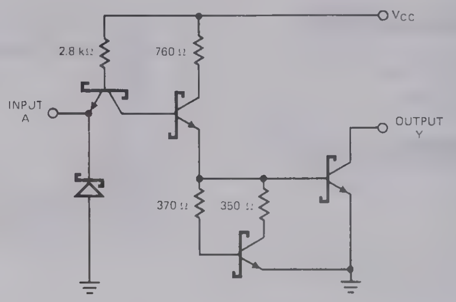


* OPEN COLLECTOR

Positive logic: Y = $\overline{A}$

SCHEMATIC DIAGRAM

(EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	† 9S05XM/54S05XM † 9S05AXM			9S05XC/74S05XC 9S05AXC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage		–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = 0.8V
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
I_{CCH}	Supply Current HIGH		9.0	19.8	mA	V_{CC} = MAX., V_{IN} = 0V
I_{CCL}	Supply Current LOW		37.8	54.0	mA	V_{CC} = MAX., Inputs Open

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
			MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	9S05	2.0	5.0	7.5	ns	V_{CC} = 5.0V	EE
		9S05A	2.0	4.0	5.5			
t_{PHL}	Turn On Delay Input to Output	9S05	2.0	4.5	7.0	ns	C_L = 15pF	
		9S05A	1.5	3.4	5.0			

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.

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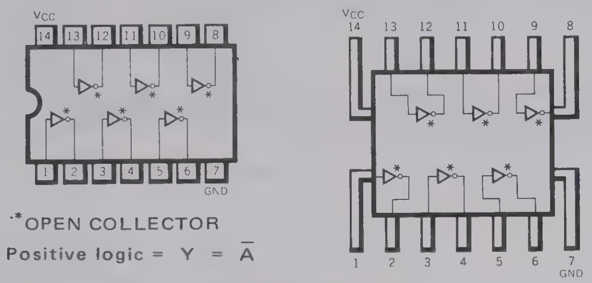
† To be announced 1972.

HEX INVERTER BUFFER/DRIVER
(WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUT)

DESCRIPTION – These TTL/SSI hex inverter buffer/driver feature high voltage open collector output for interfacing with high level circuits (such as MOS), or for driving high current loads (such as lamps or relays) and are also characterized for use as inverter buffers for driving TTL inputs. For increased fan out, several inverters in a single package may be paralleled. The 9N06/5406, 7406 have minimum breakdown voltages of 30V and the 9N16/5416, 7416 have minimum breakdown voltages of 15V. The maximum sink current is 30 mA for the 9N06/5406 and 9N16/5416 and 40 mA for the 9N06/7406 and 9N16/7416.

LOGIC AND CONNECTION DIAGRAM

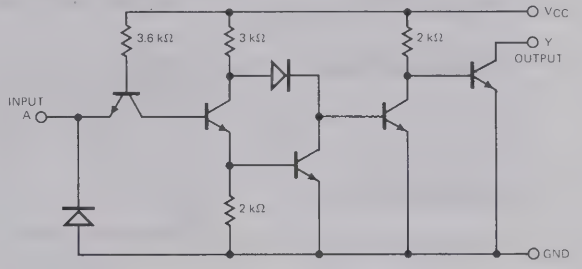
DIP (TOP VIEW) FLATPAK (TOP VIEW)



*OPEN COLLECTOR

Positive logic = Y = $\overline{A}$

SCHEMATIC DIAGRAM
(EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N06XM/5406XM 9N16XM/5416XM			9N06XC/7406XC 9N16XC/7416XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Output HIGH Voltage, V_{OH}	9N06/5406, 7406			30			30	Volts
	9N16/5416, 7416			15			15	
Output LOW Current, I_{OL}				30			40	mA

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		65
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		66
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = MAX., V_{IN} = 0.8 V		66
V_{OL}	Output LOW Voltage			0.7	Volts	I_{OL} = MAX.	V_{CC} = MIN., V_{IN} = 2.0 V	65
				0.4	Volts	I_{OL} = 16 mA		
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	67
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		68
I_{CCH}	Supply Current HIGH		30	42	mA	V_{CC} = MAX., V_{IN} = 0V		69
I_{CCL}	Supply Current LOW		27	38	mA	V_{CC} = MAX., V_{IN} = 5.0 V		69

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		10	15 *	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 110Ω	J
t_{PHL}	Turn On Delay Input to Output		15	23	ns		

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

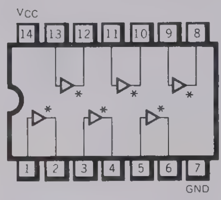
* Max. 17 ns at 125°C

HEX BUFFER/DRIVER
(WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUT)

DESCRIPTION — These TTL/SSI hex buffer/driver feature high voltage open collector output for interfacing with high level circuits (such as MOS), or for driving high current loads (such as lamps or relays) and are also characterized for use as buffers for driving TTL inputs. For increased fan out, several buffers in a single package may be paralleled. The 9N07/5407, 7404 have minimum breakdown voltages of 30V and the 9N17/5417, 7417 have minimum breakdown voltages of 15V. The maximum sink current is 30 mA for the 9N07/5407 and 40 mA for the 9N07/7407 and 9N17/7417.

LOGIC AND CONNECTION DIAGRAM

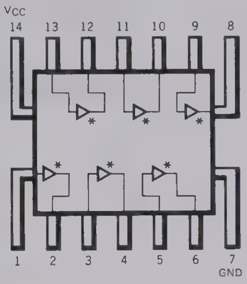
DIP (TOP VIEW)



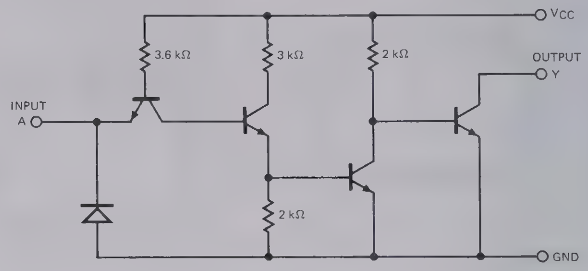
*OPEN COLLECTOR

Positive logic: Y = A

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH BUFFER/DRIVER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N07XM/5407XM 9N17XM/5417XM			9N07XC/7407XC 9N17XC/7417XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Output HIGH Level Voltage, V_{OH}	9N07/5407, 7407			30			30	Volts
	9N17/5417, 7417			15			15	
Output LOW Level Current, I_{OL}				30			40	mA

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		70
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		71
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = MAX., V_{IN} = 2.0 V		70
V_{OL}	Output LOW Voltage			0.7	Volts	I_{OL} = MAX.	V_{CC} = MIN. V_{IN} = 0.8 V	71
				0.4	Volts	I_{OL} = 16 mA		
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	72
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		73
I_{CCH}	Supply Current HIGH		29	41	mA	V_{CC} = MAX., V_{IN} = 5 V		74
I_{CCL}	Supply Current LOW		21	30	mA	V_{CC} = MAX., V_{IN} = 0V		74

SWITCHING CHARACTERISTICS (T_A = 25°C)

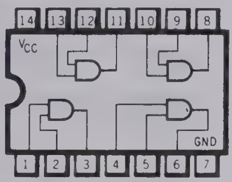
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.0	10	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 110Ω	K
t_{PHL}	Turn On Delay Input to Output		20	30	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

QUAD 2-INPUT AND GATE

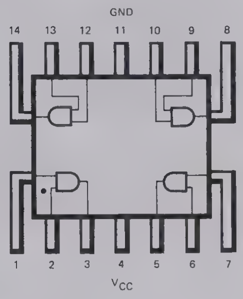
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

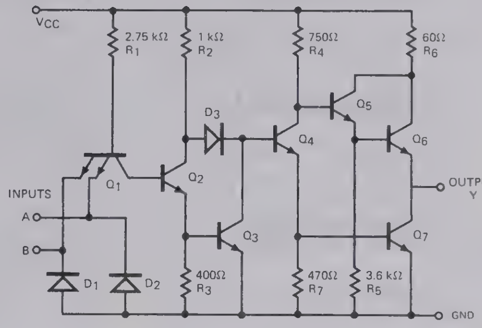


Positive logic: Y = AB

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H08XM/5408XM			9H08XC/74H08XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	75
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	77
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA, V_{IN} = 2.0V	75
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 0.8 V	77
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V — Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	79
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX. V_{IN} = 4.5 V	80
I_{CCH}	Supply Current HIGH		24	40	mA	V_{CC} = MAX., V_{IN} = 4.5 V	81
I_{CCL}	Supply Current LOW		40	64	mA	V_{CC} = MAX., V_{IN} = 0 V	81

SWITCHING CHARACTERISTICS (T_A = 25°C)

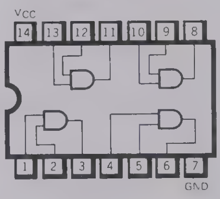
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.6	12	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		8.8	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

QUAD 2-INPUT AND GATE

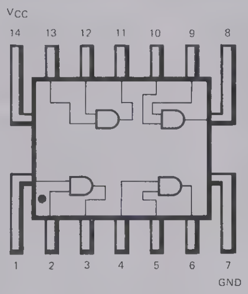
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

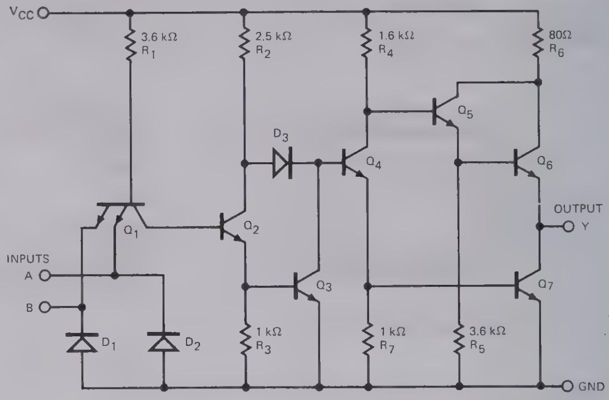


Positive logic: Y = AB

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N08XM/5408XM			9N08XC/7408XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		75
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		77
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.8 mA, V_{IH} = 2.0 V		75
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IL} = 0.8 V		77
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	79
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX.		80
I_{CCH}	Supply Current HIGH			20	mA	V_{CC} = MAX., V_{IN} = 5 V		81
I_{CCL}	Supply Current LOW			32	mA	V_{CC} = MAX., V_{IN} = 0 V		81

SWITCHING CHARACTERISTICS (T_A = 25°C)

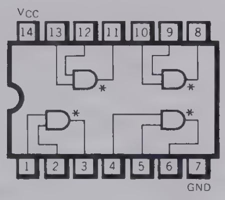
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		17.5	40	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	L
t_{PHL}	Turn On Delay Input to Output		12	25	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C
(3) Not more than one output should be shorted at a time.

QUAD 2-INPUT AND GATE (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

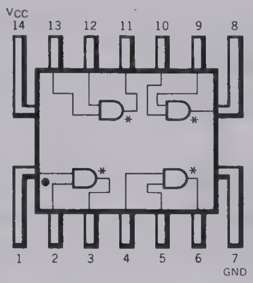
DIP (TOP VIEW)



*OPEN COLLECTOR

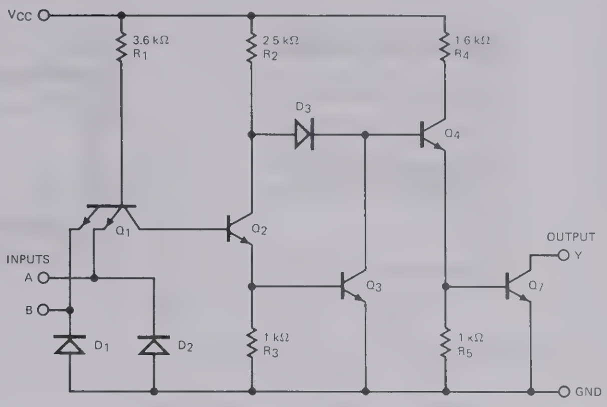
Positive logic: Y = AB

FLATPAK (TOP VIEW)



*OPEN COLLECTOR

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N09XM/5409XM			9N09XC/7409XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		76
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		77
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{IH} = 2.0 V, V_{OH} = 5.5 V		76
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IL} = 0.8 V		77
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V;	Each Input	79
I_{CCH}	Supply Current HIGH		11	21	mA	V_{CC} = MAX., V_{IN} = 5.0 V		81
I_{CCL}	Supply Current LOW		20	33	mA	V_{CC} = MAX., V_{IN} = 0 V		81

SWITCHING CHARACTERISTICS (T_A = 25°C)

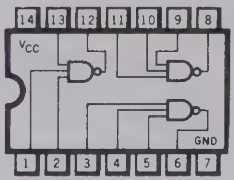
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		21	32	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	L
t_{PHL}	Turn On Delay Input to Output		16	24	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

TRIPLE 3-INPUT NAND GATE

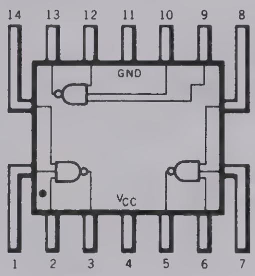
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

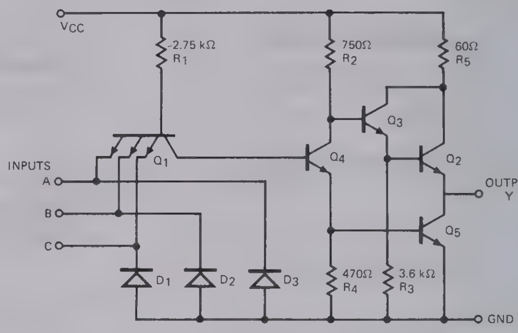


Positive logic: $Y = \overline{ABC}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H10XM/54H10XM			9H10XC/74H10XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0V		1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX.		5
I_{CCH}	Supply Current HIGH		7.5	12.6	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		19.5	30	mA	V_{CC} = MAX., V_{IN} = 4.5 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		5.9	10	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		6.3	10	ns		

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

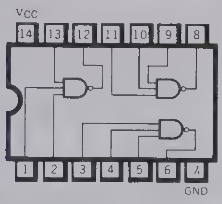
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

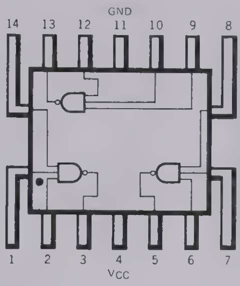
TRIPLE 3-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

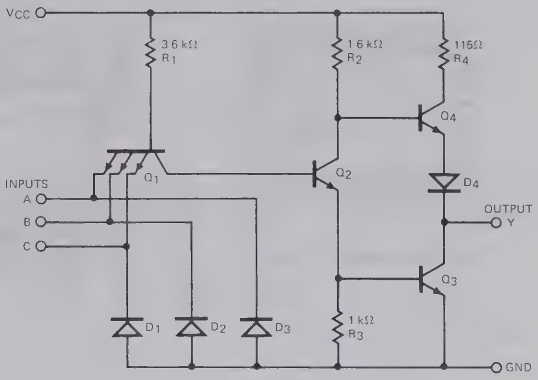


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{ABC}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N10XM/5410XM MIN.	9N10XM/5410XM TYP.	9N10XM/5410XM MAX.	9N10XC/7410XC MIN.	9N10XC/7410XC TYP.	9N10XC/7410XC MAX.	UNITS
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N10/5410	V_{CC} = MAX.	5
		–18		–55	mA	9N10/7410		
I_{CCH}	Supply Current HIGH		3.0	6.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		9.0	16.5	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output		11	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		7.0	15	ns		

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

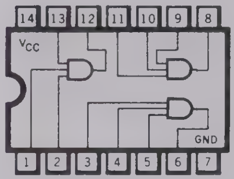
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time.

TRIPLE 3-INPUT AND GATE

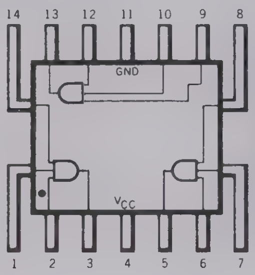
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

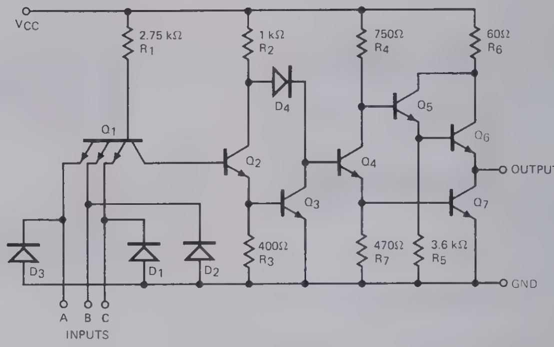


Positive logic: Y = ABC

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H11XM/54H11XM			9H11XC/74H11XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		75
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		77
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA, V_{IN} = 2.0V		75
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 0.8 V		77
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		79
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 4.5 V		80
I_{CCH}	Supply Current HIGH		18	30	mA	V_{CC} = MAX., V_{IN} = 4.5V		81
I_{CCL}	Supply Current LOW		30	48	mA	V_{CC} = MAX., V_{IN} = 0 V		81

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.6	12	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		8.8	12	ns		

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

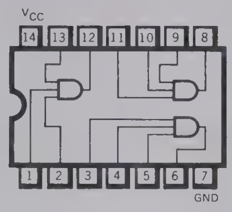
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

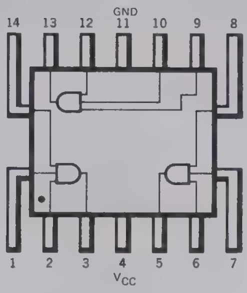
TRIPLE 3-INPUT AND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

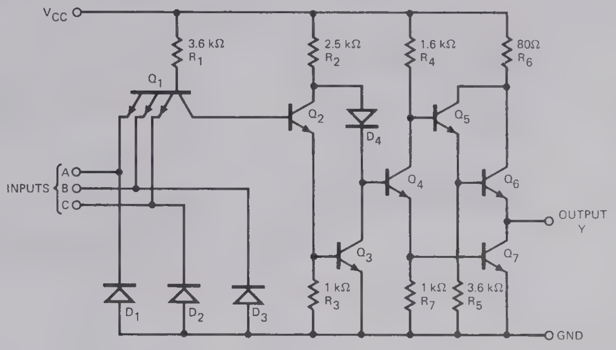


FLATPAK (TOP VIEW)



Positive logic: Y = ABC

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N11XM/5411XM			9N11XC/7411XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 2 V	
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 0.8 V	
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 4.5 V	
I_{CCH}	Supply Current HIGH		10	15	mA	V_{CC} = MAX., V_{IN} = 0 V	
I_{CCL}	Supply Current LOW		6.0	24	mA	V_{CC} = MAX., V_{IN} = 5.0 V	

SWITCHING CHARACTERISTICS (T_A = 25°C)

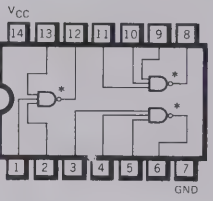
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		18	40	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω
t_{PHL}	Turn On Delay Input to Output		14	25	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

TRIPLE 3-INPUT NAND GATE (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

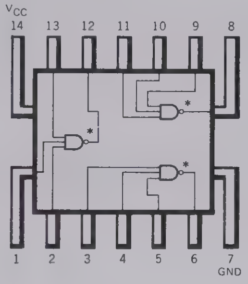
DIP (TOP VIEW)



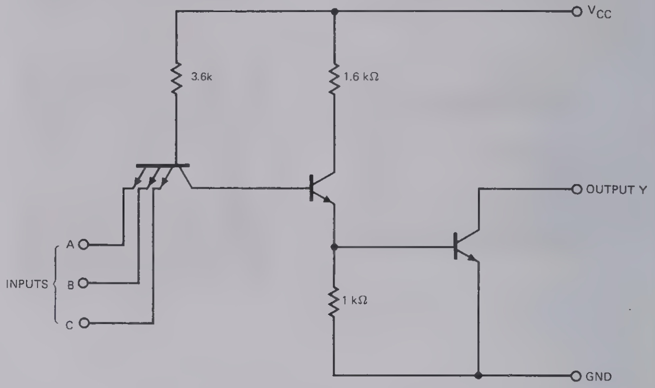
* Open collector

Positive logic: $Y = \overline{ABC}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N12XM/5412XM			9N12XC/7412XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IL} = 0.8 V		7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V (On Level)		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{CCH}	Supply Current HIGH		3.0	6.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		9.0	16.5	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay Input to Output		35	45	ns	R_L = 4 kΩ	V_{CC} = 5.0 V	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	R_L = 400Ω	C_L = 15 pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

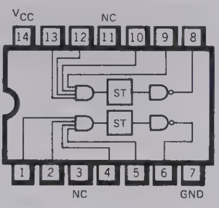
DUAL NAND SCHMITT TRIGGER

DESCRIPTION — The 9N13/5413, 7413 are dual Schmitt triggers functions, compatible with standard TTL output logic levels. Each function is essentially a 4-input NAND gate with different input threshold levels for positive and negative going signals. Typically the hysteresis , the difference between the two threshold levels, is 800 mV.

On-chip temperature compensation ensures excellent stability of the hysteresis over a wide temperature range. Typically the hysteresis changes by 3% over the range of −55°C to +125°C, the upper threshold changes by 1% over the same range. The 9N13/5413, 7413 can be triggered from slow input ramps and straight dc levels.

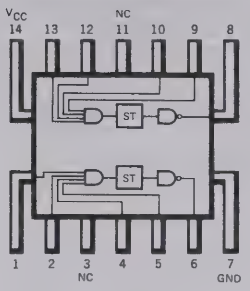
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



Positive logic: Y = $\overline{ABCD}$
NC — No internal connection

FLATPAK (TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N13XM/5413XM			9N13XC/7413XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Logic			20			20	U.L.
	LOW Logic			10			10	U.L.
Maximum Input Rise and Fall Time		No Restriction			No Restriction			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{T+}	Positive-Going Threshold Voltage	1.5	1.7	2.0	Volts	V_{CC} = 5.0 V	82
V_{T-}	Negative-Going Threshold Voltage	0.6	0.9	1.1	Volts	V_{CC} = 5.0 V	83
$V_{T+}-V_{T-}$	Hysteresis	0.4	0.8		Volts	V_{CC} = 5.0 V	82 & 83
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_I = −12 mA	85
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., V_{IN} = 0.6 V, I_{OH} = −0.8 mA	83
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., V_{IN} = 2.0 V, I_{OL} = 16 mA	82
I_{T+}	Input Current at Positive-Going Threshold		−0.65		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}	82
I_{T-}	Input Current at Negative-Going Threshold		−0.85		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}	83
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	84
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	84
I_{IL}	Input LOW Current		−1.0	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	85
I_{OS}	Output Short Circuit Current (Note 3)	−18		−55	mA	V_{CC} = MAX.	86
I_{CCH}	Supply Current HIGH		14	23	mA	V_{CC} = MAX., V_{IN} = 0V	87
I_{CCL}	Supply Current LOW		20	32	mA	V_{CC} = MAX., V_{IN} = 4.5 V	87

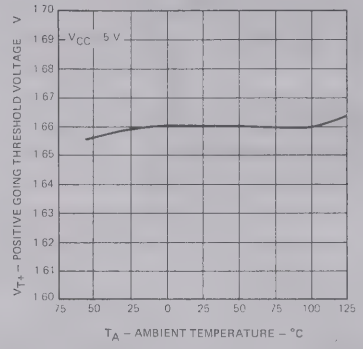
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

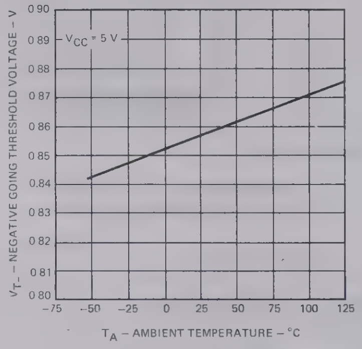
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		18	27	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 400\Omega$	M
t_{PHL}	Turn On Delay Input to Output		15	22	ns		

TYPICAL CHARACTERISTICS

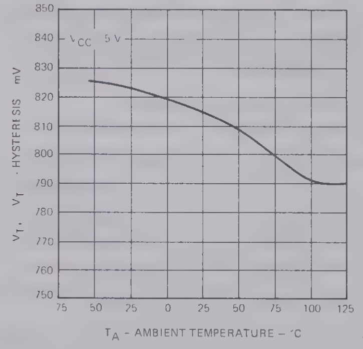
POSITIVE-GOING THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



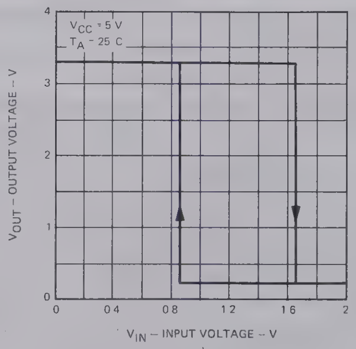
NEGATIVE-GOING THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



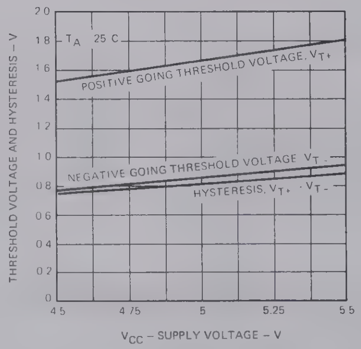
HYSTERESIS VERSUS AMBIENT TEMPERATURE



OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



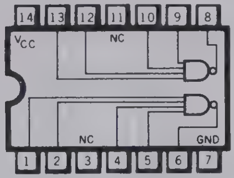
THRESHOLD VOLTAGES AND HYSTERESIS VERSUS SUPPLY VOLTAGE



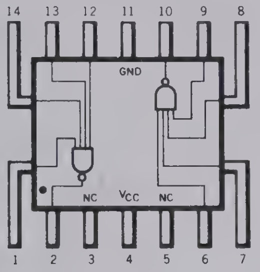
DUAL 4-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



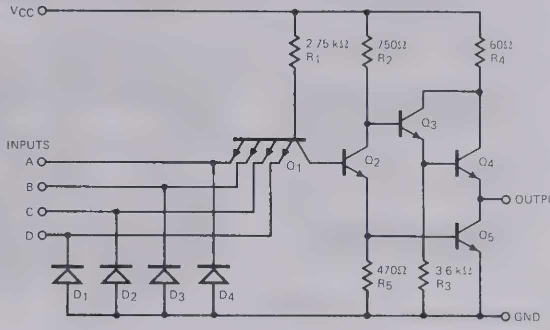
FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{ABCD}$

NC — No internal connection.

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H20XM/54H20XM			9H20XC/74H20XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatapk, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0V		1
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.		5
I_{CCH}	Supply Current HIGH		5.0	8.4	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		13	20	mA	V_{CC} = MAX., V_{IN} = 4.5 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.0	10	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		7.0	10	ns		

NOTES:

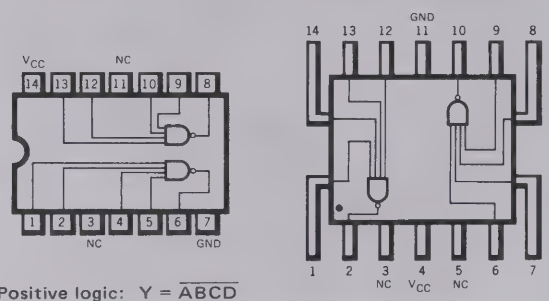
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL 4-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM



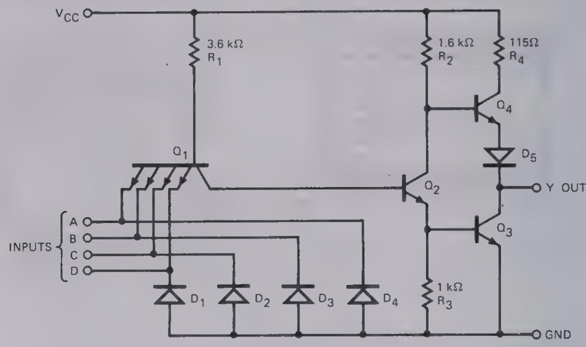
DIP (TOP VIEW)

FLATPAK (TOP VIEW)

Positive logic: Y = $\overline{ABCD}$

NC — No internal connection.

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N20XM/5420XM			9N20XC/7420XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out From Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N20/5420	V_{CC} = MAX.	5
		–18		–55	mA	9N20/7420		
I_{CCH}	Supply Current HIGH		2.0	4.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		6.0	11	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

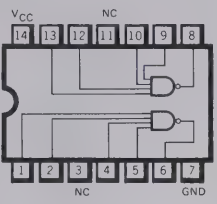
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		12	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL 4-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

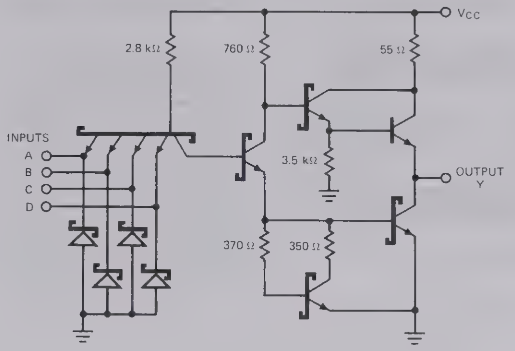


Positive logic: $Y = \overline{ABCD}$

NC—No internal connection.

SHCEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S20XM/54S20XM			9S20XC/74S20XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = -1.0mA, V_{IN} = 0.8V	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current			1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current			–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5V	Each Input
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V	
I_{CCH}	Supply Current HIGH			5.4	8.0	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW			12.6	18.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

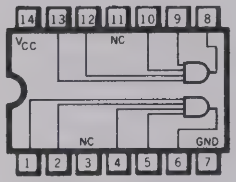
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	3.0	4.5	ns	V_{CC} = 5.0V	DD
t_{PHL}	Turn On Delay Input to Output	2.0	3.0	5.0	ns	C_L = 15pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL 4-INPUT AND GATE

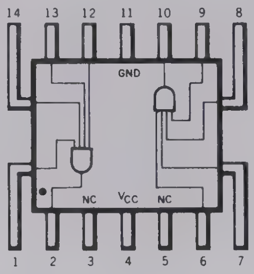
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

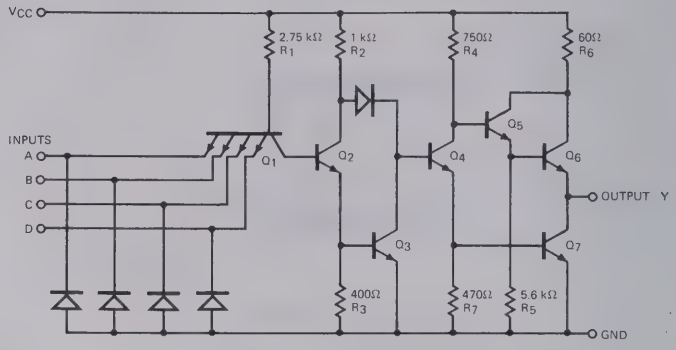


Positive logic: Y = ABCD

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.
NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H21XM/54H21XM			9H21XC/74H21XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		75
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		77
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA, V_{IN} = 2.0V		75
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 0.8 V		77
I_{IH}	Input High Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		79
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 4.5 V		80
I_{CCH}	Supply Current HIGH		12	20	mA	V_{CC} = MAX., V_{IN} = 4.5 V		81
I_{CCL}	Supply Current LOW		20	32	mA	V_{CC} = MAX., V_{IN} = 0 V		81

SWITCHING CHARACTERISTICS (T_A = 25°C)

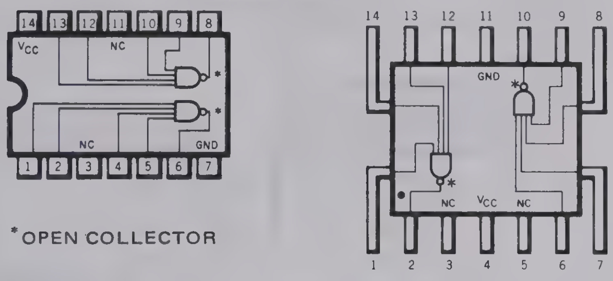
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.6	12	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		8.8	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL 4-INPUT NAND GATE (WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW) **FLATPAK** (TOP VIEW)

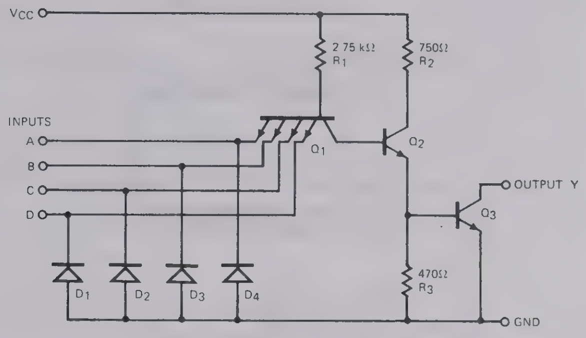


*OPEN COLLECTOR

Positive logic: Y = $\overline{ABCD}$

*OPEN COLLECTOR

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.
NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H22XM/54H22XM			9H22XC/74H22XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	7
I_{OH}	Output HIGH Current			0.25	mA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V	7
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V	1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	3
I_{CCH}	Supply Current HIGH		3.4	5.0	mA	V_{CC} = MAX., V_{IN} = 0 V	6
I_{CCL}	Supply Current LOW		26	40	mA	V_{CC} = MAX., V_{IN} = 4.5 V	6

SWITCHING CHARACTERISTICS (T_A = 25°C)

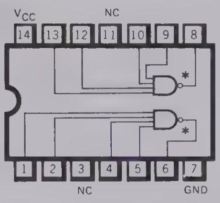
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		7.5	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

DUAL 4-INPUT NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAM

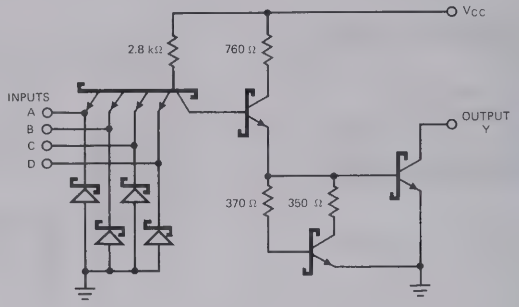
DIP (TOP VIEW)



* OPEN COLLECTOR
NC—No internal connection.
Positive logic: $Y = \overline{ABCD}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	† 9S22XM/54S22XM			9S22XC/74S22XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage		–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
I_{OH}	Output HIGH Current		0.1	250	μA	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = 0.8V	
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5V	Each Input
I_{CCH}	Supply Current HIGH		3.0	6.6	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW		12.6	18.0	mA	V_{CC} = MAX., Inputs Open	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0V	EE
t_{PHL}	Turn On Delay Input to Output	2.0	4.5	7.0	ns	C_L = 15pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.

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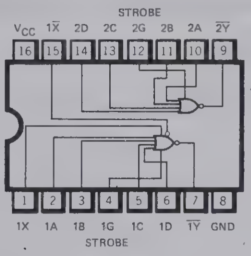
† To be announced 1972

DUAL 4-INPUT NOR GATE WITH STROBE

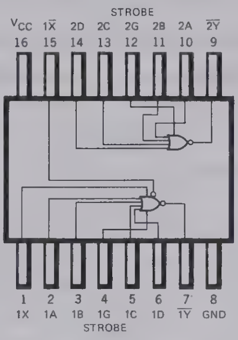
LOGIC AND CONNECTION DIAGRAM

9N23/5423, 7423

DIP (TOP VIEW)


STROBE
V_{CC} 1$\overline{X}$ 2D 2C 2G 2B 2A $\overline{2Y}$
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
1X 1A 1B 1G 1C 1D $\overline{1Y}$ GND
STROBE

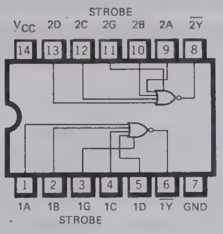
FLATPAK (TOP VIEW)


STROBE
V_{CC} 1$\overline{X}$ 2D 2C 2G 2B 2A $\overline{2Y}$
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
1X 1A 1B 1G 1C 1D $\overline{1Y}$ GND
STROBE

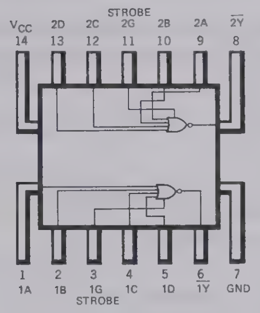
Positive logic:
$1Y = \overline{1G(1A+1B+1C+1D)+X}$
$2Y = \overline{2G(2A+2B+2C+2D)}$
X = Output of 9N60/5460, 7460

9N25/5425, 7425

DIP (TOP VIEW)

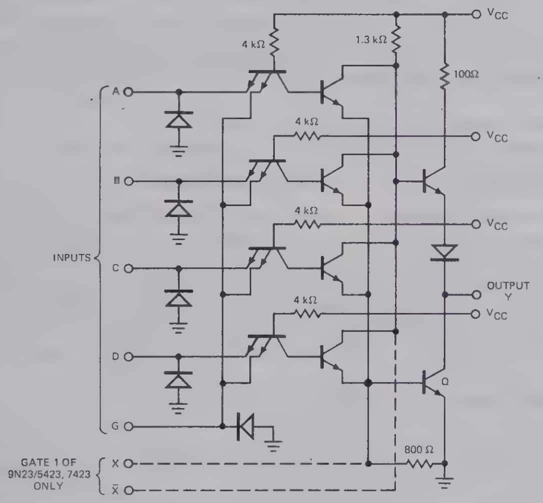

STROBE
V_{CC} 2D 2C 2G 2B 2A $\overline{2Y}$
14 13 12 11 10 9 8
1 2 3 4 5 6 7
1A 1B 1G 1C 1D $\overline{1Y}$ GND
STROBE

FLATPAK (TOP VIEW)


STROBE
V_{CC} 2D 2C 2G 2B 2A $\overline{2Y}$
14 13 12 11 10 9 8
1 2 3 4 5 6 7
1A 1B 1G 1C 1D $\overline{1Y}$ GND
STROBE

Positive logic:
$Y = \overline{G(A+B+C+D)}$

SCHEMATIC DIAGRAM
(EACH GATE)


V_{CC}
4 kΩ
1.3 kΩ
100Ω
A
B
C
D
G
INPUTS
4 kΩ
4 kΩ
4 kΩ
V_{CC}
V_{CC}
V_{CC}
OUTPUT
Y
Q
800 Ω
GATE 1 OF
9N23/5423, 7423
ONLY
X
$\overline{X}$

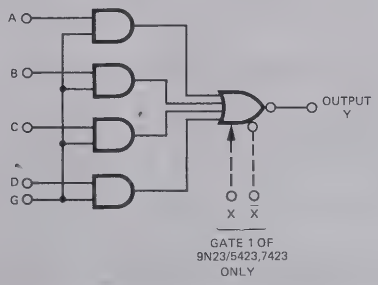
TRUTH TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

Expander inputs are open.
H = HIGH level, L = LOW level, X = irrelevant

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and $\overline{X}$ open.
(d) A total of four expander gates can be connected to the expander inputs.

LOGIC DIAGRAM
(EACH GATE)


A
B
C
D
G
OUTPUT
Y
X
$\overline{X}$
GATE 1 OF
9N23/5423,7423
ONLY

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N23XM/5423XM 9N25XM/5425XM			9N23XC/7423XC 9N25XC/7425XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC} = MIN., $I_I = -12$ mA	
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., $I_{OH} = -0.8$ mA, $V_{IL} = 0.8$ V	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., $I_{OL} = 16$ mA, $V_{IH} = 2.0$ V	
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., $V_{IN} = 5.5$ V	
I_{IH}	Input HIGH Current			40	µA	Data Inputs	V_{CC} = MAX.
				160	µA	Strobe Inputs	$V_{IN} = 2.4$ V
I_{IL}	Input LOW Current			–1.6	mA	Data Inputs	V_{CC} = MAX.
				–6.4	mA	Strobe Inputs	$V_{IN} = 0.4$ V
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	V_{CC} = MAX.	
I_{CCH}	Supply Current HIGH		8.0	16	mA	V_{CC} = MAX., All Input at 0 V	
I_{CCL}	Supply Current LOW		10	19	mA	V_{CC} = MAX., All Input at 5.0 V	

ELECTRICAL CHARACTERISTICS (9N23/5423 Circuits Only) Using Expander Inputs, $V_{CC} = 4.5$ V, $T_A = -55$°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			2.9	mA	$V_1 = 0.4$ V, $I_{OL} = 16$ mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volt	$I_{OL} = 16$ mA, $I_1 = 0.41$ mA, $R_1 = 0$	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	$I_{OH} = -400$ µA, $I_1 = 0.15$ mA, $I_2 = -0.15$ mA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	$I_{OL} = 16$ mA, $I_1 = 0.3$ mA, $R_1 = 138\Omega$	29

ELECTRICAL CHARACTERISTICS (9N23/7423 Circuits Only) Using Expander Inputs, $V_{CC} = 4.75$ V, $T_A = 0$°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			3.1	mA	$V_1 = 0.4$ V, $I_{OL} = 16$ mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volt	$I_{OL} = 16$ mA, $I_1 = 0.62$ mA, $R_1 = 0$	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	$I_{OH} = -400$ µA, $I_1 = 0.27$ mA, $I_2 = -0.27$ mA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	$I_{OL} = 16$ mA, $I_1 = 0.43$ mA, $R_1 = 130\Omega$	29

SWITCHING CHARACTERISTICS ($T_A = 25$°C) (Note 4)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 400\Omega$
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
(2) Typical limits are at $V_{CC} = 5.0$ V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Switching characteristics of the 9N23/5423, 7423 are tested with the expander pins open.

LPTTL/SSI 9L24

LOW POWER DUAL J$\overline{K}$ (OR D) FLIP-FLOP

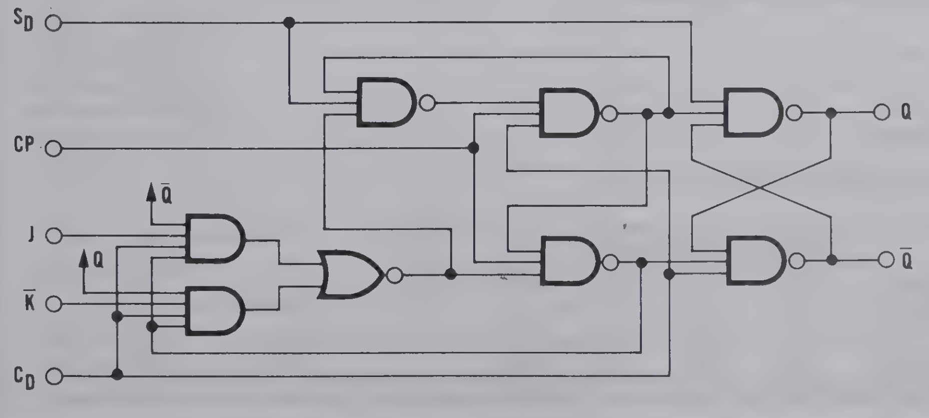
DESCRIPTION – The Low Power TTL/SSI 9L24 consists of two completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform.. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

- DUAL RANK TYPE CIRCUIT
- SEPARATE CLOCKS
- SEPARATE ASYNCHRONOUS SET AND CLEAR INPUTS
- 10 MHz TYPICAL TOGGLE FREQUENCY
- TYPICAL POWER DISSIPATION OF 30mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

PIN NAMES		LOADING	
		HIGH	LOW
$J, J_1, \overline{K}, \overline{K}_1$	Flip-Flop Inputs	0.5 U.L.	0.25 U.L.
$\overline{S}_D, \overline{S}_{D1}$	Set Inputs	1.0 U.L.	0.5 U.L.
$\overline{C}_D, \overline{C}_{D1}$	Clear Inputs	2.0 U.L.	0.75 U.L.
CP, CP_1	Clock Inputs	1.0 U.L.	0.5 U.L.
$Q, \overline{Q}, Q_1, \overline{Q}_1$	Flip-Flop Outputs	10 U.L.	2.5 U.L.

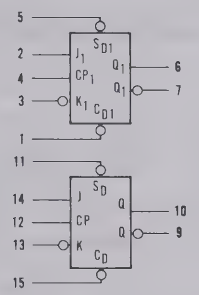
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM



SD
CP
J
K
CD
Q
Q
Q
Q

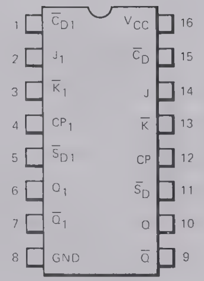
LOGIC SYMBOL



5
2
4
3
1
J1
CP1
K1
SD1
CD1
Q1
Q1
6
7
11
14
12
13
15
J
CP
K
SD
CD
Q
Q
10
9

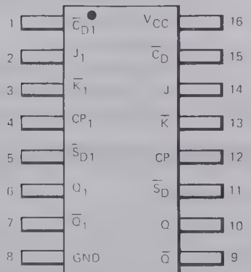
V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 CD1
2 J1
3 K1
4 CP1
5 SD1
6 Q1
7 Q1
8 GND
16 VCC
15 CD
14 J
13 K
12 CP
11 SD
10 Q
9 Q

FLATPAK (TOP VIEW)



1 CD1
2 J1
3 K1
4 CP1
5 SD1
6 Q1
7 Q1
8 GND
16 VCC
15 CD
14 J
13 K
12 CP
11 SD
10 Q
9 Q

TRUTH TABLES

SYNCHRONOUS ENTRY J–K̄ MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

t_n = before clock
t_{n+1} = after clock

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

J & $\overline{K}$ inputs connected together

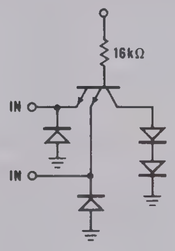
ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
$\overline{S}_D$ 5(11)	$\overline{C}_D$ 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

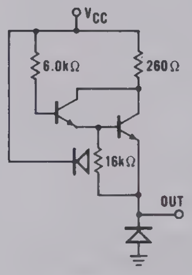
L = LOW Logic Level, H = HIGH Logic Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

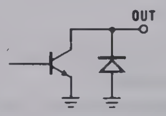
EQUIVALENT INPUT CIRCUIT



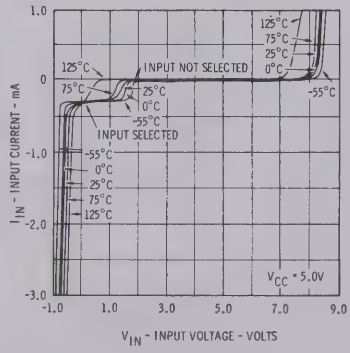
OUTPUT HIGH EQUIVALENT CIRCUIT



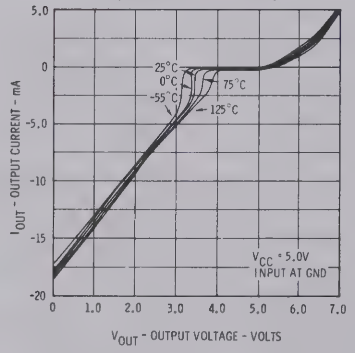
OUTPUT LOW EQUIVALENT CIRCUIT



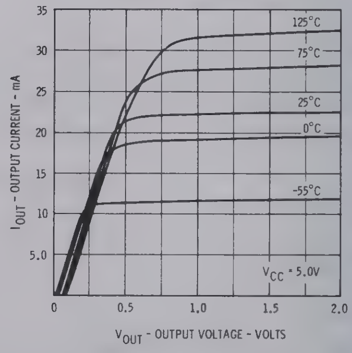
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L24XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9L24XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for all Inputs.
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for all Inputs.
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.3 V.
	J, $\overline{K}$		–0.25	–0.4		
	CP, $\overline{S}_D$		–0.50	–0.8		
	$\overline{C}_D$ (Note 3)		–0.75	–1.2		
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V.
	J, $\overline{K}$		2	20		
	CP, $\overline{S}_D$		4	40		
	$\overline{C}_D$		8	80		
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V.
I_{SC} (Note 5)	Output Short Circuit Current	–10	–22	–40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V.
I_{CC}	Power Supply Current		6.0	8.8	mA	V_{CC} = MAX.

NOTES:

(1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(2) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(3) Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, $\overline{K}$ = Logic HIGH and $\overline{S}_D$ = Logic LOW.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

(5) Not more than one output should be shorted at a time.

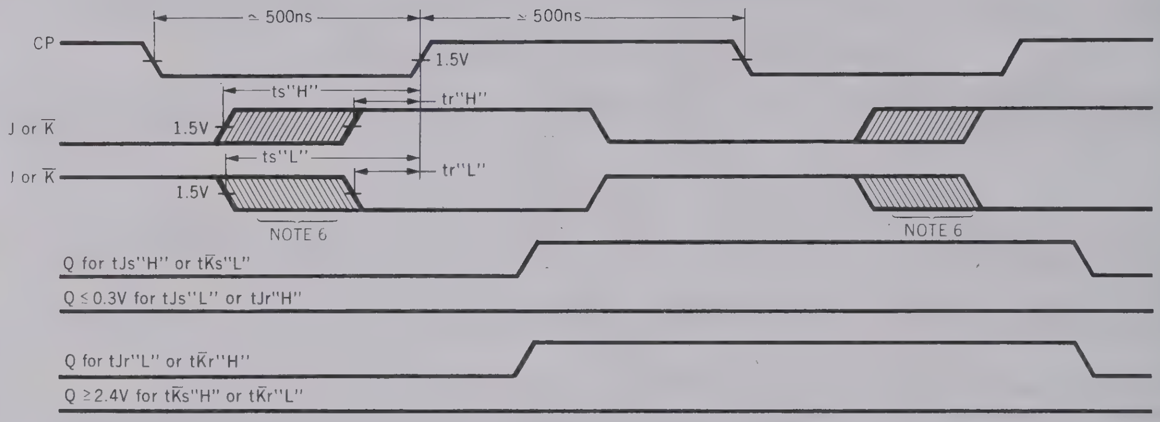
SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF)

PARAMETER		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH}	(CP to Q)		40		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V
	(CP to $\overline{Q}$)		40			Fig. 2
t_{PHL}	(CP to Q)		60		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V
	(CP to $\overline{Q}$)		60			Fig. 2
t_{PLH}	(S_D to Q)		14		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V
	(C_D to $\overline{Q}$)		14			Fig 3
t_{PHL}	(S_D to $\overline{Q}$)		50		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V
	(C_D to Q)		40			Fig. 3
t_s "H"	(J to CP)		20		ns	$\overline{K}$ ≤ 0.3 V
t_r "H"	(J to CP)		20			Fig. 1
t_s "H"	($\overline{K}$ to CP)		1.0		ns	J ≥ 2.4 V
t_r "H"	($\overline{K}$ to CP)		1.0			Fig. 1
t_s "L"	(J to CP)		–2.0		ns	$\overline{K}$ ≤ 0.3 V
t_r "L"	(J to CP)		–2.0			Fig. 1
t_s "L"	($\overline{K}$ to CP)		9.0		ns	J ≥ 2.4 V
t_r "L"	($\overline{K}$ to CP)		9.0			Fig. 1
t_{pw} "H"	(Clock Pulse Width)		40		ns	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V
t_{pw} "L"	(S_D Pulse Width)		50			
t_{pw} "L"	(C_D Pulse Width)		40			
Toggle Frequency			10		MHz	J ≥ 2.4 V, $\overline{K}$ ≤ 0.3 V

SET UP TIME – t_s is defined as the time required for the new logic level to be present at the J or $\overline{K}$ inputs prior to the clock transition from LOW to HIGH in order for the flip-flop to respond to the new $J\overline{K}$ mode.

RELEASE TIME – t_r is defined as the time allowed for a new logic level to be present at the J or $\overline{K}$ inputs prior to the clock transition from LOW to HIGH in order for the flip-flop not to respond to the new $J\overline{K}$ mode. A negative Release Time means the new logic level must not occur until after the clock transition.

SET UP AND RELEASE WAVEFORMS


≃ 500ns
≃ 500ns
CP
1.5V
ts"H"
tr"H"
J or K̄
1.5V
ts"L"
tr"L"
J or K̄
1.5V
NOTE 6
NOTE 6
Q for tJs"H" or tK̄s"L"
Q ≤ 0.3V for tJs"L" or tJr"H"
Q for tJr"L" or tK̄r"H"
Q ≥ 2.4V for tK̄s"H" or tK̄r"L"

Note (6) FORBIDDEN ZONE, if data changes during the shaded time, the state of the outputs cannot be predetermined.

FIG.1

SWITCHING WAVEFORMS

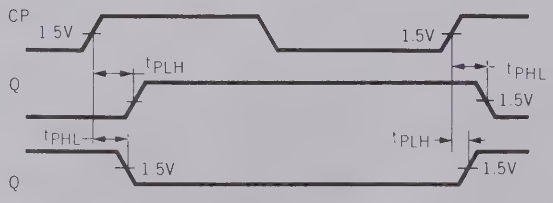

CP
1.5V
1.5V
Q
tPLH
tPHL
1.5V
tPHL
tPLH
Q
1.5V
1.5V

FIG.2

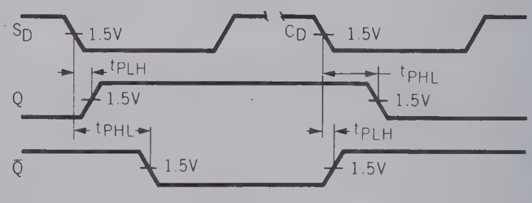

SD
1.5V
CD
1.5V
tPLH
tPHL
Q
1.5V
1.5V
tPHL
tPLH
Q̄
1.5V
1.5V

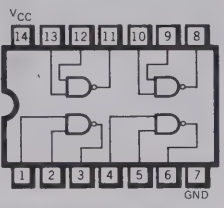
FIG.3

QUAD 2-INPUT HIGH VOLTAGE INTERFACE NAND GATE

DESCRIPTION — These open-collector NAND gates feature high output voltage ratings for interfacing with low threshold voltage MOS logic circuits or other 12V systems. Although the output is rated to withstand 15V, the V_{CC} terminal is connected to the standard 5V source. The output transistor will sink 16 mA while maintaining a low-level output voltage of 0.4V maximum thus providing a high fan out driver with the nominal power dissipation standard Series 9N/54, 74 gates.

LOGIC AND CONNECTION DIAGRAM

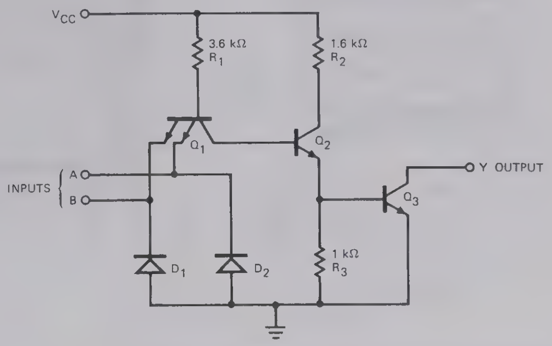
DIP (TOP VIEW)



Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N26XM/5426XM			9N26XC/7426XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Output Voltage, V_{OH}			15			15	Volts
LOW Level Output Current, I_{OL}			16			16	mA
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		88
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		89
V_{OH}	Output HIGH Voltage	15			Volts	V_{CC} = MIN., V_{IL} = 0.8 V, I_{OH} = 1.0 mA		89
I_{OH}	Output HIGH Current			50	µA	V_{CC} = MIN., V_{IL} = 0.8 V, V_{OH} = 12 V		89
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V		88
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	90
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		91
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V		92
I_{CCL}	Supply Current LOW		12	22	mA	V_{CC} = MAX., V_{IN} = 5.0 V		92

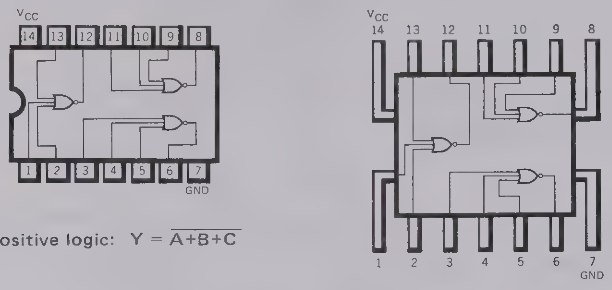
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		16	24	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 1.0 kΩ	N
t_{PHL}	Turn On Delay Input to Output		11	17	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

TRIPLE 3-INPUT NOR GATE

LOGIC AND CONNECTION DIAGRAM

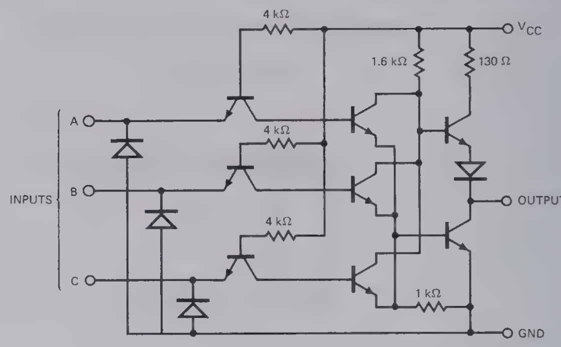


DIP (TOP VIEW)

FLATPAK (TOP VIEW)

Positive logic: $Y = \overline{A+B+C}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N27XM/5427XM			9N27XC/7427XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC} = MIN., I_I = –12 mA	
V_{OH}	Output HIGH Voltage	2.4	3.3			V_{CC} = MIN., I_{OH} = –0.8 mA, V_{IL} = 0.8 V	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V	
I_I	Input Current at Max. Input Vol.			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N27/5427	V_{CC} = MAX.
		–18		–55	mA	9N27/7427	
I_{CCH}	Supply Current HIGH		10	16	mA	V_{CC} = MAX., (Note 4)	
I_{CCL}	Supply Current LOW		16	26	mA	V_{CC} = MAX., (Note 5)	

SWITCHING CHARACTERISTICS (T_A = 25°C)

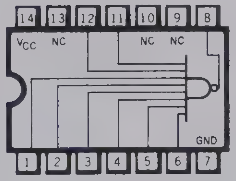
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω
t_{PHL}	Turn On Delay Input to Output		7.0	11	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Measured with all inputs grounded, and outputs open.
(5) Measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.

8-INPUT NAND GATE

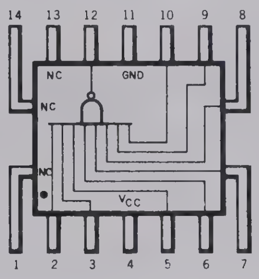
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

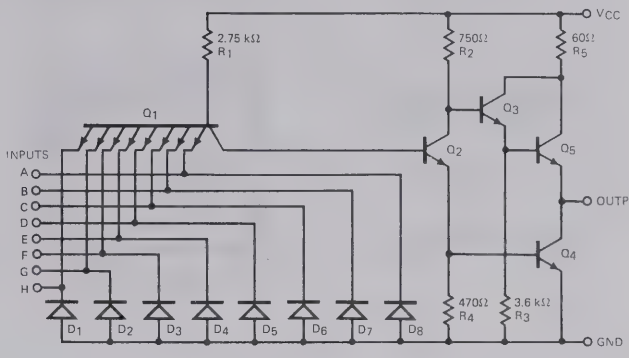


Positive logic: $Y = \overline{ABCDEFGH}$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.
NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H30XM/54H30XM			9H30XC/74H30XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0V		1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.		5
I_{CCH}	Supply Current HIGH		2.5	4.2	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		6.5	10	mA	V_{CC} = MAX., V_{IN} = 4.5 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

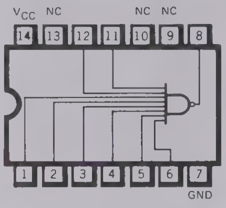
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.8	10	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		8.9	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

8-INPUT NAND GATE

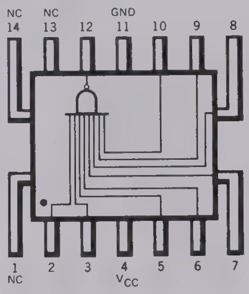
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



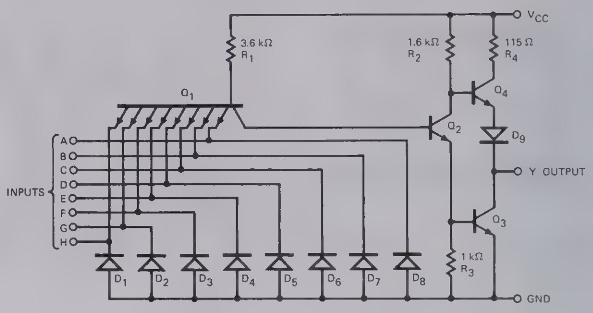
Positive logic: $Y = \overline{ABCDEFGH}$

FLATPAK (TOP VIEW)



NC — No internal connection.

SCHEMATIC DIAGRAM



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N30XM/5430XM			9N30XC/7430XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N30/5430	V_{CC} = MAX.	5
		−18		−55	mA	9N30/7430		
I_{CCH}	Supply Current HIGH		1.0	2.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		3.0	6.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

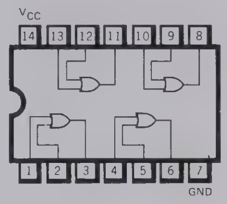
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

QUAD 2-INPUT OR GATE

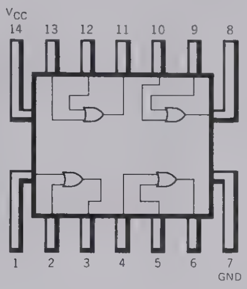
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

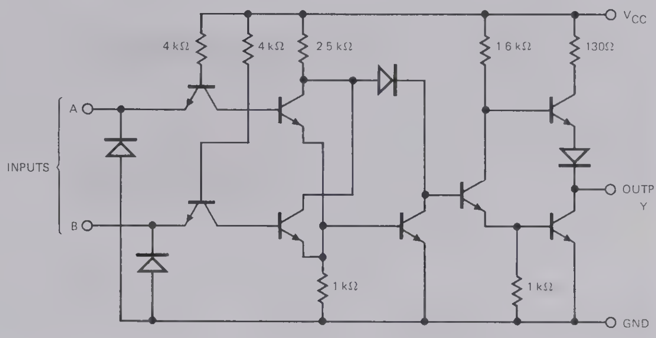


Positive logic: Y = A+B

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N32XM/5432XM			9N32XC/7432XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC} = MAX., I_I = –12 mA	
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.8 mA, V_{IH} = 2.0 V	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IL} = 0.8 V	
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	
I_{IL}	Input LOW Current			–16	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N32/5432	V_{CC} = MAX.
		–18		–55	mA	9N32/7432	
I_{CCH}	Supply Current HIGH		15	22	mA	V_{CC} = MAX., (Note 4)	
I_{CCL}	Supply Current LOW		23	38	mA	V_{CC} = MAX., (Note 5)	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω
t_{PHL}	Turn On Delay Input to Output		14	22	ns	

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time.

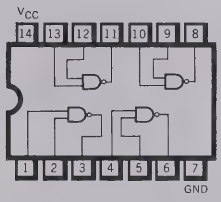
(4) Measured with one input of each gate at 4.5 V, the remaining inputs grounded and outputs open.

(5) Measured with both inputs of all gates grounded, and outputs open.

QUAD 2-INPUT NAND BUFFER

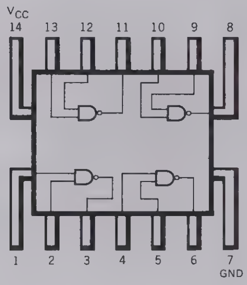
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)


VCC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
GND

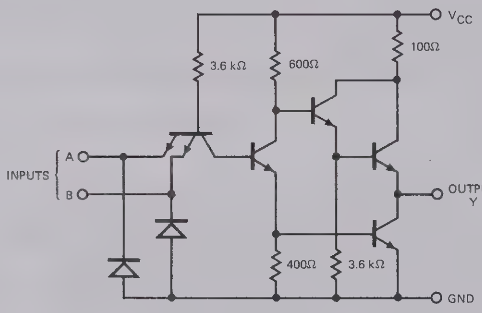
Positive logic: $Y = \overline{AB}$

FLATPAK (TOP VIEW)

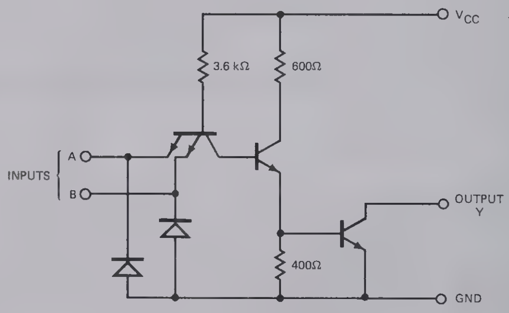

VCC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
GND

SCHEMATIC DIAGRAM
(EACH BUFFER)

9N37/5437, 7437
(TOTEM-POLE OUTPUT)


VCC
100Ω
3.6 kΩ
600Ω
INPUTS
A
B
OUTPUT
Y
400Ω
3.6 kΩ
GND

9N38/5438, 7438
(OPEN-COLLECTOR OUTPUT)


VCC
3.6 kΩ
600Ω
INPUTS
A
B
OUTPUT
Y
400Ω
GND

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N37XM/5437XM 9N38XM/5438XM			9N37XC/7437XC 9N38XC/7438XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			30			30	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

9N37/5437, 7437

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC} = MIN., I_I = –12 mA
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –1.2 mA, V_{IL} = 0.8 V
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 48 mA, V_{IH} = 2.0 V
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)	–20		–70	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCH}	Supply Current HIGH		9.0	15.5	mA	V_{CC} = MAX., All Inputs at 0 V
I_{CCL}	Supply Current LOW		34	54	mA	V_{CC} = MAX., All Inputs at 5.0 V

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 133Ω
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns	

9N38/5438, 7438

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC} = MIN., I_I = –12 mA
I_{OH}	Output HIGH Current			250	μA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IL} = 0.8 V
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 48 mA, V_{IH} = 2.0 V
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH		5.0	8.5	mA	V_{CC} = MAX., All Inputs at 0 V
I_{CCL}	Supply Current LOW		34	54	mA	V_{CC} = MAX., All Inputs at 5.0 V

SWITCHING CHARACTERISTICS (T_A = 25°C)

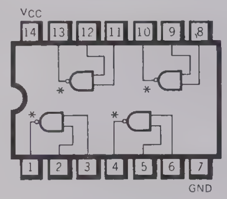
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		14	22	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 133Ω
t_{PHL}	Turn On Delay Input to Output		11	18	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

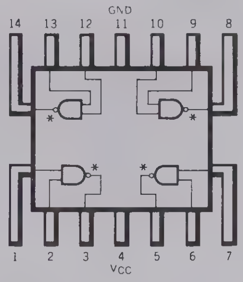
QUAD 2-INPUT NAND BUFFER (WITH OPEN COLLECTOR OUTPUT)

LOGIC AND CONNECTION DIAGRAMS

DIP (TOP VIEW) **FLATPAK** (TOP VIEW)

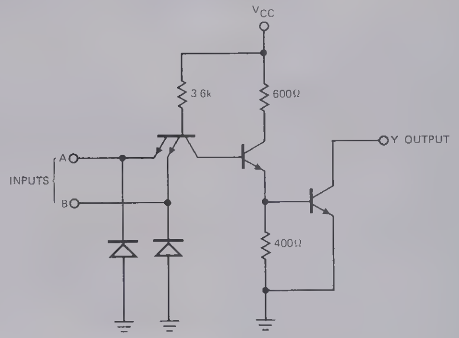


Positive logic: $Y = \overline{AB}$



*Open Collector

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N39XM/5439XM			9N39XC/7439XC			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating free-air temperature range	–55	25	125	0	25	70	°C
Normalized fan out from each output, N			30			30	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN	TYP (Note 2)	MAX	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	7
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC} = MIN., I_I = –12 mA, Other Input OPEN	85
I_{OH}	Output HIGH Current			250	µA	V_{OH} = 5.5 V, V_{IL} = 0.8 V, V_{CC} = MIN., Other input = V_{CC}	7
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 48 mA; V_{CC} = MIN., V_{IN} = 2.0 V, Other input = 2.0V	1
				0.5	Volts	I_{OL} = 60 mA	
	9N39/7439			0.6	Volts	I_{OL} = 80 mA	
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V Other Input = 0 V	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V Other Input = 0 V	
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V Other Input = 4.5 V	3
I_{CCH}	Supply Current HIGH		5.0	8.5	mA	V_{CC} = MAX., All Inputs = 0 V	6
I_{CCL}	Supply Current LOW		34	54	mA	V_{CC} = MAX., All Inputs = 5.0 V	6

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output		14	22	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 133Ω	A
t_{PHL}	Turn On Delay Input to Output		12	18	ns		

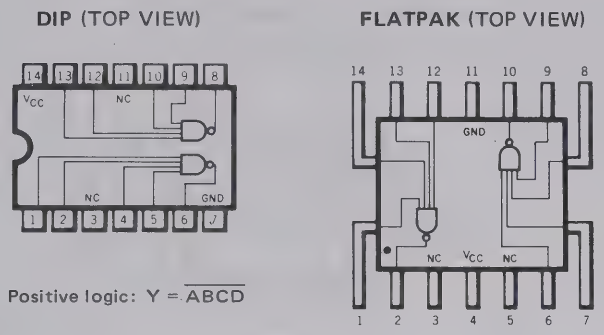
NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

DUAL 4-INPUT NAND BUFFER

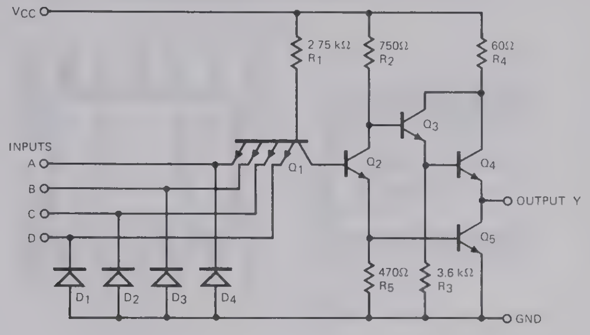
LOGIC AND CONNECTION DIAGRAM



DIP (TOP VIEW) **FLATPAK** (TOP VIEW)

Positive logic: $Y = \overline{ABCD}$

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.
NC — No internal connection

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H40XM/54H40XM			9H40XC/74H40XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Fan Out from Each Output			37.5			37.5	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –1.5 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 60 mA, V_{IN} = 2.0V		1
I_{IH}	Input HIGH Current			100	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	–40		–125	mA	V_{CC} = MAX.		5
I_{CCH}	Supply Current HIGH		10.4	16	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		25	40	mA	V_{CC} = MAX., V_{IN} = 4.5 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

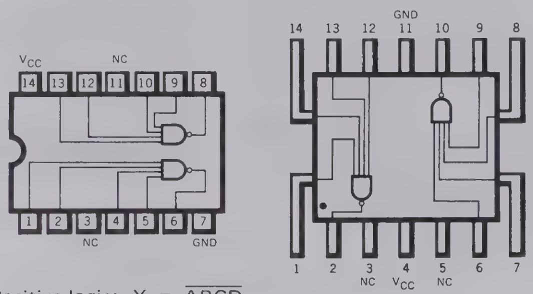
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.5	12	ns	V_{CC} = 5.0V C_L = 25 pF R_L = 93Ω	T
t_{PHL}	Turn On Delay Input to Output		8.5	12	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL 4-INPUT NAND BUFFER

LOGIC AND CONNECTION DIAGRAM

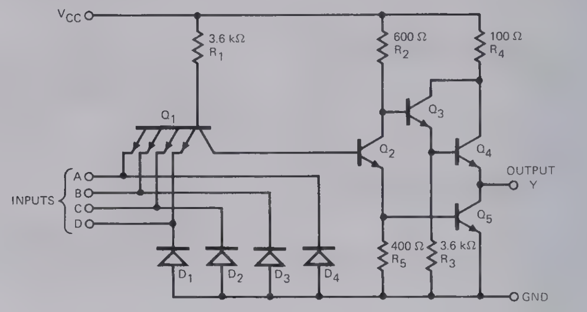
DIP (TOP VIEW) **FLATPAK** (TOP VIEW)



Positive logic: $Y = \overline{ABCD}$

NC — No internal connection.

SCHEMATIC DIAGRAM
(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N40XM/5450XM			9N40XC/7440XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			30			30	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –1.2 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.28	0.4	Volts	V_{CC} = MIN., I_{OL} = 48 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	–20		–70	mA	9N40/5440	V_{CC} = MAX.	5
		–18		–70	mA	9N40/7440		
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		17	27	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

SWITCHING CHARACTERISTICS (T_A = 25°C)

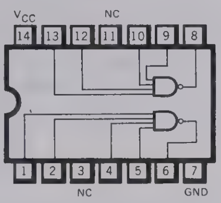
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 133 Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL 4-INPUT NAND BUFFER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

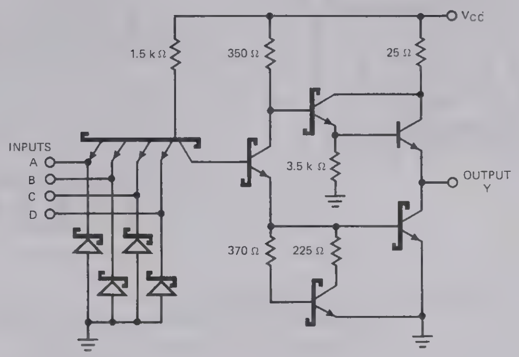


NC—No internal connection.

Positive logic: $Y = \overline{ABCD}$

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S40XM/54S40XM			9S40XC/74S40XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C
Fan Out From Each Output			37.5*			37.5*	U.L.

*37.5 (U.L.) is the LOW drive factor and 75 (U.L.) is the HIGH drive factor.
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = -3.0mA, V_{IN} = 0.8V	
		XC	2.7	3.4				
V_{OL}	Output LOW Voltage			0.4	0.5	Volts	V_{CC} = MIN., I_{OL} = 60mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current			1.0	100	µA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current			−2.5	−4.0	mA	V_{CC} = MAX., V_{IN} = 0.5V	Each Input
I_{OS}	Output Short Circuit Current (Note 3)		−50	−150	−225	mA	V_{CC} = MAX., V_{OUT} = 0V	
I_{CCH}	Supply Current HIGH			8.2	18.0	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW			27.2	44.0	mA	V_{CC} = MAX., Inputs Open	

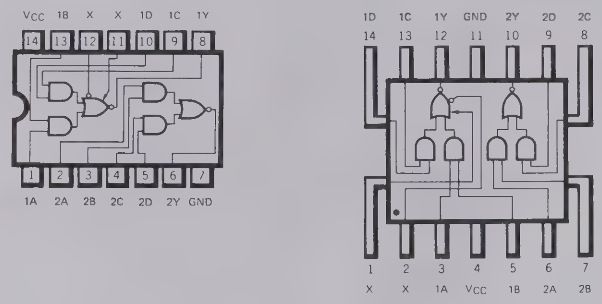
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	4.0	6.5	ns	V_{CC} = 5.0V	DD
t_{PHL}	Turn On Delay Input to Output	2.0	4.0	6.5	ns	C_L = 50pF	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

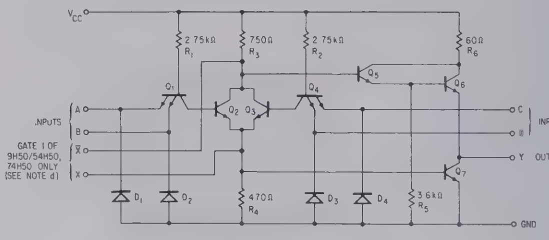
LOGIC AND CONNECTION DIAGRAM


DIP (TOP VIEW)

FLATPAK (TOP VIEW)

VCC 1B X X 1D 1C 1Y
14 13 12 11 10 9 8
1 2 3 4 5 6 7
1A 2A 2B 2C 2D 2Y GND
1D 1C 1Y GND 2Y 2D 2C
14 13 12 11 10 9 8
1 2 3 4 5 6 7
X X 1A VCC 1B 2A 2B

SCHEMATIC DIAGRAM
(EACH GATE)


VCC
2.75kΩ R1
750Ω R3
2.75kΩ R2
60Ω R6
Q1
Q2 Q3
Q4
Q5
Q6
Q7
INPUTS
A
B
GATE 1 OF 9H50/54H50, 74H50 ONLY (SEE NOTE d)
X̄
X
C
D
INPUTS
Y OUTPUT
D1
D2
470Ω R4
D3
D4
3.6kΩ R5
GND

Positive logic: $Y = \overline{(AB) + (CD) + (X)}$
(X = Output of 9H60/54H60, 74H60 or
9H62/54H62, 74H62)

NOTES:
- (a) Component values shown are typical.
- (b) Both expander inputs are used simultaneously for expanding.
- (c) If expander is not used leave X and $\overline{X}$ pins open.
- (d) Expander inputs X and $\overline{X}$ are functional on the 9H50/54H50, 74H50 circuits only. Make no external connection to X and $\overline{X}$ pins of the 9H51/54H51, 74H51.
- (e) A total of four 9H60/54H60, 74H60 expander gates or one 9H62/54H62, 74H62 expander gate may be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H50XM/54H50XM 9H51XM/54H51XM			9H50XC/74H50XC 9H51XC/74H51XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage		21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage		22
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA, V_{IN} = 0.8 V		22
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V		21
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		23
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.		25
I_{CCH}	Supply Current HIGH		8.2	12.8	mA	V_{CC} = MAX., V_{IN} = 0 V		27
I_{CCL}	Supply Current LOW		15.2	24	mA	V_{CC} = MAX., V_{IN} = 4.5 V		26

NOTES:
- (1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
- (2) Typical limits are at V_{CC} = 5.0 V, 25°C.
- (3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
- (4) Required at both input terminals of either AND section to ensure LOW level at output.
- (5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS (9H50/54H50 Circuits Only) Using Expander Inputs, V_{CC} = 4.5 V, T_A = –55°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\overline{X}}$	Expander-Node Input Current			–5.85	mA	$V_{\overline{X}}$ = 1.4 V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 20 mA, I_1 = 700 μA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4			Volts	I_{OH} = –500 μA, I_1 = 320 μA, I_2 = –320 μA	30
V_{OL}	Output LOW Voltage			0.4	Volts	I_{OL} = 20 mA, I_1 = 470 μA, R_1 = 68Ω	29

ELECTRICAL CHARACTERISTICS (9H50/74H50 Circuits Only) Using Expander Inputs, V_{CC} = 4.75 V, T_A = 0°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\overline{X}}$	Expander-Node Input Current			–6.3	mA	$V_{\overline{X}}$ = 1.4 V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 20 mA, I_1 = 1.1 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4			Volts	I_{OH} = –500 μA, I_1 = 570 μA, I_2 = –570 μA	30
V_{OL}	Output LOW Voltage			0.4	Volts	I_{OL} = 20 mA, I_1 = 600 μA, R_1 = 63Ω	29

SWITCHING CHARACTERISTICS, Expander Pins are Open (T_A = 25°C)

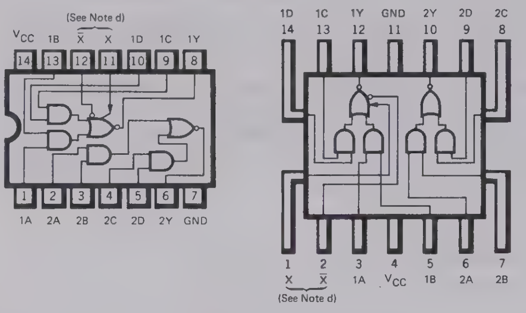
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		6.8	11	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	T
t_{PHL}	Turn On Delay Input to Output		6.2	11	ns		

SWITCHING CHARACTERISTICS (9H50/54H50, 74H50 Circuits Only) (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		11		ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω *C_X = 15 pF	U *MM & NN
t_{PHL}	Turn On Delay Input to Output		7.4		ns		

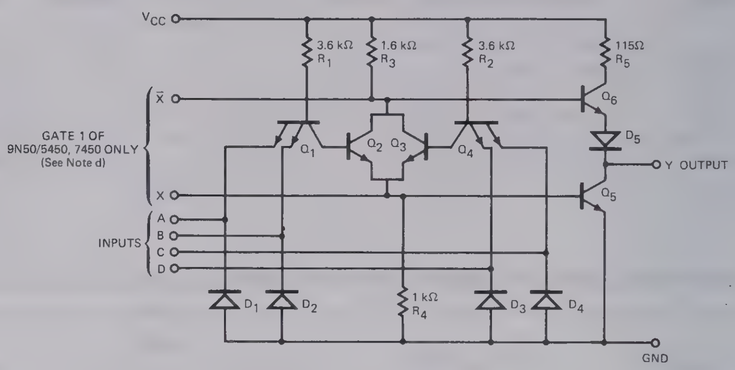
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM


(See Note d)
VCC 1B X̄ X 1D 1C 1Y
14 13 12 11 10 9 8
1 2 3 4 5 6 7
1A 2A 2B 2C 2D 2Y GND
1D 1C 1Y GND 2Y 2D 2C
14 13 12 11 10 9 8
1 2 3 4 5 6 7
X X̄ 1A VCC 1B 2A 2B
(See Note d)

DIP (TOP VIEW) **FLATPAK** (TOP VIEW)

SCHEMATIC DIAGRAM (EACH GATE)


VCC
3.6 kΩ R1
1.6 kΩ R3
3.6 kΩ R2
115Ω R5
X̄
Q6
GATE 1 OF 9N50/5450, 7450 ONLY (See Note d)
Q1
Q2 Q3
Q4
D5
Y OUTPUT
X
Q5
INPUTS
A
B
C
D
1 kΩ R4
D1 D2 D3 D4
GND

Positive logic: $Y = \overline{(AB) + (CD) + (X)}$
(X = Output of 9N60/5460, 7460)

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and X̄ pins open.
(d) Make no external connection to X and X̄ pins of the 9N51/5451, 7451.
(e) A total of four expander gates can be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N50XM/5450XM 9N51XM/5451XM			9N50XC/7450XC 9N51XC/7451XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage		21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage		22
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = 0.8 V		22
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		21
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		23
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N50/5450; 9N51/5451	V_{CC} = MAX.	25
		−18		−55	mA	9N50/7450; 9N51/7451		
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V		26
I_{CCL}	Supply Current LOW		7.4	14	mA	V_{CC} = MAX., V_{IN} = 5.0 V		27

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and X̄ are open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Required at both input terminals of either AND section to ensure LOW level at output..
(5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS (9N50/5450 CIRCUITS), Using Expander Inputs, $V_{CC} = 4.5$ V, $T_A = -55°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			2.9	mA	$V_1 = 0.4$ V, $I_{OL} = 16$ mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	$I_{OL} = 16$ mA, $I_1 = 0.41$ mA, $R_1 = 0\Omega$	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	$I_{OH} = -400\ \mu A$, $I_1 = 0.15$ mA, $I_2 = -0.15$ mA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	$I_{OL} = 16$ mA, $I_1 = 0.3$ mA, $R_1 = 138\Omega$	29

ELECTRICAL CHARACTERISTICS (9N50/7450 CIRCUITS), Using Expander Inputs, $V_{CC} = 4.75$ V, $T_A = 0°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			3.1	mA	$V_1 = 0.4$ V, $I_{OL} = 16$ mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	$I_{OL} = 16$ mA, $I_1 = 0.62$ mA, $R_1 = 0\Omega$	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	$I_{OH} = -400\ \mu A$, $I_1 = 270\ \mu A$, $I_2 = -270\ \mu A$	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	$I_{OL} = 16$ mA, $I_1 = 0.43$ mA, $R_1 = 130\Omega$	29

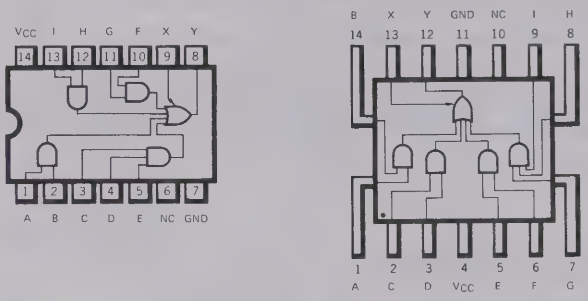
SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 400\Omega$	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

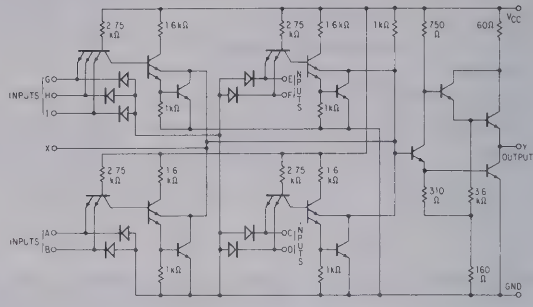
EXPANDABLE 2-2-2-3-INPUT AND-OR GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW) **FLATPAK** (TOP VIEW)



SCHEMATIC DIAGRAM



Positive logic:

Y = (AB) + (CDE) + (FG) + (HI) + (X)

Positive logic:

Y = (AB) + (CD) + (EF) + (GHI) + (X)

(X = Output of 9H61/54H61, 74H61)

NOTES:
(a) Component values shown are typical.
(b) A total of six expander gates may be connected to the expander input X.
(c) NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H52XM/54H52XM			9H52XC/74H52XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage	105
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage	106
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA, V_{IN} = 2.0 V	105
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 0.8 V	106
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	108
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V, Each Input	
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	107
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 4.5 V	109
I_{CCH}	Supply Current HIGH		20	31	mA	V_{CC} = MAX., V_{IN} = 4.5 V	110
I_{CCL}	Supply Current LOW		15.2	24	mA	V_{CC} = MAX., V_{IN} = 0V	110

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pin is open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Duration of short-circuit test should not exceed 1 second.
(4) Required at all input terminals of one AND section to ensure HIGH level at output.
(5) Required at one input terminal of each AND section to ensure LOW level at output.

ELECTRICAL CHARACTERISTICS (9H52/54H52 Circuits Only) Using Expander Inputs, $V_{CC} = 4.5$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_{INX}	Expander-Node Input Current	–2.7		–4.5	mA	$V_X = 1.0$ V, $I_{OH} = -500$ µA, $T_A = -55°$C	111
V_{OH}	Output HIGH Voltage	2.4			Volts		
V_{OL}	Output LOW Voltage			0.4	Volts	$I_{INX} = -300$ µA, $I_{OL} = 20$ mA, $T_A = 125°$C	112

ELECTRICAL CHARACTERISTICS (9H52/74H52 Circuits Only) Using Expander Inputs, $V_{CC} = 4.75$ V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_{INX}	Expander-Node Input Current	–2.9		–5.35	mA	$V_X = 1.0$ V, $I_{OH} = -500$ µA, $T_A = 0°$C	111
V_{OH}	Output HIGH Voltage	2.4			Volts		
V_{OL}	Output LOW Voltage			0.4	Volts	$I_{INX} = -300$ µA, $I_{OL} = 20$ mA, $T_A = 70°$C	112

SWITCHING CHARACTERISTICS, Expander Pin is Open ($T_A = 25°$C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		10.6	15	ns	$V_{CC} = 5.0$ V $C_L = 25$ pF $R_L = 280\Omega$	T
t_{PHL}	Turn On Delay Input to Output		9.2	15	ns		

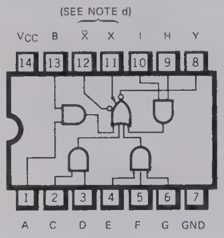
SWITCHING CHARACTERISTICS ($T_A = 25°$C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		14.8		ns	$V_{CC} = 5.0$ V $C_L = 25$ pF $R_L = 280\Omega$ $^*C_X = 15$ pF	V *MM & NN
t_{PHL}	Turn On Delay Input to Output		9.8		ns		

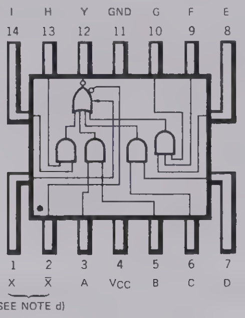
EXPANDABLE 2-2-2-3 INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM

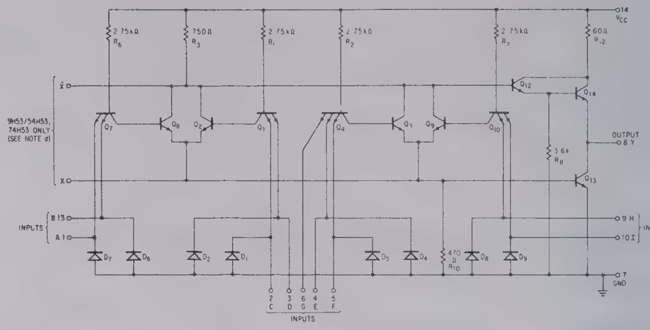
DIP (TOP VIEW)


(SEE NOTE d)
VCC B X̄ X I H Y
14 13 12 11 10 9 8
1 2 3 4 5 6 7
A C D E F G GND

FLATPAK (TOP VIEW)


I H Y GND G F E
14 13 12 11 10 9 8
1 2 3 4 5 6 7
X X̄ A VCC B C D
(SEE NOTE d)

SCHEMATIC DIAGRAM


14 VCC
2.75kΩ R6
750Ω R3
2.75kΩ R1
2.75kΩ R2
2.75kΩ R7
60Ω R12
X̄
X
9H53/54H53, 74H53 ONLY (SEE NOTE d)
Q7 Q8 Q2 Q1 Q4 Q3 Q9 Q10 Q12 Q14 Q13
3.6k R8
OUTPUT 8 Y
INPUTS B 13 A 1
D7 D6 D2 D1 D5 D4 D8 D9
470 Ω R10
9 H
10 I
INPUTS
7 GND
2 C 3 D 6 G 4 E 5 F
INPUTS

Positive logic: $Y = \overline{(AB) + (CD) + (EFG) + (HI)\ E\ (X)}$
(X = Output of 9H60/54H60, 74H60 or
9H62/54H62, 74H62)

NOTES:
- (a) Component values shown are typical.
- (b) Both expander inputs are used simultaneously for expanding.
- (c) If expander is not used leave X and $\overline{X}$ pins open.
- (d) Expander inputs X and $\overline{X}$ are functional on the 9H53/54H53, 74H53 circuits only. Make no external connection to X and $\overline{X}$ pins of the 9H54/54H54, 74H54.
- (e) A total of four 9H60/54H60, 74H60 expander gates or one 9H62/54H62, 74H62 expander gate may be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H53XM/54H53XM 9H54XM/54H54XM			9H53XC/74H53XC 9H54XC/74H54XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage	21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage	22
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA, V_{IN} = 0.8 V	22
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V	21
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	23
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX.	25
I_{CCH}	Supply Current HIGH		7.1	11	mA	V_{CC} = MAX., V_{IN} = 0 V	27
I_{CCL}	Supply Current LOW		9.4	14	mA	V_{CC} = MAX., V_{IN} = 4.5 V	26

NOTES:
- (1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
- (2) Typical limits are at V_{CC} = 5.0 V, 25°C.
- (3) Duration of short-circuit test should not exceed 1 second.
- (4) Required at all input terminals of one AND section to ensure LOW level at output.
- (5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS (9H53/54H53 Circuits Only) Using Expander Inputs, $V_{CC} = 4.5$ V, $T_A = -55°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX			
$I_{IN\bar{X}}$	Expander-Node Input Current			–5.85	mA	$V_{\bar{X}} = 1.4$ V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	$I_{OL} = 20$ mA, $I_1 = 700\ \mu A$, $R_1 = 0\Omega$	29
V_{OH}	Output HIGH Voltage	2.4			Volts	$I_{OH} = -500\ \mu A$, $I_1 = 320\ \mu A$, $I_2 = -320\ \mu A$	30
V_{OL}	Output LOW Voltage			0.4	Volts	$I_{OL} = 20$ mA, $I_1 = 470\ \mu A$, $R_1 = 68\Omega$	29

ELECTRICAL CHARACTERISTICS (9H53/74H53 Circuits Only) Using Expander Inputs, $V_{CC} = 4.75$ V, $T_A = 0°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\bar{X}}$	Expander-Node Input Current			–6.3	mA	$V_{\bar{X}} = 1.4$ V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	$I_{OL} = 20$ mA, $I_1 = 1.1$ mA, $R_1 = 0\Omega$	29
V_{OH}	Output HIGH Voltage	2.4			Volts	$I_{OH} = -500\ \mu A$, $I_1 = 570\ \mu A$, $I_2 = -570\ \mu A$	30
V_{OL}	Output LOW Voltage			0.4	Volts	$I_{OL} = 20$ mA, $I_1 = 600\ \mu A$, $R_1 = 63\Omega$	29

SWITCHING CHARACTERISTICS, Expander Pins are Open ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.0	11	ns	$V_{CC} = 5.0$V $C_L = 25$ pF $R_L = 280\Omega$	T
t_{PHL}	Turn On Delay Input to Output		6.2	11	ns		

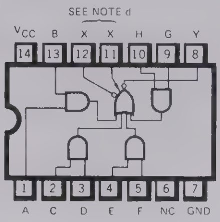
SWITCHING CHARACTERISTICS (9H53/54H53, 74H53 Circuits Only) ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		11.4			$V_{CC} = 5.0$ V $C_L = 25$ pF $R_L = 280\Omega$ $^*C_X = 15$ pF	U *MM & NN
t_{PHL}	Turn On Delay Input to Output		7.4				

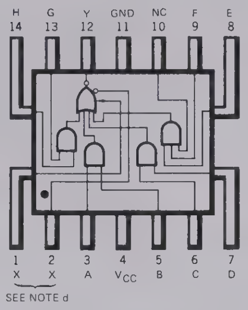
EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM

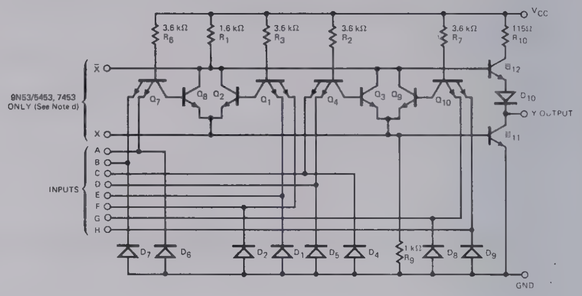
DIP (TOP VIEW)


SEE NOTE d
VCC B X X̄ H G Y
14 13 12 11 10 9 8
1 2 3 4 5 6 7
A C D E F NC GND

FLATPAK (TOP VIEW)


H G Y GND NC F E
14 13 12 11 10 9 8
1 2 3 4 5 6 7
X X̄ A VCC B C D
SEE NOTE d

SCHEMATIC DIAGRAM


VCC
3.6 kΩ R6
1.6 kΩ R1
3.6 kΩ R3
3.6 kΩ R2
3.6 kΩ R7
115Ω R10
X̄
Q7 Q8 Q2 Q1 Q4 Q3 Q9 Q10
Q12
D10
Y OUTPUT
Q11
9N53/5453, 7453 ONLY (See Note d)
X
INPUTS
A B C D E F G H
D7 D6 D2 D1 D5 D4 D8 D9
1 kΩ R9
GND

Positive logic: $Y = \overline{(AB) + (CD) + (EF) + (GH) + (X)}$
(X = Output of 9N60/5460, 7460)

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and X̄ pins open.
(d) Make no external connection to X and X̄ pins of the 9N54/5454, 7454.
(e) A total of four expander gates can be connected to the expander inputs.
(f) NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N53XM/5453XM 9N54XM/5454XM			9N53XC/7453XC 9N54XC/7454XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage		21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage		22
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V		22
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		21
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		23
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N53/5453; 9N54/5454	V_{CC} = MAX.	25
		–18		–55	mA	9N53/7453; 9N54/7454		
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0 V		26
I_{CCL}	Supply Current LOW		5.1	9.5	mA	V_{CC} = MAX., V_{IN} = 5.0 V		27

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and X̄ are open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Required at both input terminals of one AND section to ensure LOW level at output.
(5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS 9N53/5453 CIRCUITS, Using Expander Inputs, V_{CC} = 4.5 V, T_A = 55°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			2.9	mA	V_1 = 0.4 V, I_{OL} = 16 mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 16 mA, I_1 = 0.41 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	I_{OH} = –400 μA, I_1 = 0.15 mA, I_2 = –0.15 mA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 16 mA, I_1 = 0.3 mA, R_1 = 138Ω	29

ELECTRICAL CHARACTERISTICS 9N53/7453 CIRCUITS, Using Expander Inputs, V_{CC} = 4.75 V, T_A = 0°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
I_X	Expander Current			3.1	mA	V_1 = 0.4 V, I_{OL} = 16 mA	28
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	I_{OL} = 16 mA, I_1 = 0.62 mA, R_1 = 0Ω	29
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	I_{OH} = –400 μA, I_1 = 270 μA, I_2 = –270 μA	30
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	I_{OL} = 16 mA, I_1 = 0.43 mA, R_1 = 130Ω	29

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		13	22	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output		8.0	15	ns		

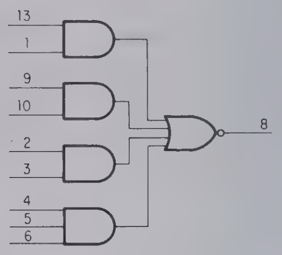
LPTTL/SSI 9L54

LOW POWER AND-OR-INVERT GATE

DESCRIPTION — The Low Power TTL/SSI 9L54 is a four wide, 2-2-2-3-input AND-OR-INVERT Gate. It is designed for low power and medium speed operation.

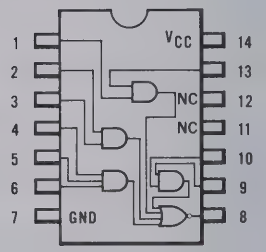
- **TYPICAL POWER DISSIPATION OF 10 mW**
- **TYPICAL DELAY OF 25 ns**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **TTL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" PACKAGES**

LOGIC SYMBOL

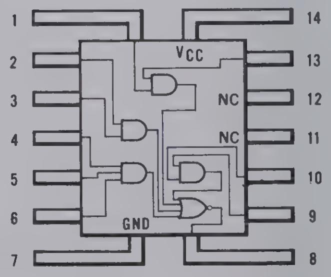

13
1
9
10
2
3
4
5
6
8

V_{CC} = Pin 14
Gnd = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1
2
3
4
5
6
7
14
13
12
11
10
9
8
VCC
NC
NC
GND

FLATPAK (TOP VIEW)


1
2
3
4
5
6
7
14
13
12
11
10
9
8
VCC
NC
NC
GND

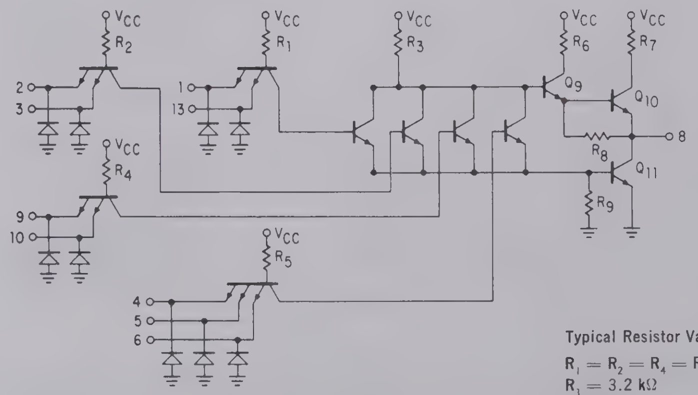
NC = No Internal Connection

PIN NAMES

	LOADING	
	HIGH	LOW
INPUTS (Pins 1, 2, 3, 4, 5, 6, 9, 10, 13)	0.75 U.L.	0.38 U.L.
OUTPUT (Pin 8)	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.

SCHEMATIC DIAGRAM


VCC
R2
VCC
R1
VCC
R3
VCC
R6
VCC
R7
2
3
1
13
Q9
Q10
8
R8
VCC
R4
Q11
R9
9
10
VCC
R5
4
5
6

Typical Resistor Values
$R_1 = R_2 = R_4 = R_5 = 10.4\ k\Omega$
$R_3 = 3.2\ k\Omega$
$R_6 = 600\ \Omega$
$R_7 = 320\ \Omega$
$R_8 = 16\ k\Omega$
$R_9 = 2.66\ \Omega$

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L54XM	4.5V	5.0V	5.5V	−55°C to 125°C
9L54XC	4.75V	5.0V	5.25V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted) (See Notes 1 & 2)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 3)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, $V_{IN} = V_{IL}$
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, $V_{IN} = V_{IH}$
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.38	−0.6	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		3.0	30	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 4)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V Inputs grounded.
I_{CC}	Power Supply Current		2.6	3.7	mA	V_{CC} = MAX., Inputs HIGH
			1.6	2.7	mA	V_{CC} = MAX., Inputs LOW
t_{PLH}	Turn Off Delay		28		ns	V_{CC} = 5.0 V, See Fig. 1
t_{PHL}	Turn On Delay		22		ns	C_L = 15 pF

NOTES:

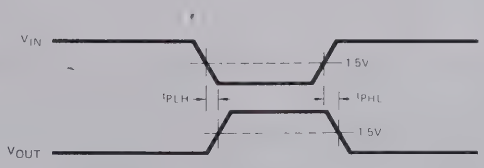
(1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(2) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(3) Typical limits are at V_{cc}= 5.0V, 25°C, and max. loading.

(4) Not more than one output should be shorted at a time.

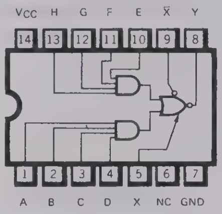
Fig. 1 SWITCHING TIME WAVEFORM



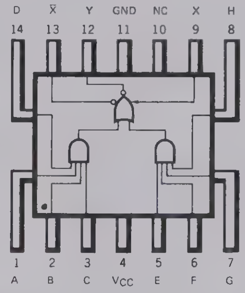
EXPANDABLE 4-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM

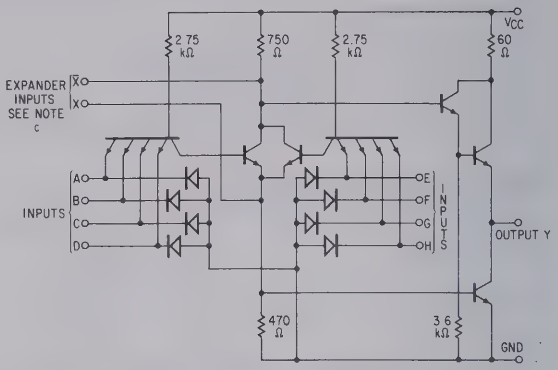
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM



Positive logic: $Y = \overline{(ABCD) + (EFGH) + (X)}$
X = Output of 9H60/54H60, 74H60 or 9H62/54H62, 74H62.

NOTES:
(a) Component values shown are typical.
(b) Both expander inputs are used simultaneously for expanding.
(c) If expander is not used leave X and X̄ pins open.
(d) A total of four 9H60/54H60, 74H60 expander gates or one 9H62/54H62, 74H62 expander gate may be connected to the expander inputs.
(e) NC — No internal connection.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H55XM/54H55XM			9H55XC/74H55XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage (Note 4)	2.0			Volts	Guaranteed Input HIGH Voltage		21
V_{IL}	Input LOW Voltage (Note 5)			0.8	Volts	Guaranteed Input LOW Voltage		22
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA, V_{IN} = 0.8 V		22
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V		21
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	24
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		23
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX.		25
I_{CCH}	Supply Current HIGH		4.5	6.4	mA	V_{CC} = MAX., V_{IN} = 0 V		27
I_{CCL}	Supply Current LOW		7.5	12	mA	V_{CC} = MAX., V_{IN} = 4.5 V		26

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Duration of short-circuit test should not exceed 1 second.
(4) Required at all input terminals of either AND section to ensure LOW level at output.
(5) Required at one input terminal of each AND section to ensure HIGH level at output.

ELECTRICAL CHARACTERISTICS (9H55/54H55 Circuits Only) Using Expander Inputs, $V_{CC} = 4.5$ V, $T_A = -55°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\overline{X}}$	Expander-Node Input Current			–5.85	mA	$V_{\overline{X}} = 1.4$ V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	$I_{OL} = 20$ mA, $I_1 = 700\ \mu A$, $R_1 = 0\Omega$	29
V_{OH}	Output HIGH Voltage	2.4			Volts	$I_{OH} = -500\ \mu A$, $I_1 = 320\ \mu A$, $I_2 = -320\ \mu A$	30
V_{OL}	Output LOW Voltage			0.4	Volts	$I_{OL} = 20$ mA, $I_1 = 470\ \mu A$, $R_1 = 68\Omega$	29

ELECTRICAL CHARACTERISTICS (9H55/74H55 Circuits Only) Using Expander Inputs, $V_{CC} = 4.75$ V, $T_A = 0°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$I_{IN\overline{X}}$	Expander-Node Input Current			–6.3	mA	$V_{\overline{X}} = 1.4$ V	104
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q			1.0	Volts	$I_{OL} = 20$ mA, $I_1 = 1.1$ mA, $R_1 = 0\Omega$	29
V_{OH}	Output HIGH Voltage	2.4			Volts	$I_{OH} = -500\ \mu A$, $I_1 = 570\ \mu A$, $I_2 = -570\ \mu A$	30
V_{OL}	Output LOW Voltage			0.4	Volts	$I_{OL} = 20$ mA, $I_1 = 600\ \mu A$, $R_1 = 63\Omega$	29

SWITCHING CHARACTERISTICS, Expander Pins are Open ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		7.0	11	ns	$V_{CC} = 5.0$ V $C_L = 25$ pF $R_L = 280\Omega$	T
t_{PHL}	Turn On Delay Input to Output		6.5	11	ns		

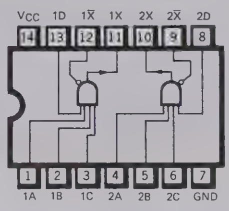
SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		11.4		ns	$V_{CC} = 5.0$ V $C_L = 25$ pF $R_L = 280\Omega$ $^*C_X = 15$ pF	U *MM & NN
t_{PHL}	Turn On Delay Input to Output		7.7		ns		

DUAL 4-INPUT EXPANDER

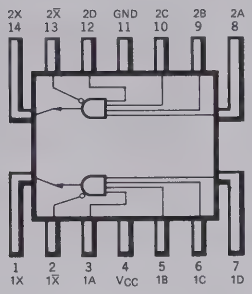
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

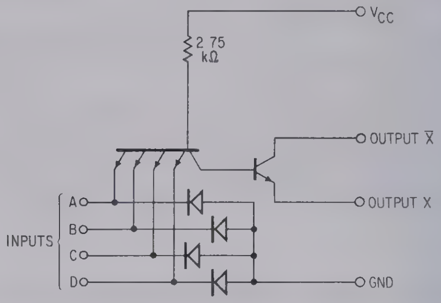


Positive logic: X = ABCD when connected to X and $\overline{X}$ pins of 9H50/54H50, 74H50; 9H53/54H53, 74H53 or 9H55/54H55, 74H55 circuit.

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH EXPANDER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H60XM/54H60XM			9H60XC/74H60XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Maximum number of expanders that may be fanned in to one expandable AND OR Invert Gate			4			4	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	(Note 3)	31
V_{IL}	Input LOW Voltage			0.8	Volts	(Note 4)	32
V_{ON}	On-State Output Voltage			0.4	Volts	V_{CC} = MIN., V_{IN} = 2.0 V, V_1 = 1.0 V T_A = –55°C, I_{ON} = 5.85 mA T_A = 0°C I_{ON} = 6.3 mA	31
				0.4	Volts	V_{CC} = MAX., V_{IN} = 2.0 V, V_1 = 0.6 V T_A = 125°C, I_{ON} = 7.85 mA T_A = 70°C, I_{ON} = 7.4 mA	
I_{OFF}	Off-State Output Current			320	µA	T_A = –55°C, V_{CC} = MIN., V_{IN} = 0.8 V	32
				570	µA	T_A = 0°C, V_1 = 4.5 V, R = 575Ω	
I_{ON}	On-State Output Current	–470			µA	T_A = –55°C, V_{CC} = MIN., V_{IN} = 2.0 V	33
		–600			µA	T_A = 0°C, V_1 = 1.0 V	
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V, Each Input	34
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	32
$I_{CC(ON)}$	On-State Supply Current		1.9	3.5	mA	V_{CC} = MAX., V_{IN} = 4.5 V, V_1 = 0.85 V	35
$I_{CC(OFF)}$	Off-State Supply Current		3.0	4.5	mA	V_{CC} = MAX., V_{IN} = 0 V, V_1 = 0.85 V	35

OUTPUT CAPACITANCE, V_{CC} AND GND TERMINALS OPEN (T_A = 25°C)

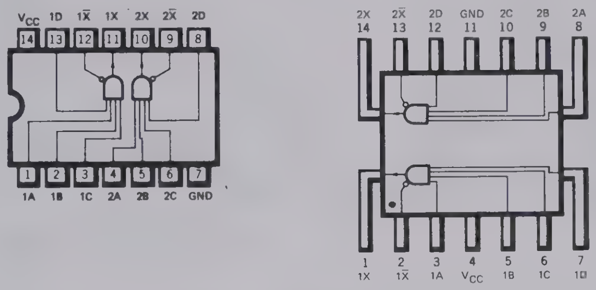
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
$C_{\overline{X}}$	Effective Capacitance of Output Transistor Q_1		1.3		pF	f = 1 MHz	BB

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Required at all input terminals to ensure output is in the on state.
(4) Required at any input terminal to ensure output is in the off state.

DUAL 4-INPUT EXPANDER

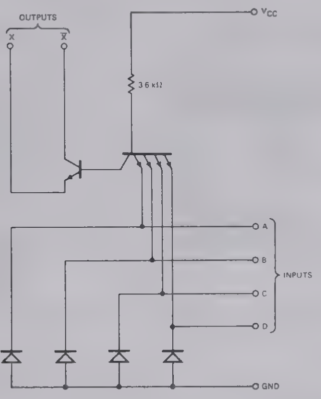
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW) **FLATPAK** (TOP VIEW)



Positive logic: X = ABCD when connected to X and X̄ pins of 9N50/5450, 7450; 9N53/5453, 7453 circuit.

SCHEMATIC DIAGRAM (EACH EXPANDER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N60XM/5460XM			9N60XC/7460XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Maximum number of expanders that may be fanned-in to one expandable AND OR Invert Gate			4			4	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		31
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		32
V_{ON}	On-State Output Voltage			0.4	Volts	V_{CC} = MIN., V_{IN} = 2.0 V V_1 = 1.0 V, R = 1.1 kΩ T_A = –55°C T_A = 0°C		31
I_{OFF}	Off-State Output Current			150	µA	T_A = –55°C	V_{CC} = MIN., V_{IN} = 0.8 V	32
				270	µA	T_A = 0°C	V_1 = 4.5 V, R = 1.2 kΩ	
I_{ON}	On-State Output Current	–0.3			mA	T_A = –55°C, V_{CC} = MIN., V_{IN} = 2.0 V, V_1 = 1.0 V		33
		–0.43			mA	V_{CC} = 4.75 V, V_{IN} = 2.0 V, V_1 = 1.0 V		
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	34
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		32
$I_{CC\ (on)}$	On-State Supply Current		1.2	2.5	mA	V_{CC} = MAX., V_{IN} = 5.0 V, V_1 = 0.85 V		35
$I_{CC\ (off)}$	Off-State Supply Current		2.0	4.0	mA	V_{CC} = MAX., V_{IN} = 0 V, V_1 = 0.85 V		35

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	*Turn Off Delay Input to Output		15	30	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	B
t_{PHL}	*Turn On Delay Input to Output		10	20	ns		

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

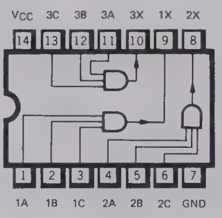
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

*Through 9N50/5450, 7450; 9N53/5453, 7453.

TRIPLE 3-INPUT EXPANDER

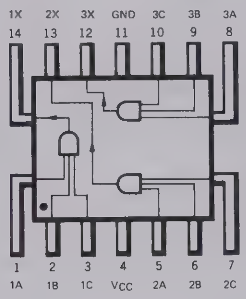
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

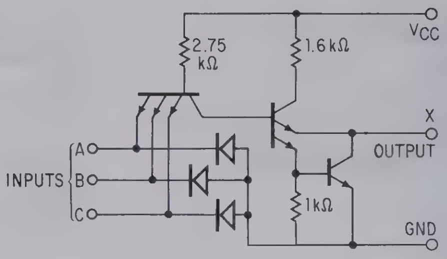


Positive logic: $X = ABC$

FLATPAK (TOP VIEW)



SCHEMATIC DIAGRAM (EACH EXPANDER)



Component values shown are typical.

When connected to the X input of the 9H52/54H52, 74H52 circuit.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H61XM/54H61XM			9H61XC/74H61XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	(Note 3)		114
V_{IL}	Input LOW Voltage			0.8	Volts	(Note 4)		113
V_{ON}	On-State Output Voltage			1.0	Volts	V_{CC} = MIN., V_{IH} = 2 V T_A = –55°C, I_{ON} = 4.5 mA T_A = 0°C, I_{ON} = 5.35 mA		114
I_{OFF}	Off-State Output Current			50	µA	V_{CC} = MIN., V_{IL} = 0.8 V V_{OFF} = 2.2 V, T_A = MAX.		113
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	78
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		79
$I_{CC(ON)}$	On-State Supply Current		11	16	mA	V_{CC} = MAX., V_{IN} = 4.5 V		81
$I_{CC(OFF)}$	Off-State Supply Current		5.0	7.0	mA	V_{CC} = MAX., V_{IN} = 0 V		81

OUTPUT CAPACITANCE, V_{CC} AND GND TERMINALS OPEN (T_A = 25°C)

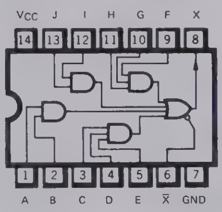
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
C_X	Effective Capacitance of Output Transistor Q_1		1.3		pF	f = 1 MHz	CC

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Required at all input terminals to ensure output is in the on state.
(4) Required at any input terminal to ensure output is in the off state.

3-2-2-3-INPUT AND-OR EXPANDER

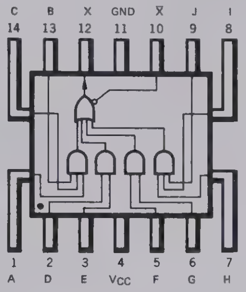
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



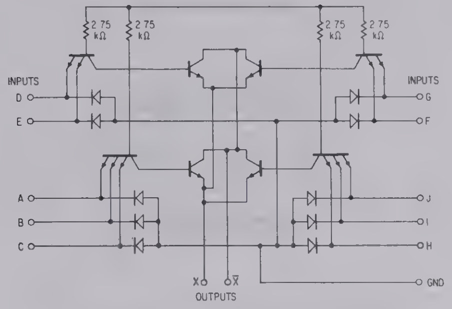
Positive logic:
X = (AB) + (CDE) + (FGH) + (IJ)

FLATPAK (TOP VIEW)



Positive logic:
X = (ABC) + (DE) + (FG) + (HIJ)

SCHEMATIC DIAGRAM



Component values shown are typical.

When connected to X and X̄ pins of 9H50/54H50, 74H50; 9H53/54H53, 74H53 or 9H55/54H55, 74H55 circuit.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H62XM/54H62XM			9H62XC/74H62XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Maximum number of expanders that may be fanned in to one expandable AND OR Invert Gate			1			1	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 2)	MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	(Note 3)	115
V_{IL}	Input LOW Voltage			0.8	Volts	(Note 4)	116
V_{ON}	On-State Output Voltage			0.4	Volts	V_{CC} = MIN., V_{IN} = 2.0 V, V_1 = 1.0 V T_A = –55°C, I_{ON} = 5.85 mA T_A = 0°C, I_{ON} = 6.3 mA	115
				0.4	Volts	V_{CC} = MAX., V_{IN} = 2.0 V, V_1 = 0.6 V T_A = 125°C, I_{ON} = 7.85 mA T_A = 70°C, I_{ON} = 7.4 mA	
I_{OFF}	Off-State Output Current			320	µA	T_A = –55°C; V_{CC} = MIN., V_{IN} = 0.8 V	116
				570	µA	T_A = 0°C; V_1 = 4.5 V, R = 575Ω	
I_{ON}	On-State Output Current	–470			µA	T_A = –55°C; V_{CC} = MIN., V_{IN} = 2.0 V	117
		–600			µA	T_A = 0°C; V_1 = 1.0 V	
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V; Each Input	119
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	118
$I_{CC(ON)}$	On-State Supply Current		3.8	7.0	mA	V_{CC} = MAX., V_{IN} = 4.5 V, V_1 = 0.85 V	120
$I_{CC(OFF)}$	Off-State Supply Current		6.0	9.0	mA	V_{CC} = MAX., V_{IN} = 0 V, V_1 = 0.85 V	120

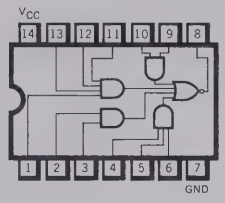
OUTPUT CAPACITANCE, V_{CC} AND GND TERMINALS OPEN (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
$C_{\bar{X}}$	Effective Capacitance of Output Transistor Q_1		1.3		pF	f = 1 MHz	BB

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Required at all input terminals of one AND section to ensure output is in the on state.
(4) Required at one input terminal of each AND section to ensure output is in the off state.

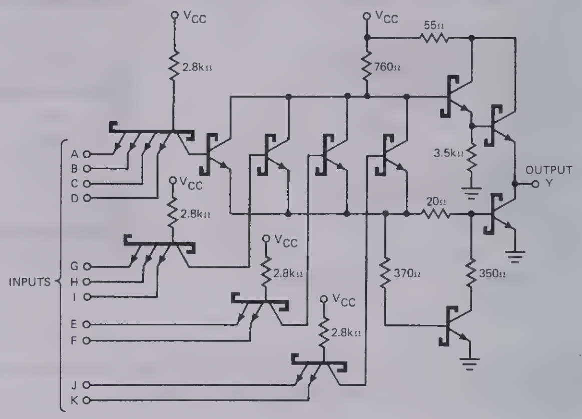
4-2-3-2-INPUT AND-OR-INVERT GATE

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: $\overline{ABCD + EF + GHE + JK}$

SCHEMATIC DIAGRAM



All inputs have Schottky clamp diodes.
Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S64XM/54S64XM			9S64XC/74S64XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA, V_{IN} = 0.8 V
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current			–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CCH}	Supply Current HIGH			7.0	12.5	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCL}	Supply Current LOW			8.5	16	mA	V_{CC} = MAX., (Note 4)

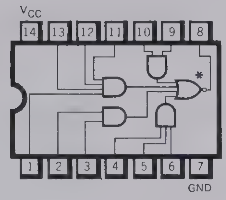
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	3.5	5.5	ns	V_{CC} = 5.0 V C_L = 15 pF	FF
t_{PHL}	Turn On Delay Input to Output	2.0	3.5	5.5	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CCL} is measured with all inputs of one gate open, and remaining inputs grounded.

4-2-3-2-INPUT AND-OR-INVERT GATE (WITH OPEN COLLECTOR)

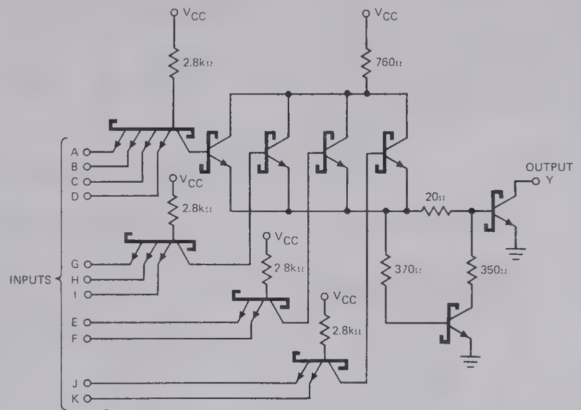
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



*OPEN COLLECTOR

Positive logic: $\overline{ABCD + EF + GHI + JK}$

SCHEMATIC DIAGRAM



Component values shown are typical.
All inputs have clamp diodes (not shown).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	†9S65XM/54S65XM			9S65XC/74S65XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Input Loading for Each Input			1.25			1.25	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–1.2	Volts	V_{CC} = MIN., I_{IN} = –18 mA
I_{OH}	Output HIGH Current		0.1	250	µA	V_{CC} = MIN., V_{OH} = 5.5 V, V_{IN} = 0.8 V
V_{OL}	Output LOW Voltage		0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current		1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
I_{CCH}	Supply Current HIGH		6.0	11.0	mA	V_{CC} = MAX., V_{IN} = 0 V
I_{CCL}	Supply Current LOW		8.5	16	mA	V_{CC} = MAX., (Note 3)

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	5.0	7.5	ns	V_{CC} = 5.0 V C_L = 15 pF	FF
t_{PHL}	Turn On Delay Input to Output	2.0	5.5	8.5	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) I_{CCL} is measured with all inputs of one gate open, and remaining inputs grounded.

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† To be announced 1972

EDGE TRIGGERED JK FLIP-FLOP

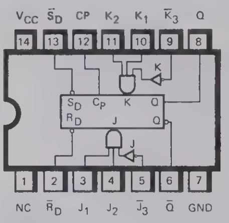
DESCRIPTION – The 9N70/5470, 7470 is a gated input edge triggered JK flip-flop offering direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Information at the J and K inputs is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, when the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are designed for medium to high speed applications and offer a significant saving in system power dissipation and package count where input gating is required.

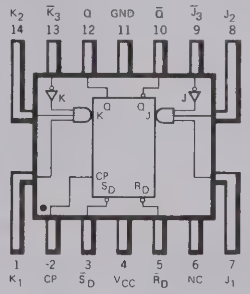
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

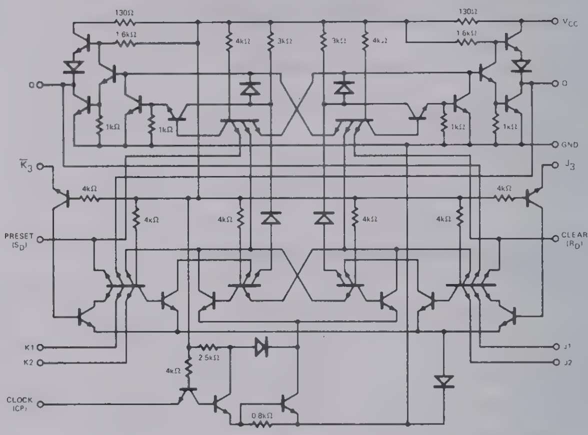

V_{CC}
$\overline{S}_D$
CP
K_2
K_1
$\overline{K}_3$
Q
14
13
12
11
10
9
8
K
S_D
C_P
K
Q
R_D
J
$\overline{Q}$
J
1
2
3
4
5
6
7
NC
$\overline{R}_D$
J_1
J_2
$\overline{J}_3$
$\overline{Q}$
GND

NC – No internal connection.

FLATPAK (TOP VIEW)


K_2
$\overline{K}_3$
Q
GND
$\overline{Q}$
$\overline{J}_3$
J_2
14
13
12
11
10
9
8
K
K
Q
$\overline{Q}$
J
J
CP
S_D
R_D
1
2
3
4
5
6
7
K_1
CP
$\overline{S}_D$
V_{CC}
$\overline{R}_D$
NC
J_1

SCHEMATIC DIAGRAM


130Ω
1.6kΩ
4kΩ
3kΩ
1kΩ
4kΩ
130Ω
1.6kΩ
V_{CC}
$\overline{Q}$
Q
1kΩ
1kΩ
1kΩ
1kΩ
GND
$\overline{K}_3$
$\overline{J}_3$
4kΩ
4kΩ
4kΩ
4kΩ
4kΩ
4kΩ
4kΩ
PRESET (S_D)
CLEAR (R_D)
K1
K2
J1
J2
2.5kΩ
4kΩ
CLOCK (CP)
0.8kΩ

Component values shown are typical.

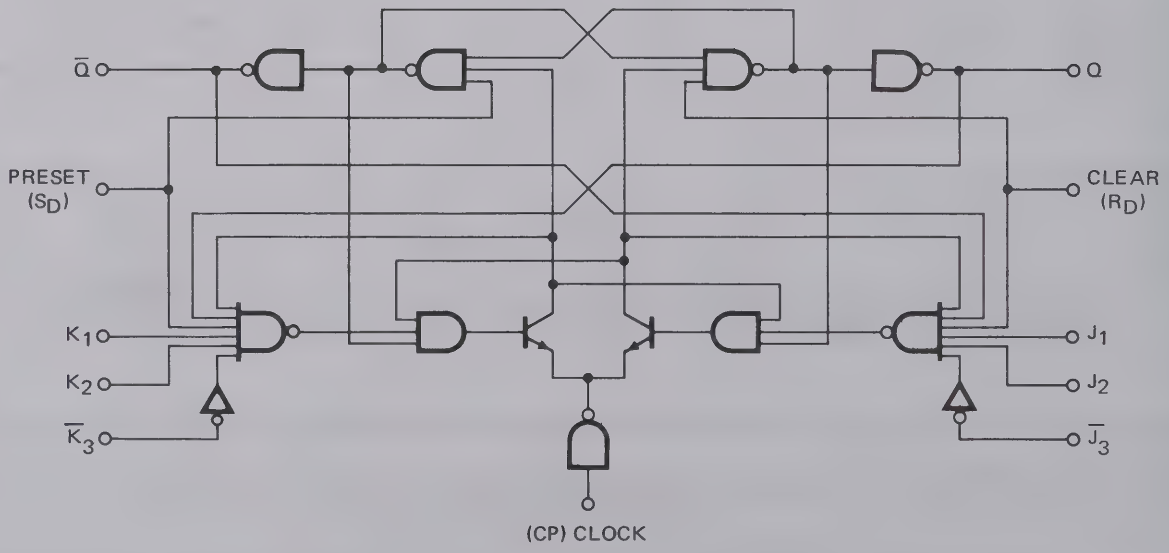
Positive logic:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset or clear function can occur only
when clock input is LOW

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
$J = J1 \cdot J2 \cdot \overline{J3}$
$K = K1 \cdot K2 \cdot \overline{K3}$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
If inputs $\overline{J3}$ or $\overline{K3}$ are not used they must be grounded.

LOGIC DIAGRAM


$\overline{Q}$
Q
PRESET (S_D)
CLEAR (R_D)
K_1
K_2
$\overline{K}_3$
J_1
J_2
$\overline{J}_3$
(CP) CLOCK

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N70XM/5470XM			9N70XC/7470XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Clock Pulse Transition Time to HIGH Level, $t_{1(clock)}$ (See Fig. D)	5.0		150	5.0		150	ns
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. D)	20			20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. C)	25			25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. C)	25			25			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	36 & 37
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	36 & 37
V_{OH}	Output HIGH Voltae	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA	36
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	37
I_{IH}	Input HIGH Current at J_1, J_2, $\overline{J}_3$, K_1, K_2, $\overline{K}_3$ or Clock			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	39
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear or Preset			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V	39
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J_1, J_2, $\overline{J}_3$, K_1, K_2, $\overline{K}_3$ or Clock			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	38
	Input LOW Current at Clear or Preset			–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	38
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9N70/5470 V_{CC} = MAX.	40
		–18		–57	mA	9N70/7470 V_{IN} = 0 V	
I_{CC}	Supply Current		13	26	mA	V_{CC} = MAX., V_{IN} = 5.0 V	39

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	20	35		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	D
t_{setup}	Maximum Input Setup Time		10	20	ns		D
t_{hold}	Maximum Input Hold Time		0	5.0	ns		D
t_{PLH}	Turn Off Delay Clear or Preset to Output			50	ns		C
t_{PHL}	Turn On Delay Clear or Preset to Output			50	ns		C
t_{PLH}	Turn Off Delay Clock to Output	10	27	50	ns		D
t_{PHL}	Turn On Delay Clock to Output	10	18	50	ns		D

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

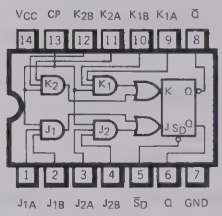
(3) Not more than one output should be shorted at a time.

JK MASTER/SLAVE FLIP-FLOP WITH AND-OR INPUTS

DESCRIPTION — The HSTTL/SSI 9H71/54H71, 74H71 is a High Speed JK Master/Slave flip-flop with AND-OR gate inputs. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from AND-OR gate inputs to master. 3) Disable AND-OR gate inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

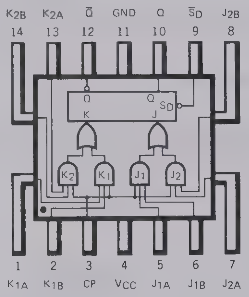
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



V_{CC}
CP
K_{2B}
K_{2A}
K_{1B}
K_{1A}
$\overline{Q}$
14
13
12
11
10
9
8
K_2
K_1
K
Q
J_1
J_2
J
S_D
$\overline{Q}$
1
2
3
4
5
6
7
J_{1A}
J_{1B}
J_{2A}
J_{2B}
$\overline{S}_D$
Q
GND

FLATPAK (TOP VIEW)

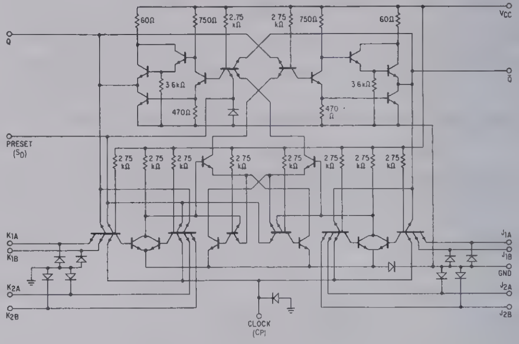


K_{2B}
K_{2A}
$\overline{Q}$
GND
Q
$\overline{S}_D$
J_{2B}
14
13
12
11
10
9
8
$\overline{Q}$
Q
S_D
K
J
K_2
K_1
J_1
J_2
1
2
3
4
5
6
7
K_{1A}
K_{1B}
CP
V_{CC}
J_{1A}
J_{1B}
J_{2A}

Positive logic:

LOW input to preset sets Q to HIGH level
Preset is independent of clock

SCHEMATIC DIAGRAM



V_{CC}
Q
$\overline{Q}$
60Ω
750Ω
2.75 kΩ
2.75 kΩ
750Ω
60Ω
3.6kΩ
3.6kΩ
470Ω
470 Ω
PRESET ($\overline{S}_D$)
2.75 kΩ
K_{1A}
K_{1B}
K_{2A}
K_{2B}
J_{1A}
J_{1B}
GND
J_{2A}
J_{2B}
CLOCK (CP)

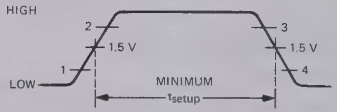
Component values shown are typical.

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

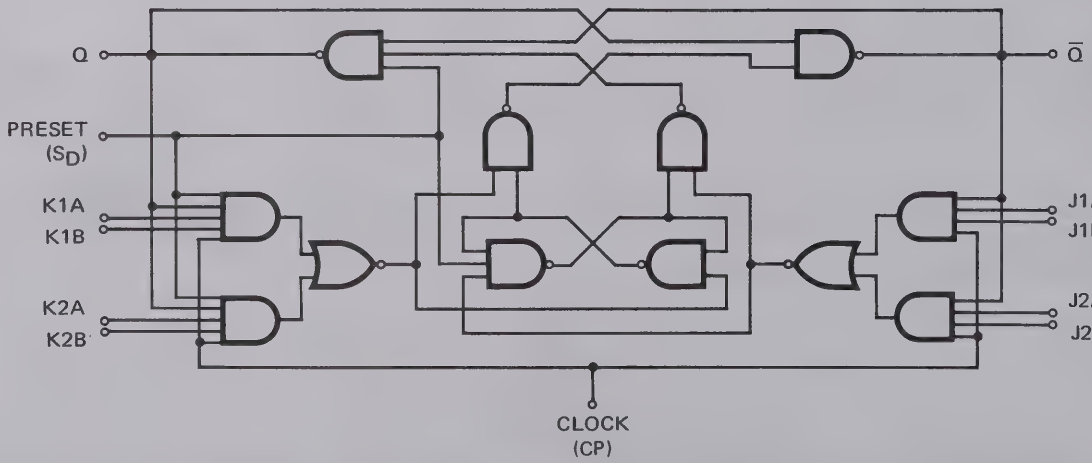
NOTES:
J = (J1A·J1B)+(J2A·J2B)
K = (K1A·K1B)+(K2A·K2B)
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM



HIGH
LOW
1
2
3
4
1.5 V
1.5 V
MINIMUM
t_{setup}

LOGIC DIAGRAM



Q
$\overline{Q}$
PRESET (S_D)
K1A
K1B
K2A
K2B
J1A
J1B
J2A
J2B
CLOCK (CP)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H71XM/54H71XM			9H71XC/74H71XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	121 & 122
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	121 & 122
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA	121
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	122
I_{IH}	Input HIGH Current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset			150	µA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
	Input LOW Current at Preset			–6.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
	Input LOW Current at Clock			–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 0 V	127
I_{CC}	Supply Current		19	30	mA	V_{CC} = MAX.	124

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset to Output		6.0	13	ns		X
t_{PHL}	Turn On Delay Preset to Output		12	24	ns		X
t_{PLH}	Turn Off Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn On Delay Clock to Output	10	22	27	ns		W

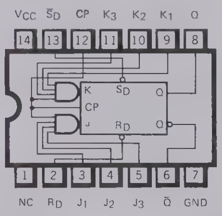
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

JK MASTER/SLAVE FLIP-FLOP WITH AND INPUTS

DESCRIPTION — The HSTTL/SSI 9H72/54H72, 74H72 is a High Speed JK Master/Slave flip-flop with AND gate inputs. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from AND gate inputs to master. 3) Disable AND gate inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

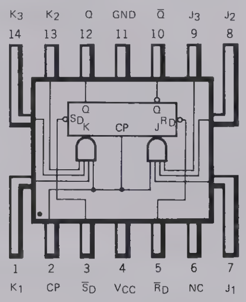
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



VCC
S̄D
CP
K3
K2
K1
Q
14
13
12
11
10
9
8
K
SD
Q
CP
J
RD
Q̄
1
2
3
4
5
6
7
NC
R̄D
J1
J2
J3
Q̄
GND

FLATPAK (TOP VIEW)



K3
K2
Q
GND
Q̄
J3
J2
14
13
12
11
10
9
8
Q
Q̄
SD
K
CP
J
RD
1
2
3
4
5
6
7
K1
CP
S̄D
VCC
R̄D
NC
J1

NC — No internal connection.

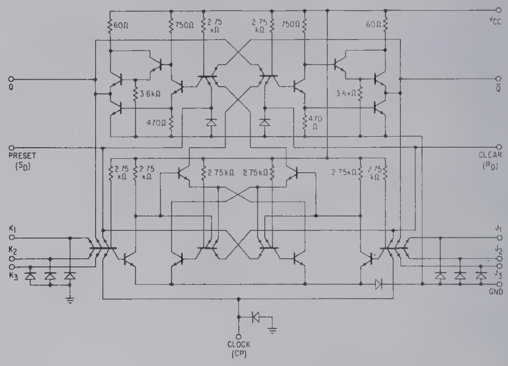
Positive logic:

LOW input to preset sets Q to HIGH level

LOW input to clear sets Q to LOW level

Preset and clear are independent of clock

SCHEMATIC DIAGRAM



60Ω
750Ω
2.75 kΩ
2.75 kΩ
750Ω
60Ω
VCC
Q
Q̄
3.6kΩ
3.6kΩ
470Ω
470 Ω
PRESET (S̄D)
CLEAR (R̄D)
2.75 kΩ
2.75 kΩ
2.75kΩ
2.75kΩ
2.75kΩ
2.75 kΩ
K1
K2
K3
J1
J2
J3
GND
CLOCK (CP)

Component values shown are typical.

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:

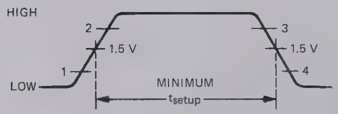
J = J1·J2·J3

K = K1·K2·K3

t_n = Bit time before clock pulse

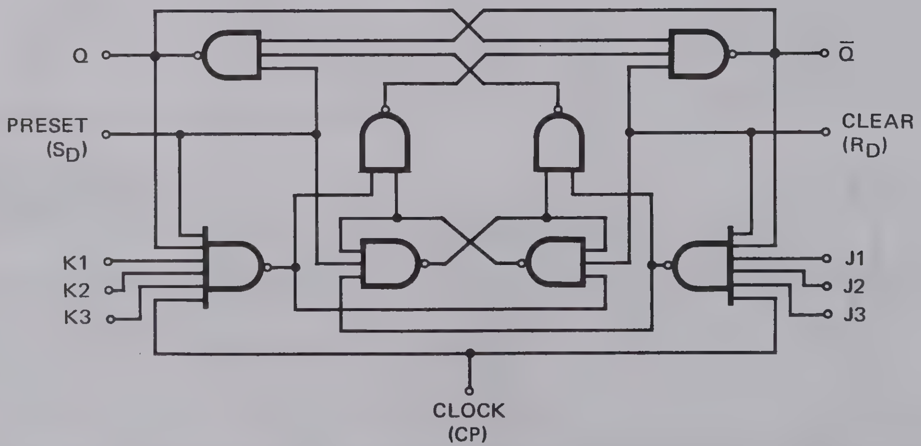
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM



HIGH
LOW
1
2
3
4
1.5 V
1.5 V
MINIMUM
t_{setup}

LOGIC DIAGRAM



Q
Q̄
PRESET (SD)
CLEAR (RD)
K1
K2
K3
J1
J2
J3
CLOCK (CP)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H72XM/54H72XM			9H72XC/74H72XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)	16			16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geqslant t_{p(clock)}$			$\geqslant t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	41 & 42
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	41 & 42
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA	41
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	42
I_{IH}	Input HIGH Current at J2, J3, K1, K2, or K3			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at J1,			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock Preset or Clear			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J1, J2, J3, K1, K2, K3, or Clock			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
	Input LOW Current at Preset or Clear			–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 0 V	45
I_{CC}	Supply Current		16	25	mA	V_{CC} = MAX.	44

SWITCHING CHARACTERISTICS (T_A = 25°C)

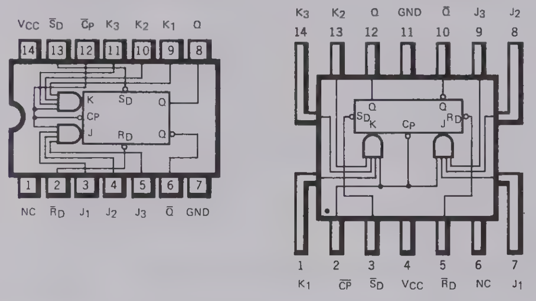
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear or Preset to Output		6.0	13	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output		12	24	ns		X
t_{PLH}	Turn Off Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn On Delay Clock to Output	10	22	27	ns		W

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Note more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

JK MASTER/SLAVE FLIP-FLOP WITH AND INPUTS

DESCRIPTION – The TTL/SSI 9N72/5472, 7472 is a JK Master/Slave flip-flop with AND gate inputs. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from AND gate inputs to master. 3) Disable AND gate inputs. 4) Transfer information from master to slave.

LOGIC AND CONNECTION DIAGRAM



DIP (TOP VIEW)

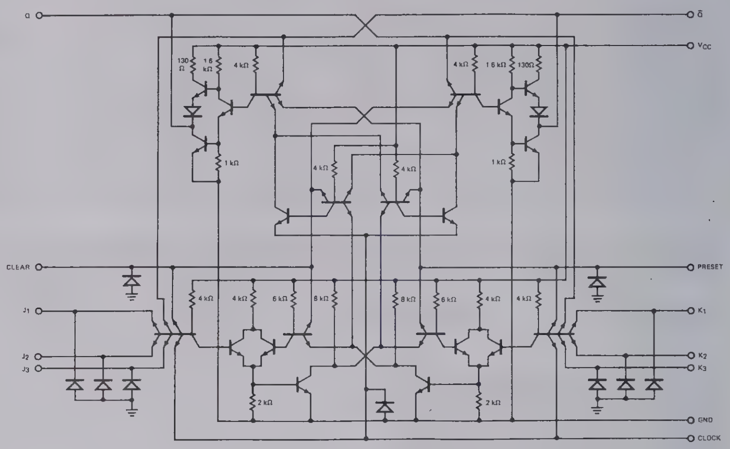
FLATPAK (TOP VIEW)

V_{CC}
$\overline{S}_D$
$\overline{C}_P$
K_3
K_2
K_1
Q
14
13
12
11
10
9
8
K
S_D
CP
J
R_D
Q
$\overline{Q}$
1
2
3
4
5
6
7
NC
$\overline{R}_D$
J_1
J_2
J_3
$\overline{Q}$
GND
K_3
K_2
Q
GND
$\overline{Q}$
J_3
J_2
14
13
12
11
10
9
8
S_D
K
CP
J
R_D
1
2
3
4
5
6
7
K_1
$\overline{CP}$
$\overline{S}_D$
V_{CC}
$\overline{R}_D$
NC
J_1

NC — No internal connection.

Positive logic:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM



Q
$\overline{Q}$
V_{CC}
130 Ω
1.6 kΩ
4 kΩ
1 kΩ
CLEAR
PRESET
J_1
J_2
J_3
K_1
K_2
K_3
6 kΩ
8 kΩ
2 kΩ
GND
CLOCK

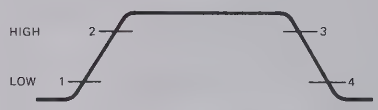
Component values shown are typical.

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

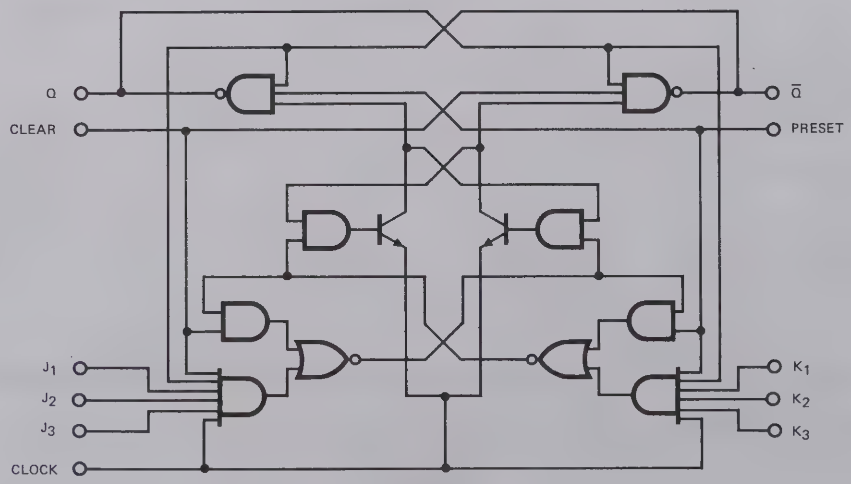
NOTES:
J = J1 · J2 · J3
K = K1 · K2 · K3
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



HIGH
LOW
1
2
3
4

LOGIC DIAGRAM



Q
CLEAR
$\overline{Q}$
PRESET
J_1
J_2
J_3
CLOCK
K_1
K_2
K_3

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N72XM/5472XM			9N72XC/7472XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. E)	20			20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. F)	25			25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. F)	25			25			ns
Input Setup Time, t_{setup} (See Fig. E)	$\geqslant t_{p(clock)}$			$\geqslant t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	41 & 42
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	41 & 42
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA	41
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	42
I_{IH}	Input HIGH Current at J_1, J_2, J_3, K_1, K_2 or K_3			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear Preset or Clock			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J_1, J_2, J_3, K_1, K_2 or K_3			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
	Input LOW Current at Clear, Preset or Clock			–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9N72/5472 V_{CC} = MAX.	45
		–18		–57	mA	9N72/7472 V_{IN} = 0 V	
I_{CC}	Supply Current		10	20	mA	V_{CC} = MAX., V_{IN} = 5.0 V	44

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	15	20		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	E
t_{PLH}	Turn Off Delay Clear or Preset to Output		16	25	ns		F
t_{PHL}	Turn On Delay Clear or Preset to Output		25	40	ns		F
t_{PLH}	Turn Off Delay Clock to Output	10	16	25	ns		E
t_{PHL}	Turn On Delay Clock to Output	10	25	40	ns		E

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

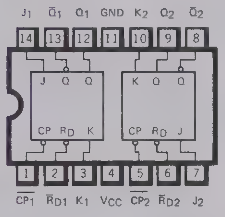
(3) Not more than one output should be shorted at a time.

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE CLEARS AND CLOCKS

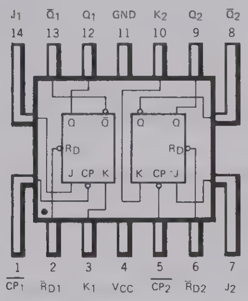
DESCRIPTION – The HSTTL/SSI 9H73/54H73, 74H73 is a High Speed Dual JK Master/Slave flip-flop with separate clears and separate clocks. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)


J1 Q̄1 Q1 GND K2 Q2 Q̄2
14 13 12 11 10 9 8
J Q Q̄
K Q Q̄
CP RD K
CP RD J
1 2 3 4 5 6 7
C̄P̄1 R̄D1 K1 VCC C̄P̄2 R̄D2 J2

FLATPAK (TOP VIEW)

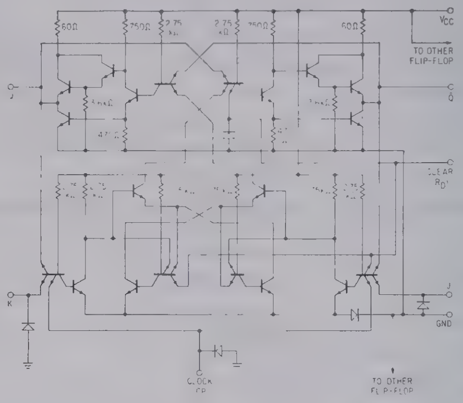

J1 Q̄1 Q1 GND K2 Q2 Q̄2
14 13 12 11 10 9 8
Q Q̄
RD
J CP K
Q Q̄
RD
K CP J
1 2 3 4 5 6 7
C̄P̄1 R̄D1 K1 VCC C̄P̄2 R̄D2 J2

Positive logic:

LOW input to clear sets Q to LOW level

Clear is independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)


60Ω
750Ω
2.75 kΩ
2.75 kΩ
750Ω
60Ω
VCC
TO OTHER FLIP-FLOP
Q
Q̄
CLEAR RD
K
J
GND
CLOCK CP
TO OTHER FLIP-FLOP

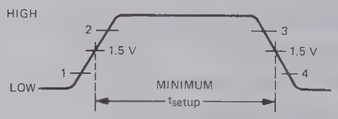
Component values shown are typical.
Resistor values are in ohms.

TRUTH TABLE

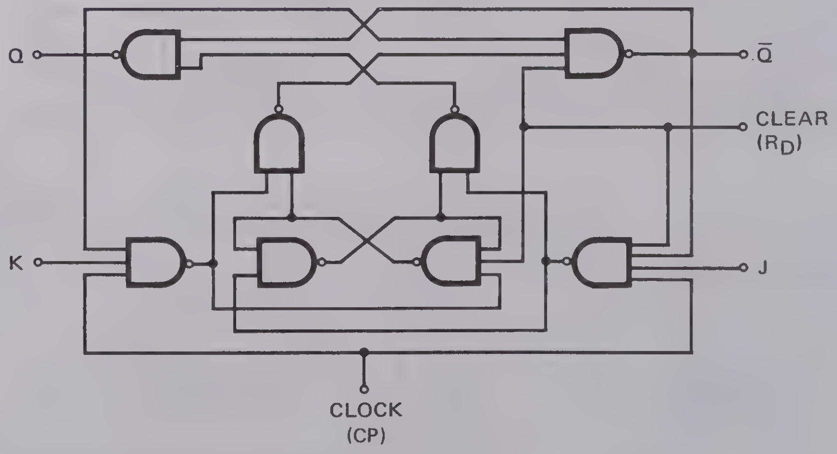
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORMS


HIGH
LOW
1
2
3
4
1.5 V
1.5 V
MINIMUM
tsetup

LOGIC DIAGRAM
(EACH FLIP-FLOP)


Q
Q̄
CLEAR
(RD)
K
J
CLOCK
(CP)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H73XM/54H73XM			9H73XC/74H73XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flaptak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.5 mA	46
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock			5.0	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K or Clock			–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clear			–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 0V	50
I_{CC}	Supply Current		32	50	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear to Output		6.0	13	ns		X
t_{PHL}	Turn On Delay Clear to Output		12	24	ns		X
t_{PLH}	Turn Off Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn On Delay Clock to Output	10	22	27	ns		W

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

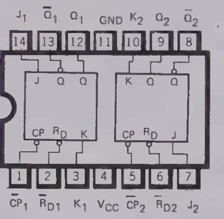
DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE CLEARS AND CLOCKS

DESCRIPTION – The TTL/SSI 9N73/5473, 7473 and 9N107/54107, 74107 are Dual JK Master/Slave flip-flops with a separate clear and a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave.

LOGIC AND CONNECTION DIAGRAM

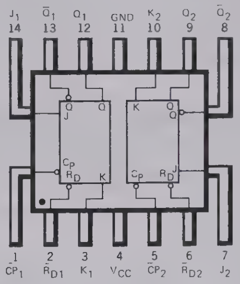
9N73/5473, 7473

DIP (TOP VIEW)



J_1 $\bar{Q}_1$ Q_1 GND K_2 Q_2 $\bar{Q}_2$
14 13 12 11 10 9 8
J Q $\bar{Q}$
K Q $\bar{Q}$
CP R_D K
CP R_D J
1 2 3 4 5 6 7
$\bar{CP}_1$ $\bar{R}_{D1}$ K_1 V_{CC} $\bar{CP}_2$ $\bar{R}_{D2}$ J_2

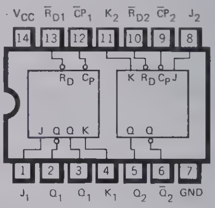
FLATPAK (TOP VIEW)



J_1 $\bar{Q}_1$ Q_1 GND K_2 Q_2 $\bar{Q}_2$
14 13 12 11 10 9 8
1 2 3 4 5 6 7
$\bar{CP}_1$ $\bar{R}_{D1}$ K_1 V_{CC} $\bar{CP}_2$ $\bar{R}_{D2}$ J_2

9N107/54107, 74107

DIP (TOP VIEW)



V_{CC} $\bar{R}_{D1}$ $\bar{CP}_1$ K_2 $\bar{R}_{D2}$ $\bar{CP}_2$ J_2
14 13 12 11 10 9 8
R_D C_P
K R_D C_P J
J Q Q K
Q Q
1 2 3 4 5 6 7
J_1 $\bar{Q}_1$ Q_1 K_1 Q_2 $\bar{Q}_2$ GND

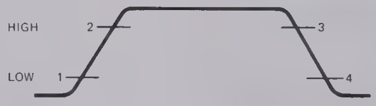
Positive logic:
LOW input to clear sets Q to LOW level
Clear is independent of clock

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

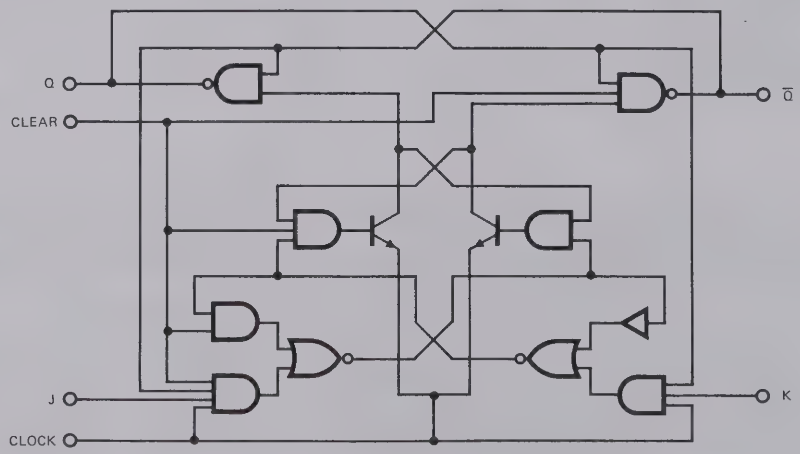
NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



HIGH
LOW
1
2
3
4

LOGIC DIAGRAM
(EACH FLIP-FLOP)



Q
CLEAR
J
CLOCK
$\bar{Q}$
K

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N73XM/5473XM 9N107XM/54107XM			9N73XC/7473XC 9N107XC/74107XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. E)	20			20			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. F)	25			25			ns
Input Setup Time, t_{setup} (See Fig. E)	$\geqslant t_{p(clock)}$			$\geqslant t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH		46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW		46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA		46
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		47
I_{IH}	Input HIGH Current at J or K			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V		49
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Clock or Clear			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V		49
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at J or K			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		48
	Input LOW Current at Clear or Clock			–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		48
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9N73/5473; 9N107/54107	V_{CC} = MAX. V_{IN} = 0 V	50
		–18		–57	mA	9N73/7473; 9N107/74107		
I_{CC}	Supply Current		20	40	mA	V_{CC} = MAX.		49

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	15	20		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	E
t_{PLH}	Turn Off Delay Clear to Output		16	25	ns		F
t_{PHL}	Turn On Delay Clear to Output		25	40	ns		F
t_{PLH}	Turn Off Delay Clock to Output	10	16	25	ns		E
t_{PHL}	Turn On Delay Clock to Output	10	25	40	ns		E

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

DUAL D TYPE EDGE TRIGGERED FLIP-FLOP

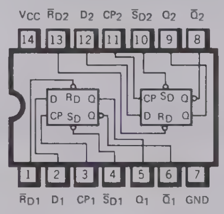
DESCRIPTION – The HSTTL/SSI 9H74/54H74, 74H74 is a High Speed Dual, Edge Triggered flip-flop utilizing TTL circuitry to perform D type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect.

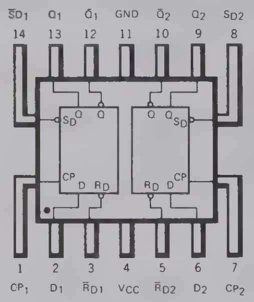
These circuits are fully compatible for use with the Fairchild TTL family. Input clamping diodes are provided to minimize transmission line effects and thereby simplify systems design. Maximum clock frequency is 35 MHz, with a typical power dissipation of 75 mW per flip-flop.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

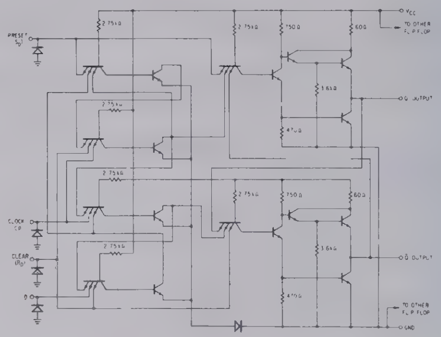


FLATPAK (TOP VIEW)



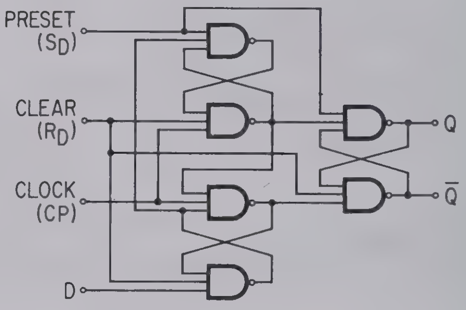
Asynchronous Inputs:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)



Component values shown are typical.

LOGIC DIAGRAM (EACH FLIP-FLOP)



TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
L	L	H
H	H	L

H = HIGH Level, L = LOW Level

NOTES: t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H74XM/54H74XM MIN.	TYP.	MAX.	9H74XC/74H74XC MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Fan Out from Each Output	LOW Level			12.5			12.5	U.L.
	HIGH Level			25			25	
Clock Frequency, f_{clock}		0		35	0		35	MHz
Width of Clock Pulse, $t_{pw(clock)}$ (See Figure Z or AA)		15			15			ns
Width of Preset pulse, $t_{pw(preset)}$ (See Figure Y)		25			25			ns
Width of Clear Pulse, $t_{pw(clear)}$ (See Figure Y)		25			25			ns
Input Setup Time, t_{setup} (See Note a)	HIGH Level Data (See Figure Z)	10			10			ns
	LOW Level Data (See Figure AA)	15			15			ns
Input Hold Time, t_{hold} (See Note b and Figures Z and AA)		0			0			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
(a) Setup time is the interval immediately preceding the positive going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
(b) Hold time is the interval immediately following the positive going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	52 & 53
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	52 & 53
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA	52
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	53
I_{IH}	Input HIGH Current into D			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current into Preset or Clock			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current into Clear into Clear			150	µA	V_{CC} = MAX., V_{IN} = 2.4 V	55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current into Preset or D			–2.0	mA	V_{CC} = MAX. V_{IN} = 5.5 V	54
	Input LOW Current into Clear or Clock			–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	54
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 0 V	56
I_{CC}	Supply Current		30	42	mA	9H74/54H74 V_{CC} = MAX.	55
			30	50	mA	9H74/74H74	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
f_{CLOCK}	Maximum Clock Frequency	35	43		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	Z & AA
t_{PLH}	Turn Off Delay Clear or Preset Inputs to Output			20	ns		Y
t_{PHL}	Turn On Delay Clear or Preset Inputs to Output			30	ns		Y
t_{PLH}	Turn Off Delay Clock Input to Output	4.0	8.5	15	ns		Z & AA
t_{PHL}	Turn On Delay Clock Input to Output	7.0	13	20	ns		Z & AA

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL D TYPE EDGE TRIGGERED FLIP-FLOP

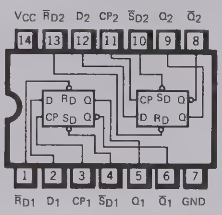
DESCRIPTION — The 9N74/5474, 7474 are edge triggered dual D type flip-flops with direct clear and preset inputs and both Q and $\overline{Q}$ outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. They are designed for use in medium to high speed applications.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out and information present will not be transferred to the output.

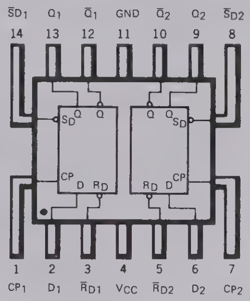
The 9N74/5474, 7474 have the same clocking characteristics as the 9N70/5470, 7470 gated (edge triggered) flip-flop circuits. They can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

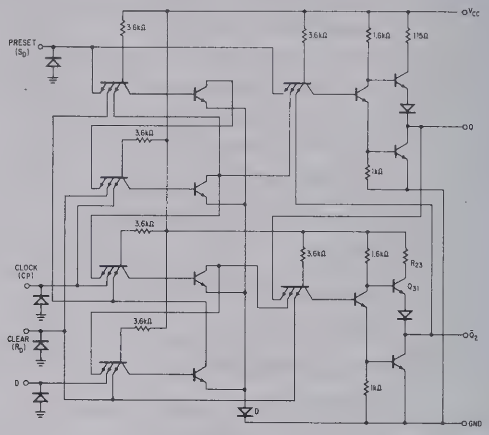

VCC R̄D2 D2 CP2 S̄D2 Q2 Q̄2
14 13 12 11 10 9 8
D RD Q
CP SD Q
CP SD Q
D RD Q
1 2 3 4 5 6 7
R̄D1 D1 CP1 S̄D1 Q1 Q̄1 GND

FLATPAK (TOP VIEW)


S̄D1 Q1 Q̄1 GND Q̄2 Q2 S̄D2
14 13 12 11 10 9 8
SD Q Q
Q Q SD
CP D RD
RD D CP
1 2 3 4 5 6 7
CP1 D1 R̄D1 VCC R̄D2 D2 CP2

Positive logic:
- LOW input to preset sets Q to HIGH level
- LOW input to clear sets Q to LOW level
- Preset and clear are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)


VCC
3.6kΩ
3.6kΩ
1.6kΩ
115Ω
PRESET (SD)
Q
3.6kΩ
1kΩ
3.6kΩ
3.6kΩ
1.6kΩ
R23
Q31
CLOCK (CP)
CLEAR (RD)
3.6kΩ
Q̄
D
1kΩ
D
GND

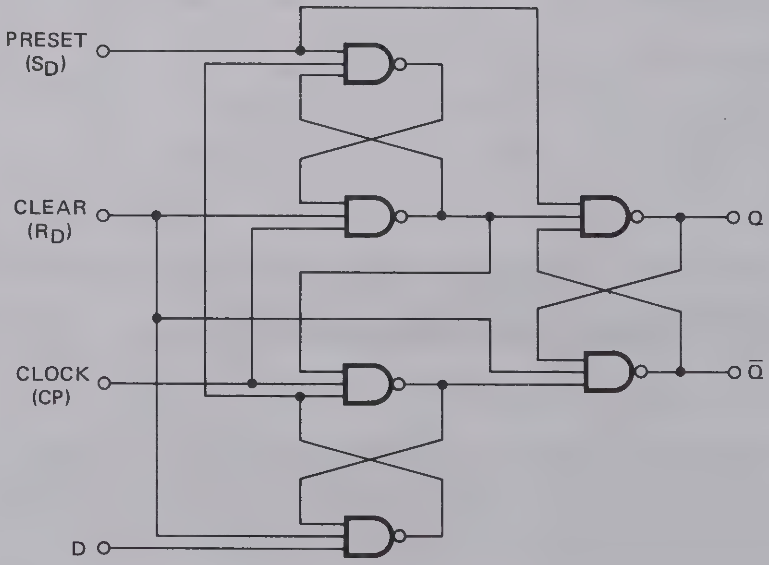
Component values shown are typical.

TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
L	L	H
H	H	L

NOTES:
t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

LOGIC DIAGRAM (EACH FLIP-FLOP)


PRESET (SD)
CLEAR (RD)
CLOCK (CP)
D
Q
Q̄

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N74XM/5474XM			9N74XC/7474XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. G)	30			30			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. C)	30			30			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. C)	30			30			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	52 & 53
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	52 & 53
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA	52
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	53
I_{IH}	Input HIGH Current at D			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset or Clock			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V	55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			120	μA	V_{CC} = MAX., V_{IN} = 2.4 V	55
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input-LOW Current at Preset or D			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	54
	Input LOW Current at Clear or Clock			–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	54
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9N74/5474 V_{CC} = MAX.	56
		–18		–57	mA	9N74/7474 V_{IN} = 0 V	
I_{CC}	Supply Current		17	30	mA	V_{CC} = MAX.	55

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	15	25		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	G
t_{setup}	Maximum Input Setup Time		15	20	ns		G
t_{hold}	Maximum Input Hold Time		2.0	5.0	ns		G
t_{PLH}	Turn Off Delay Clear or Preset to Output			25	ns		C
t_{PHL}	Turn On Delay Clear or Preset to Output			40	ns		C
t_{PLH}	Turn Off Delay Clock to Output	10	14	25	ns		G
t_{PHL}	Turn On Delay Clock to Output	10	20	40	ns		G

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

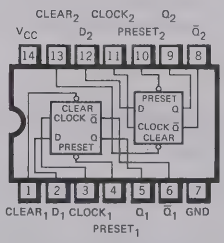
DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

DESCRIPTION – The 9S74/54S74, 74S74 dual edge-triggered flip-flops utilize Schottky TTL circuitry to produce very high speed D-type flip-flops. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. Maximum clock frequency is 100 MHz with a typical power dissipation of 66 mW per flip-flop.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive logic: LOW input to preset sets Q to HIGH level
LOW input to clear resets Q to LOW level
Preset and clear are independent of clock

SYNCHRONOUS TRUTH TABLE (EACH FLIP-FLOP)

t_n	t_{n+1}	
INPUT	OUTPUT	
D	Q	$\overline{Q}$
L	L	H
H	H	L

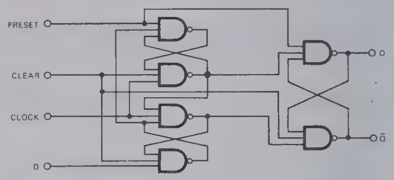
H = HIGH level
L = LOW level
D = Data

NOTES:
A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

ASYNCHRONOUS TRUTH TABLE (EACH FLIP-FLOP)

INPUT		OUTPUT	
Preset	Clear	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

LOGIC DIAGRAM (EACH FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	† 9S74XM/54S74XM			9S74XC/74S74XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

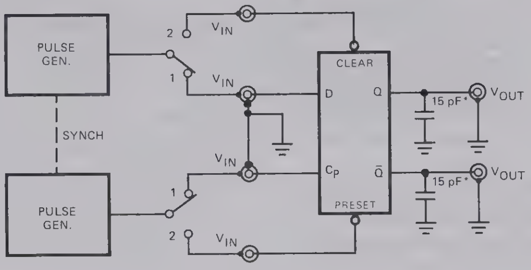
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	D		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
		Preset or Clock		2.0	100		
		Clear		3.0	150		
I_{IL}	Input LOW Current at	D		–1.4	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		Preset or Clock		–2.8	–4.0		
		Clear		–4.2	–6.0		
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. (Note 4)

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with clock and data inputs grounded and either preset or clear inputs grounded.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
f_{max}	Maximum Clock Frequency		100		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH}	Turn Off Delay Clear or Preset to Output		4.0		ns	
t_{PHL}	Turn On Delay Clear or Preset to Output		7.0		ns	
t_{PLH}	Turn Off Delay Clock to Output		7.0		ns	
t_{PHL}	Turn On Delay Clock to Output		7.0		ns	

SWITCHING CHARACTERISTICS


PULSE GEN.
SYNCH
PULSE GEN.
2
1
1
2
V_IN
V_IN
V_IN
V_IN
CLEAR
D
Q
C_P
Q̄
PRESET
15 pF*
15 pF*
V_OUT
V_OUT

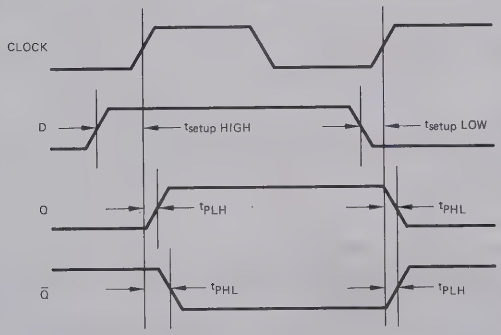
*Includes all probe and jig capacitance.

PULSE GENERATOR SETTINGS

CLOCK	D	DIRECT SET, CLEAR
$f \approx 1$ MHz $t_f = t_r = 2.5$ ns Amp = 0 to 3 V Duty cycle= 50%	$f \approx 500$ kHz $t_f = t_r = 2.5$ ns Amp = 0 to 3 V t_{setup} (HIGH) = 5 ns t_{setup} (LOW) = 4 ns Duty cycle = Adjust pulse width to attain t_{setup} (HIGH) and t_{setup} (LOW) relative to clock as shown in waveforms.	$f \approx 1$ MHz $t_f = t_r = 2.5$ ns Amp = 0 to 3 V Duty cycle =Adjust pulse width and synch to attain waveforms shown.

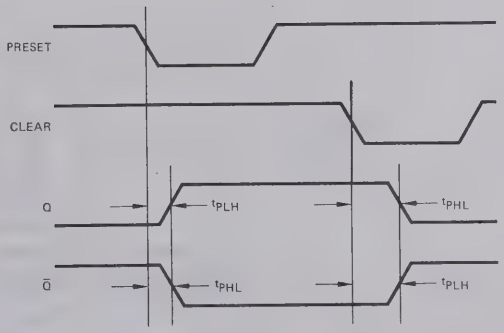
SWITCHING WAVEFORMS

CLOCK TO OUTPUT DELAY[†]


CLOCK
D
t_{setup} HIGH
t_{setup} LOW
Q
t_{PLH}
t_{PHL}
Q̄
t_{PHL}
t_{PLH}

SWITCH IN POSITION 1

DIRECT SET, AND CLEAR TO OUTPUT DELAY


PRESET
CLEAR
Q
t_{PLH}
t_{PHL}
Q̄
t_{PHL}
t_{PLH}

SWITCH IN POSITION 2

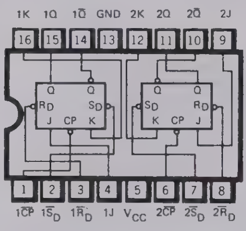
[†] Direct set and clear inputs connected to V_{CC} thru 2 kΩ resistor during test.

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE PRESETS, CLEARS AND CLOCKS

DESCRIPTION — The HSTTL/SSI 9H76/54H76, 74H76 is a High Speed Dual JK Master/Slave flip-flop with separate presets, separate clears and separate clocks. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is a HIGH state.

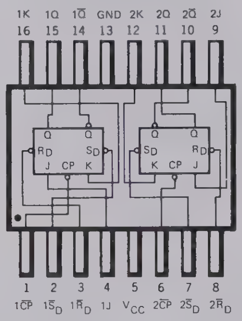
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



1K 1Q 1Q̄ GND 2K 2Q 2Q̄ 2J
16 15 14 13 12 11 10 9
Q Q̄ R̄D S̄D J CP K
Q Q̄ S̄D R̄D K CP J
1 2 3 4 5 6 7 8
1C̄P 1S̄D 1R̄D 1J VCC 2C̄P 2S̄D 2R̄D

FLATPAK (TOP VIEW)

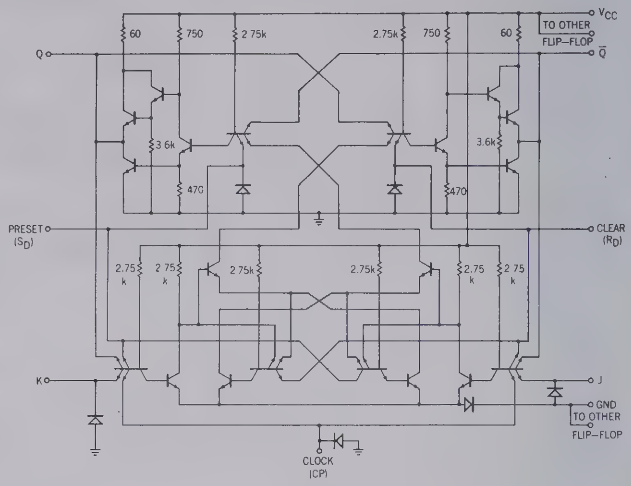


1K 1Q 1Q̄ GND 2K 2Q 2Q̄ 2J
16 15 14 13 12 11 10 9
Q Q̄ R̄D S̄D J CP K
Q Q̄ S̄D R̄D K CP J
1 2 3 4 5 6 7 8
1C̄P 1S̄D 1R̄D 1J VCC 2C̄P 2S̄D 2R̄D

Positive logic:

LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Clear and preset are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)



VCC
TO OTHER FLIP–FLOP
60
750
2.75k
2.75k
750
60
Q
Q̄
3.6k
3.6k
470
470
PRESET (SD)
CLEAR (RD)
2.75 k
2.75 k
2.75k
2.75k
2.75 k
2.75 k
K
J
GND
TO OTHER FLIP–FLOP
CLOCK (CP)

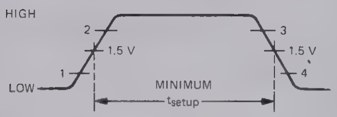
Component values shown are typical.

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

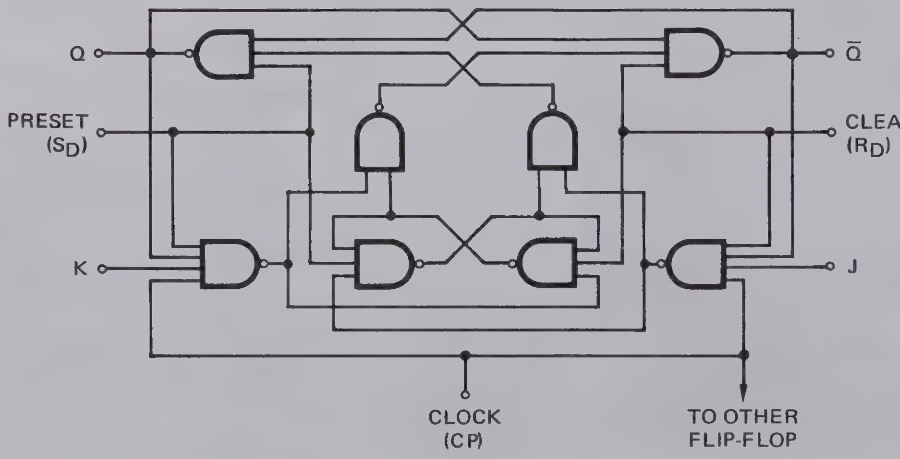
NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



HIGH
LOW
1
2
3
4
1.5 V
1.5 V
MINIMUM
tsetup

LOGIC DIAGRAM
(EACH FLIP-FLOP)



Q
Q̄
PRESET (SD)
CLEAR (RD)
K
J
CLOCK (CP)
TO OTHER FLIP-FLOP

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H76XM/54H76XM			9H76XC/74H76XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)	16			16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	46
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J, K or Clock			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear or Preset			100	μA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K or Clock			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clear or Preset			−4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0	50
I_{CC}	Supply Current		32	50	mA	V_{CC} = MAX., V_{IN} = 4.5 V	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear or Preset to Output		6.0	13	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output		12	24	ns		X
t_{PLH}	Turn Off Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn on Delay Clock to Output	10	22	27	ns		W

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

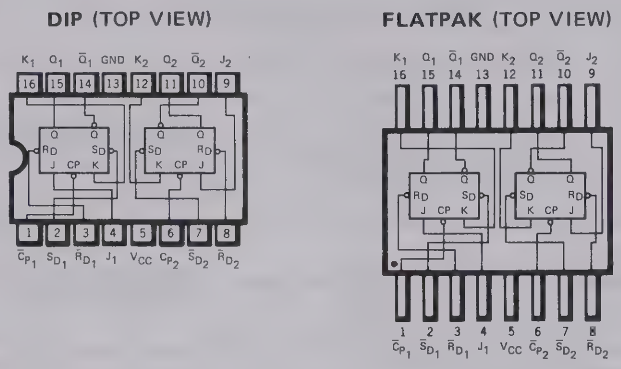
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE PRESETS, CLEARS AND CLOCKS

DESCRIPTION – The TTL/SSI 9N76/5476, 7476 is a Dual JK Master/Slave flip-flop with separate presets, separate clears and separate clocks. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave.

LOGIC AND CONNECTION DIAGRAM

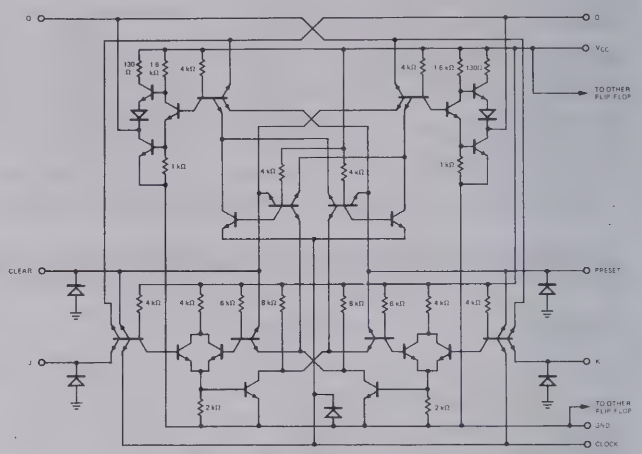

DIP (TOP VIEW)

FLATPAK (TOP VIEW)

K1 Q1 Q̄1 GND K2 Q2 Q̄2 J2
16 15 14 13 12 11 10 9
Q Q̄ R̄D S̄D J CP K
Q̄ Q S̄D R̄D K CP J
1 2 3 4 5 6 7 8
C̄P1 S̄D1 R̄D1 J1 VCC C̄P2 S̄D2 R̄D2

Positive logic:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Clear and preset are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)


Q
Q̄
VCC
TO OTHER FLIP FLOP
130 Ω
1.6 kΩ
4 kΩ
1 kΩ
CLEAR
PRESET
6 kΩ
8 kΩ
2 kΩ
J
K
GND
CLOCK

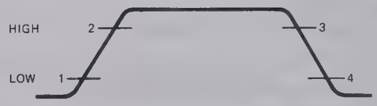
Component values shown are typical.

TRUTH TABLE

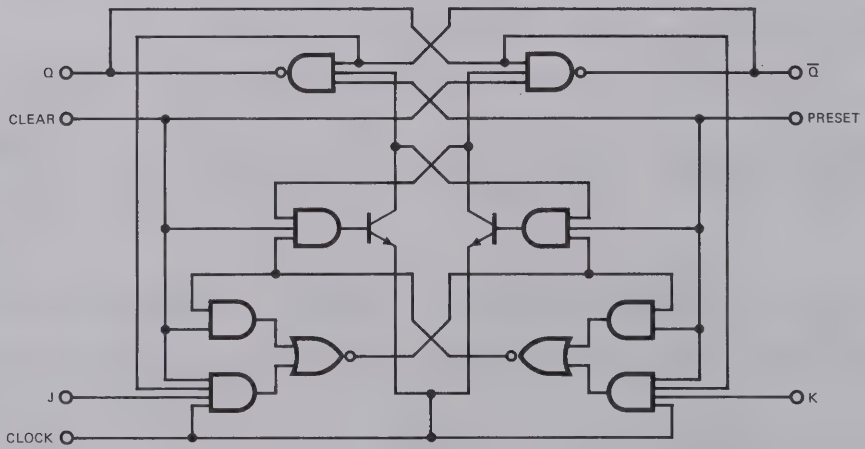
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM


HIGH
LOW
1
2
3
4

LOGIC DIAGRAM
(EACH FLIP-FLOP)


Q
CLEAR
J
CLOCK
Q̄
PRESET
K

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N76XM/5476XM			9N76XC/7476XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. E)	20			20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. F)	25			25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. F)	25			25			ns
Input Setup Time, t_{setup} (See Fig. E)	$\geqslant t_{p(clock)}$			$\geqslant t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA	46
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	47
I_{IH}	Input HIGH Current at J or K			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	49
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear, Preset or Clock			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V	49
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J or K			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	48
	Input LOW Current at Clear, Preset, or Clock			–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	48
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9N76/5476 V_{CC} = MAX.	51
		–18		–57	mA	9N76/7476 V_{IN} = 0 V	
I_{CC}	Supply Current		20	40	mA	V_{CC} = MAX.	49

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	15	20		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	E
t_{PLH}	Turn Off Delay Clear or Preset to Output		16	25	ns		F
t_{PHL}	Turn On Delay Clear or Preset to Output		25	40	ns		F
t_{PLH}	Turn Off Delay Clock to Output	10	16	25	ns		E
t_{PHL}	Turn On Delay Clock to Output	10	25	40	ns		E

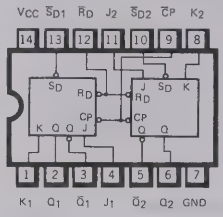
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Note more than one output should be shorted at a time.

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE PRESETS, AND A COMMON CLEAR AND CLOCK

DESCRIPTION — The HSTTL/SSI 9H78/54H78, 74H78 is a High Speed Dual JK Master/Slave flip-flop with separate presets, a common clear and a common clock. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

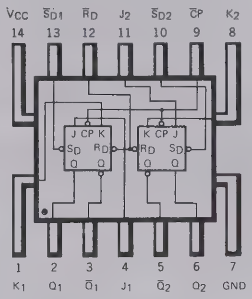
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



V_{CC} $\overline{S}_{D1}$ $\overline{R}_D$ J_2 $\overline{S}_{D2}$ $\overline{CP}$ K_2
14 13 12 11 10 9 8
S_D R_D CP K Q $\overline{Q}$ J
J S_D K R_D CP Q $\overline{Q}$
1 2 3 4 5 6 7
K_1 Q_1 $\overline{Q}_1$ J_1 $\overline{Q}_2$ Q_2 GND

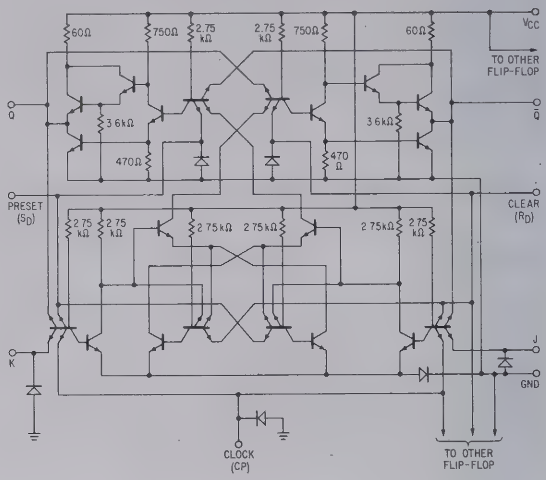
FLATPAK (TOP VIEW)



V_{CC} $\overline{S}_{D1}$ $\overline{R}_D$ J_2 $\overline{S}_{D2}$ $\overline{CP}$ K_2
14 13 12 11 10 9 8
J CP K S_D R_D Q $\overline{Q}$
K CP J R_D S_D Q $\overline{Q}$
1 2 3 4 5 6 7
K_1 Q_1 $\overline{Q}_1$ J_1 $\overline{Q}_2$ Q_2 GND

Positive logic:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP FLOP)



60Ω
750Ω
2.75 kΩ
2.75 kΩ
750Ω
60Ω
V_{CC}
TO OTHER FLIP-FLOP
Q
$\overline{Q}$
3.6kΩ
3.6kΩ
470Ω
470 Ω
PRESET (S_D)
CLEAR (R_D)
2.75 kΩ
2.75 kΩ
2.75 kΩ
2.75 kΩ
2.75 kΩ
2.75 kΩ
K
J
GND
CLOCK (CP)
TO OTHER FLIP-FLOP

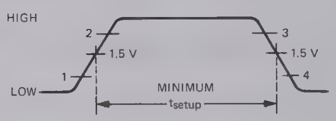
Component values shown are typical.

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

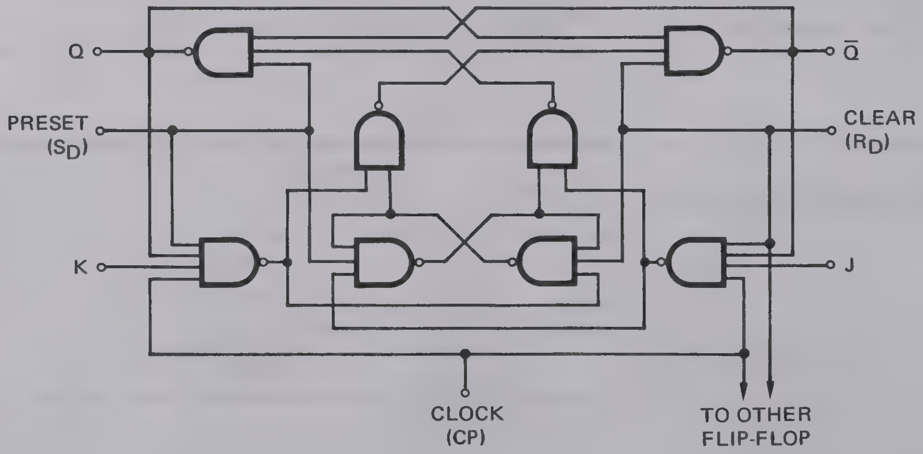
NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



HIGH
LOW
1
2
3
4
1.5 V
1.5 V
MINIMUM
t_{setup}

LOGIC DIAGRAM
(EACH FLIP-FLOP)



Q
$\overline{Q}$
PRESET (S_D)
CLEAR (R_D)
K
J
CLOCK (CP)
TO OTHER FLIP-FLOP

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9H78XM/54H78XM			9H78XC/74H78XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Fan Out from Each Output			12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)	12			12			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)	16			16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)	16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	46 & 47
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	46
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset or Clock			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			200	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J or K			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Preset or Clock			−4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clear			−8.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0V	51
I_{CC}	Supply Current		32	50	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	25	30		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear to Output		6	13	ns		X
t_{PHL}	Turn On Delay Clear to Output		12	24	ns		X
t_{PLH}	Turn On Delay Clock to Output	6.0	14	21	ns		W
t_{PHL}	Turn On Delay Clock to Output	10	22	27	ns		W

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

LPTTL/SSI 9L86

LOW POWER QUAD EXCLUSIVE OR GATE

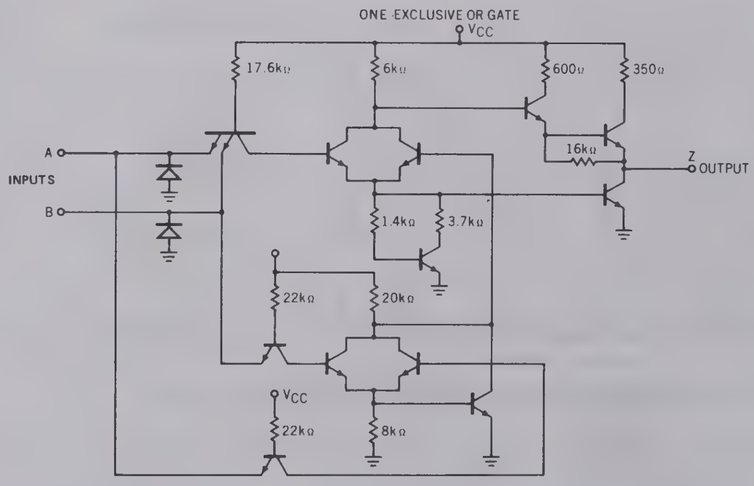
DESCRIPTION — The Low Power TTL/SSI 9L86 consists of four Exclusive OR Gates. Designed for low power, medium speed operation, the 9L86 is useful in large number of code conversion, parity generation/checking and comparison applications. The exclusive OR gate produces an output when the inputs are complementary. The Boolean expression for the device is: $Z = A\overline{B} + \overline{A}B$.

- **TYPICAL PROPAGATION DELAY OF 25 ns**
- **TYPICAL POWER DISSIPATION OF 25 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 14-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

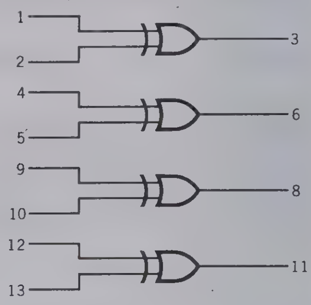
PIN NAMES	LOADING	
	HIGH	LOW
INPUTS (Pins 1, 2, 4, 5, 9, 10, 12, 13)	0.75 U.L.	0.38 U.L.
OUTPUTS (Pins 3, 6, 8, 11)	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

SCHEMATIC DIAGRAM

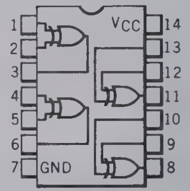

ONE EXCLUSIVE OR GATE
VCC
17.6kΩ
6kΩ
600Ω
350Ω
A
INPUTS
B
16kΩ
Z
OUTPUT
1.4kΩ
3.7kΩ
22kΩ
20kΩ
VCC
22kΩ
8kΩ

LOGIC SYMBOL

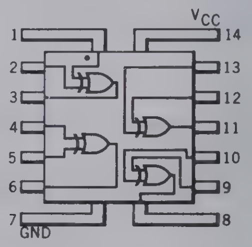

1
2
3
4
5
6
9
10
8
12
13
11

V_{CC} = PIN 14
GND = PIN 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1
2
3
4
5
6
7
GND
VCC
14
13
12
11
10
9
8

FLATPAK (TOP VIEW)


VCC
1
2
3
4
5
6
7
GND
14
13
12
11
10
9
8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9L86XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9L86XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted) (See Notes 1, 2 & 3)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP. Note 3	MAX.			
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IN} = V_{IL} or V_{IH} per Truth Table	
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH voltage for all inputs	
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input LOW voltage for all inputs	
I_{IL}	Input LOW Current		−0.48	−0.6	mA	V_{CC} = MAX., V_{IN} = 0.3 V, other input = 4.5 V	
I_{IH}	Input HIGH Current		6.0	30	µA	V_{CC} = MAX., V_{IN} = 2.4 V	other input = 0.0 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{SC}*	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V, "A" inputs = 0.0 V, "B" inputs = 4.5 V	
I_{CC}	Power Supply Current		6.8	9.5	mA	V_{CC} = MAX., All inputs = 0.0 V	
			3.4	5.0	mA	V_{CC} = MAX., "A" inputs = 4.5 V, "B" inputs = 0.0 V	
			6.3	9.0	mA	V_{CC} = MAX., All inputs = 4.5 V	

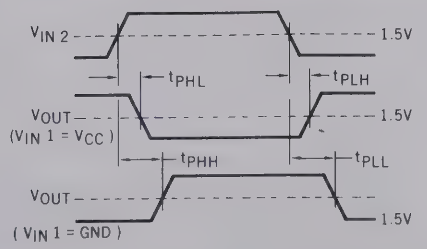
NOTES:
1. Conditions for testing, not shown in the Table, are chose to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

* Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	9L86XM			9L86XC			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
t_{PLH}	Switching Times	8	15	20	8	15	25	ns	V_{IN1} = 5.0 V	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}		10	25	35	10	25	40	ns		
t_{PHH}	Switching Times	12	25	40	12	25	40	ns	V_{IN1} = 0.0 V	
t_{PLL}		20	35	45	20	35	50	ns		

SWITCHING TIME WAVEFORMS



TRUTH TABLE

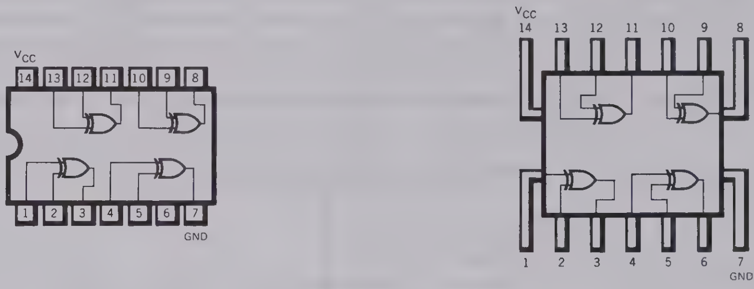
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

QUAD 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION – The TTL/SSI 9N86/5486, 7486 is a Quad 2-input Exclusive OR gate designed to perform the function: $Y = A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to the HIGH level.

Input clamping diodes are provided to minimize transmission line effects. On chip input buffers are also provided to lower the fan in requirement to only 1 U.L. (unit load). The 9N86/5486, 7486 is fully compatible with all members of the Fairchild TTL family.

LOGIC AND CONNECTION DIAGRAM



DIP (TOP VIEW)

FLATPAK (TOP VIEW)

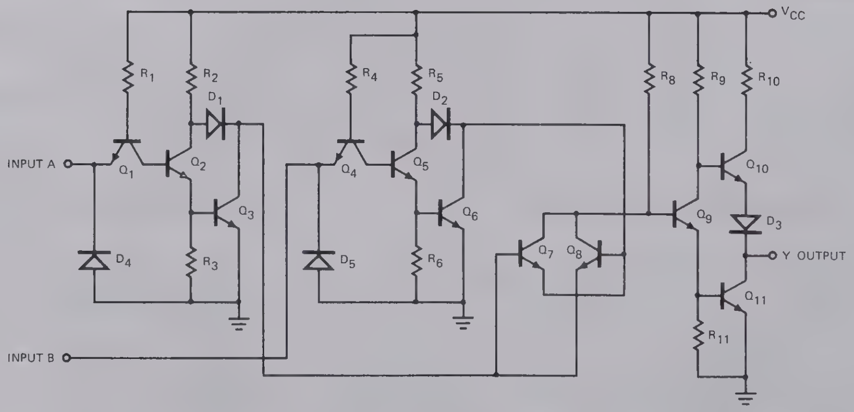
V_{CC}
14
13
12
11
10
9
8
1
2
3
4
5
6
7
GND

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Positive logic: $Y = A \oplus B$

SCHEMATIC DIAGRAM



V_{CC}
R_1
R_2
D_1
R_4
R_5
D_2
R_8
R_9
R_{10}
INPUT A
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
Q_8
Q_9
Q_{10}
D_3
D_4
R_3
D_5
R_6
Y OUTPUT
Q_{11}
R_{11}
INPUT B

1/4 of Circuit shown.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9N86XM/5486XM			9N86XC/7486XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output N	LOW Level			10			10	U.L.
	HIGH Level			20			20	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		98
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		98
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −800 µA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		98
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		99
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	(Each Input)	100
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V (Each Input)		101
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9N86/5486	V_{CC} = MAX., V_{IH} = 4.5 V V_{IL} = 0 V	102
		−18		−55	mA	9N86/7486		
I_{CC}	Supply Current		30	43	mA	9N86/5486	V_{CC} = MAX., V_{IN} = 4.5 V	103
			30	50	mA	9N86/7486		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay Input to Output		15	23	ns	Other Input Low	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	S
			18	30		Other Input High		
t_{PHL}	Turn On Delay Input to Output		11	17		Other Input Low		
			13	22		Other Input High		

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

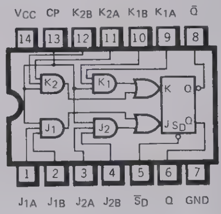
(3) Not more than one output should be shorted at a time.

JK EDGE TRIGGERED FLIP-FLOP WITH AND-OR INPUTS

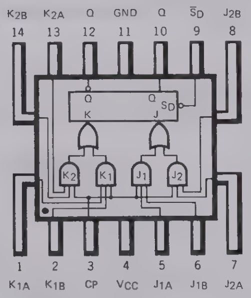
DESCRIPTION — The HSTTL/SSI 9H101/54H101, 74H101 is a High Speed JK Negative Edge Triggered flip-flop. The AND-OR gate inputs are inhibited while the clock input is LOW; when the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

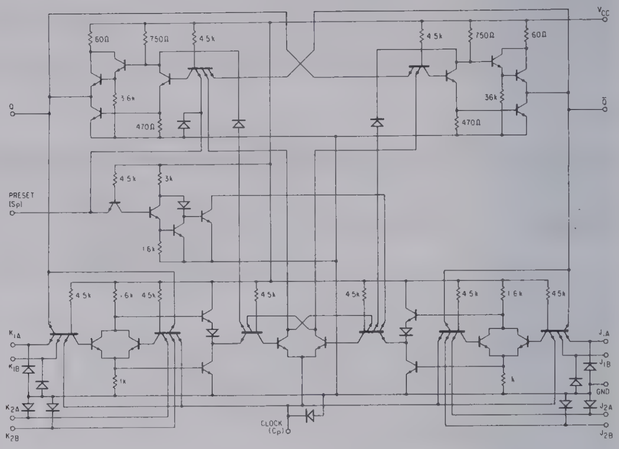

VCC CP K2B K2A K1B K1A Q̄
14 13 12 11 10 9 8
K2 K1 K Q̄
J1 J2 J SD Q
1 2 3 4 5 6 7
J1A J1B J2A J2B S̄D Q GND

FLATPAK (TOP VIEW)


K2B K2A Q GND Q S̄D J2B
14 13 12 11 10 9 8
Q̄ Q SD
K J
K2 K1 J1 J2
1 2 3 4 5 6 7
K1A K1B CP VCC J1A J1B J2A

Positive logic:
LOW input to preset sets Q to HIGH level
Preset is independent of clock

SCHEMATIC DIAGRAM

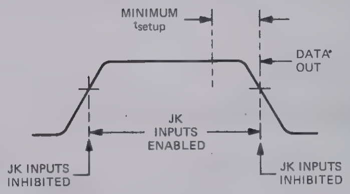

VCC
60Ω
750Ω
4.5k
3.6k
470Ω
36k
Q
Q̄
PRESET (SD)
3k
1.6k
K1A
K1B
K2A
K2B
J1A
J1B
J2A
J2B
GND
CLOCK (CP)

TRUTH TABLE

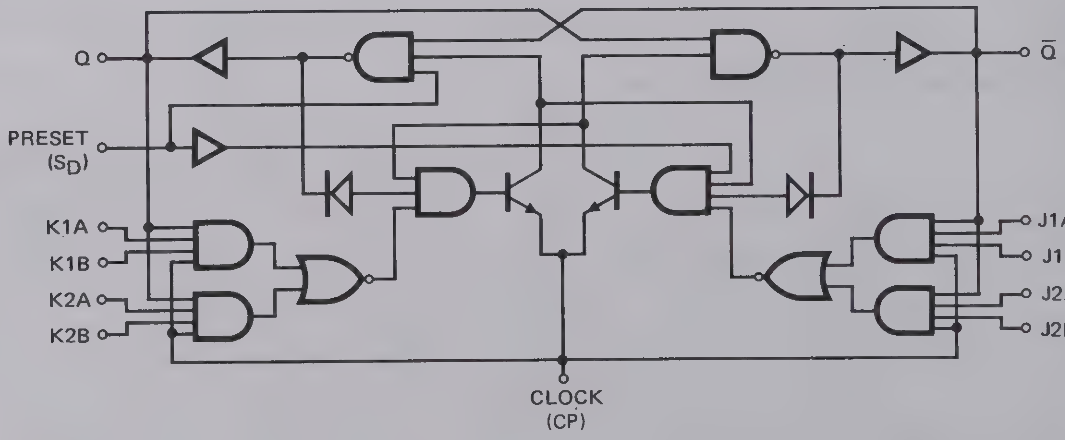
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	Q_n

NOTES:
J = (J1A·J1B) + (J2A·J2B)
K = (k1A·K1B) + (K2A·K2B)
t_n = Bit time before clock
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM


MINIMUM t_{setup}
DATA OUT
JK INPUTS ENABLED
JK INPUTS INHIBITED
JK INPUTS INHIBITED

LOGIC DIAGRAM


Q
Q̄
PRESET (SD)
K1A
K1B
K2A
K2B
J1A
J1B
J2A
J2B
CLOCK (CP)

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H101XM/54H101XM			9H101XC/74H101XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)		16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	121&122
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	121&122
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = –0.5 mA	121
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	122
I_{IH}	Input HIGH Current at J or K			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		–1.0	mA	V_{CC} = MAX., V_{IN} = 2.4V	124
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, or Preset		–1.0	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
	Input LOW Current at Clock		–3.0	–4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V	123
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 0 V	127
I_{CC}	Supply Current		20	38	mA	V_{CC} = MAX.	124

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Preset to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Preset to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

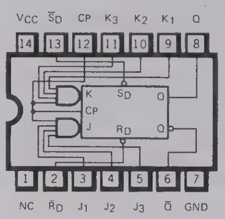
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

JK EDGE TRIGGERED FLIP-FLOP WITH AND INPUTS

DESCRIPTION — The HSTTL/SSI 9H102/54102, 74H102 is a High Speed JK Negative Edge Triggered flip-flop. They feature gated JK inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is LOW; when the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

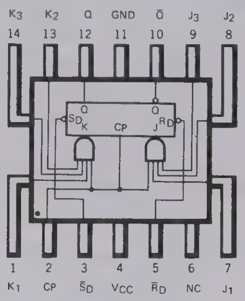
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

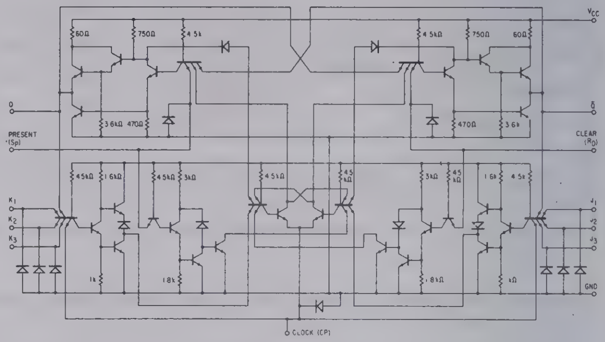

VCC
S̄D
CP
K3
K2
K1
Q
14
13
12
11
10
9
8
K
SD
Q
CP
J
RD
Q̄
1
2
3
4
5
6
7
NC
R̄D
J1
J2
J3
Q̄
GND

NC — No internal connection.

FLATPAK (TOP VIEW)


K3
K2
Q
GND
Q̄
J3
J2
14
13
12
11
10
9
8
SD
Q
K
CP
Q̄
RD
J
1
2
3
4
5
6
7
K1
CP
S̄D
VCC
R̄D
NC
J1

SCHEMATIC DIAGRAM


VCC
Q
PRESENT (SD)
Q̄
CLEAR (RD)
K1
K2
K3
J1
J2
J3
GND
CLOCK (CP)

Positive logic:

LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

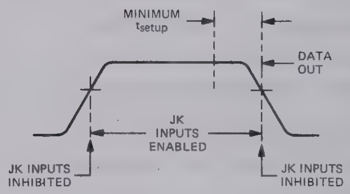
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

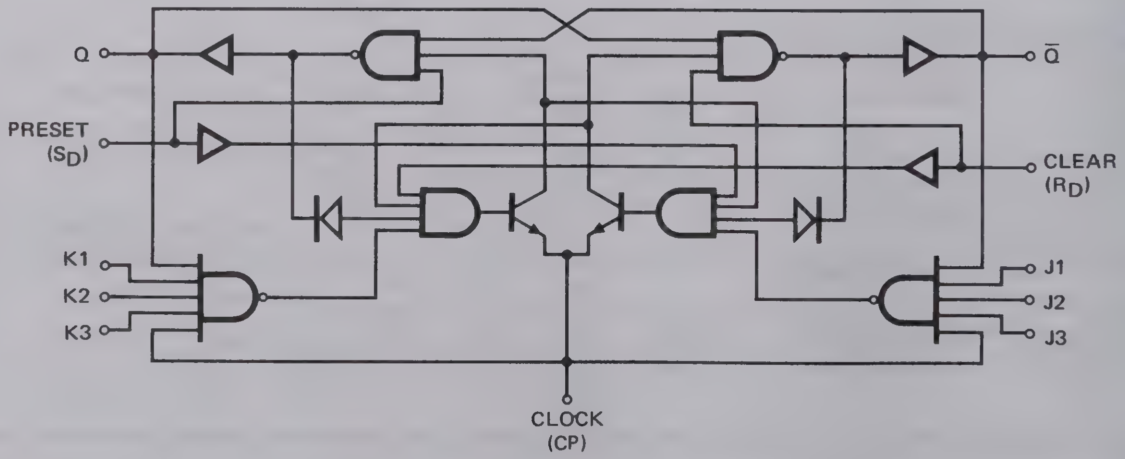
NOTES:

J = J1·J2·J3
K = K1·K2·K3
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM


MINIMUM tsetup
DATA OUT
JK INPUTS ENABLED
JK INPUTS INHIBITED
JK INPUTS INHIBITED

LOGIC DIAGRAM


Q
PRESET (SD)
K1
K2
K3
Q̄
CLEAR (RD)
J1
J2
J3
CLOCK (CP)

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H102XM/54H102XM			9H102XC/74H102XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)		15			15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)		15			15			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 1)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	41 & 42
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	41 & 42
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	41
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	42
I_{IH}	Input HIGH Current at J1, J2, J3 K1, K2, or K3			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		−1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset or Clear			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	44
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J1, J2, J3 K1, K2, K3, Preset, or Clear		−1.0	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
	Input LOW Current at Clock		−3.0	−4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V	43
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0 V	45
I_{CC}	Supply Current		20	38	mA	V_{CC} = MAX.	44

SWITCHING CHARACTERISTICS (T_A = 25°)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

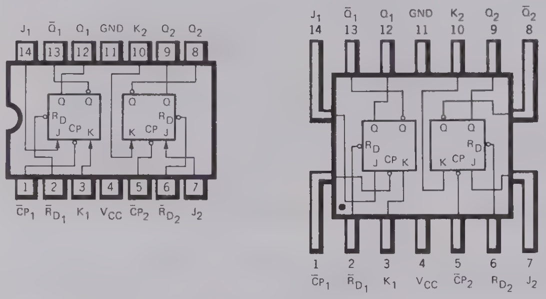
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

DUAL JK EDGE TRIGGERED FLIP-FLOP WITH SEPARATE CLEARS AND CLOCKS

DESCRIPTION — The HSTTL/SSI 9H103/54H103, 74H103 is a High Speed JK Negative Edge Triggered flip-flop. They feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

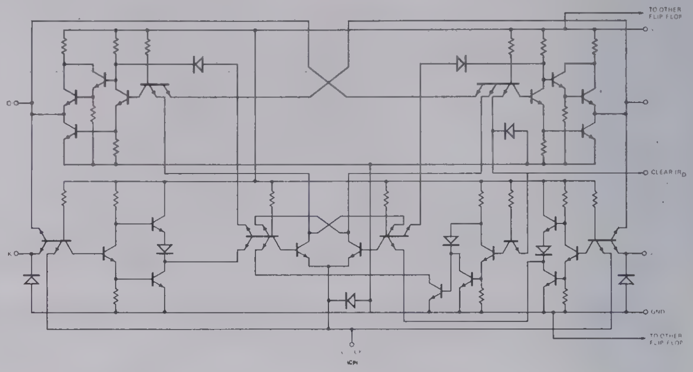
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW) **FLATPAK** (TOP VIEW)


J1 Q̄1 Q1 GND K2 Q2 Q̄2
14 13 12 11 10 9 8
Q Q̄ RD J CP K
Q Q̄ RD K CP J
1 2 3 4 5 6 7
C̄P1 R̄D1 K1 VCC C̄P2 R̄D2 J2

Positive logic: LOW input to clear sets Q to LOW level
Clear is independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)

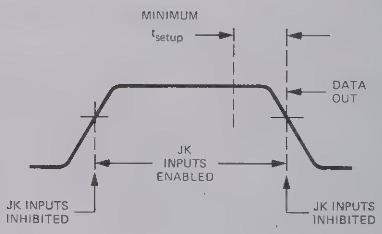

TO OTHER FLIP FLOP
Q
Q̄
CLEAR RD
K
J
GND
VCC
TO OTHER FLIP FLOP

TRUTH TABLE

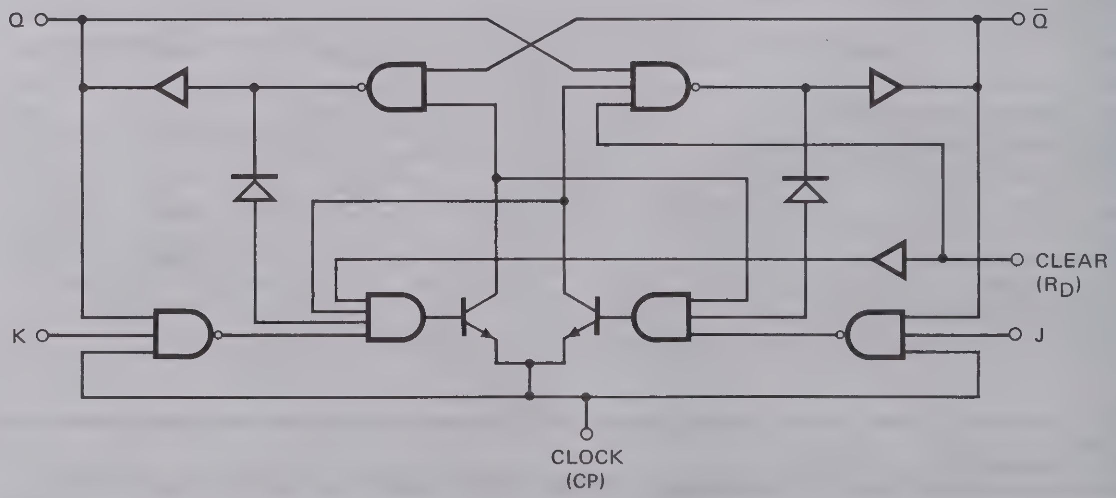
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM


MINIMUM
t_{setup}
DATA OUT
JK INPUTS ENABLED
JK INPUTS INHIBITED
JK INPUTS INHIBITED

LOGIC DIAGRAM
(EACH FLIP-FLOP)


Q
Q̄
CLEAR
(RD)
K
J
CLOCK
(CP)

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H103XM/54H103XM			9H103XC/74H103XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)		16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = –0.5 mA	46
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		–1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			100	μA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K, or Clear		–1.0	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clock		–3.0	–4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 0 V	50
I_{CC}	Supply Current		40	76	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

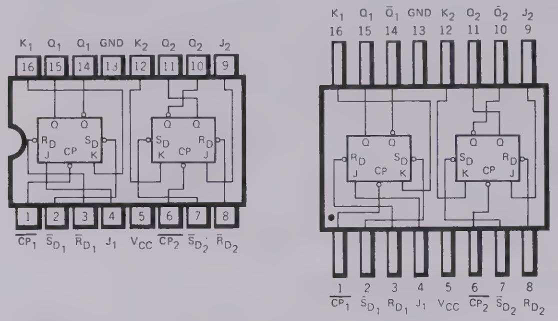
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Clear to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Clear to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Clear to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

DUAL JK EDGE TRIGGERED FLIP-FLOP WITH SEPARATE PRESETS, CLEARS AND CLOCKS

DESCRIPTION — The HSTTL/SSI 9H106/54H106, 74H106 is a High Speed JK Negative Edge Triggered flip-flop. They feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM

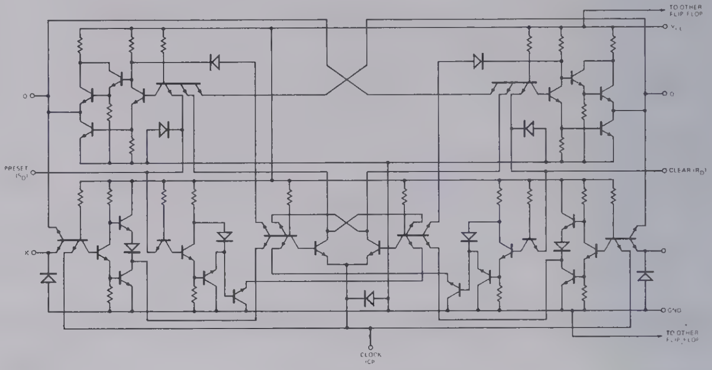

DIP (TOP VIEW)

FLATPAK (Top View)

K1 Q1 Q̄1 GND K2 Q2 Q̄2 J2
16 15 14 13 12 11 10 9
Q Q̄ RD SD J CP K
Q Q̄ SD RD K CP J
1 2 3 4 5 6 7 8
C̄P̄1 S̄D1 R̄D1 J1 VCC C̄P̄2 S̄D2 R̄D2

Positive logic: LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)

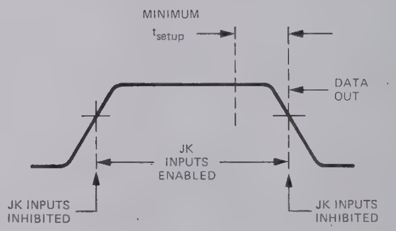

TO OTHER FLIP FLOP
VCC
Q
Q̄
PRESET (SD)
CLEAR (RD)
K
J
GND
TO OTHER FLIP FLOP
CLOCK (CP)

TRUTH TABLE

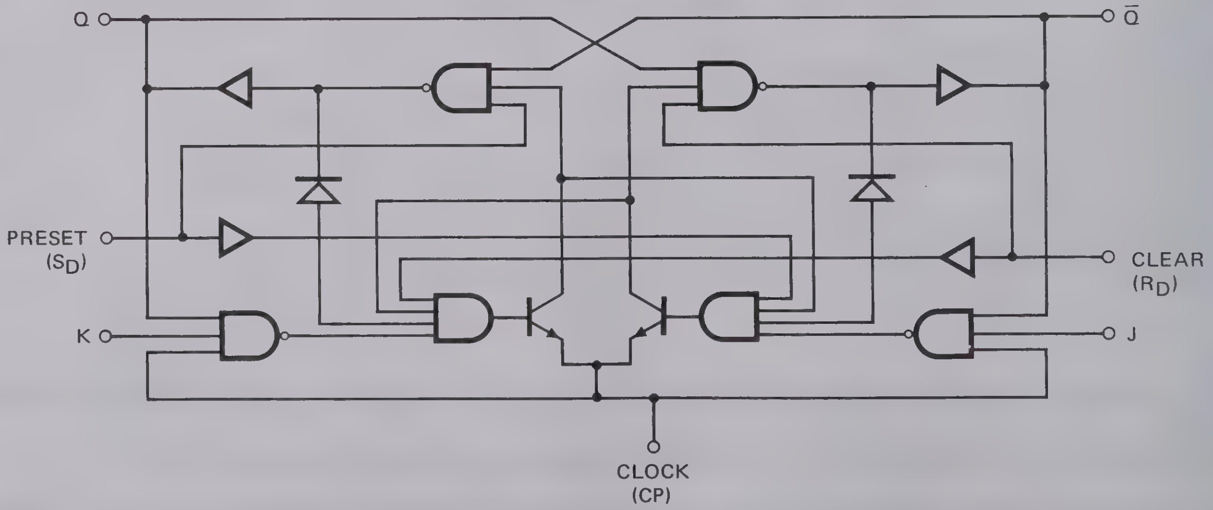
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM


MINIMUM
t_{setup}
DATA OUT
JK INPUTS ENABLED
JK INPUTS INHIBITED
JK INPUTS INHIBITED

LOGIC DIAGRAM
(EACH FLIP-FLOP)


Q
Q̄
PRESET (SD)
K
CLEAR (RD)
J
CLOCK (CP)

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H106XM/54H106XM			9H106XC/74H106XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)		16			16			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)		16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = −0.5 mA	46
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		−1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset or Clear			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K, Preset, or Clear		−1.0	−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clock		−3.0	−4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{IN} = 0 V	51
I_{CC}	Supply Current		40	76	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°)

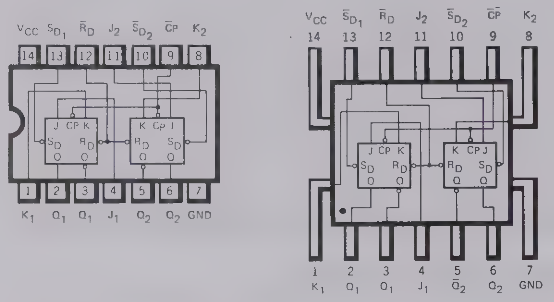
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset or Clear to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

DUAL JK EDGE TRIGGERED FLIP-FLOP WITH SEPARATE PRESETS AND A COMMON CLEAR AND CLOCK

DESCRIPTION — The HSTTL/SSI 9H108/54H108, 74H108 is a High Speed JK Negative Edge Triggered flip-flop. They feature individual J,K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes HIGH, the inputs are enabled and data will be accepted. Logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

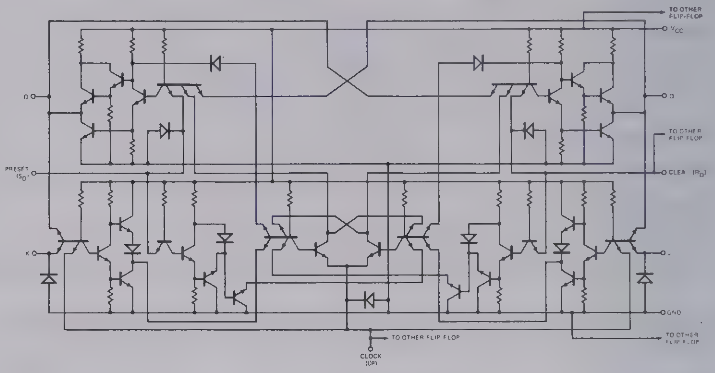
LOGIC AND CONNECTION DIAGRAM


DIP (TOP VIEW)

FLATPAK (TOP VIEW)
V_{CC}
$\overline{S}_{D1}$
$\overline{R}_D$
J_2
$\overline{S}_{D2}$
$\overline{CP}$
K_2
14
13
12
11
10
9
8
J CP K
S_D R_D
Q $\overline{Q}$
K CP J
R_D S_D
1
2
3
4
5
6
7
K_1
Q_1
$\overline{Q}_1$
J_1
$\overline{Q}_2$
Q_2
GND

Positive logic: LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

SCHEMATIC DIAGRAM
(EACH FLIP—FLOP)

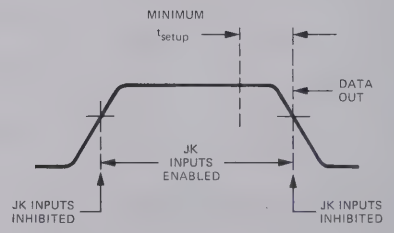

TO OTHER FLIP-FLOP
V_{CC}
Q
$\overline{Q}$
TO OTHER FLIP FLOP
PRESET (S_D)
CLEAR (R_D)
K
J
GND
TO OTHER FLIP FLOP
TO OTHER FLIP FLOP
CLOCK (CP)

TRUTH TABLE

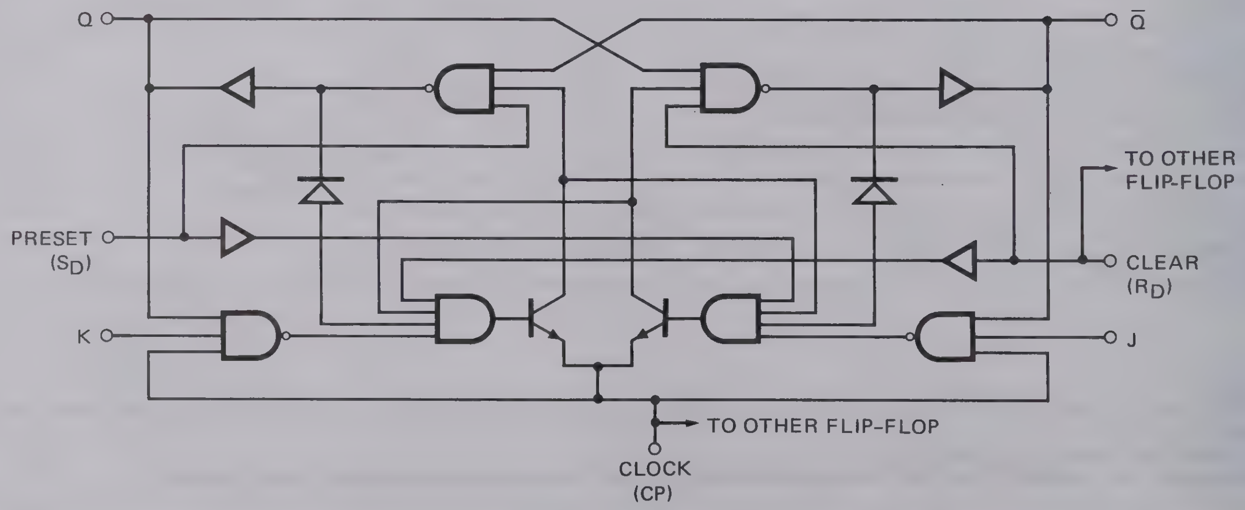
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM


MINIMUM t_{setup}
DATA OUT
JK INPUTS ENABLED
JK INPUTS INHIBITED
JK INPUTS INHIBITED

LOGIC DIAGRAM
(EACH FLIP—FLOP)


Q
$\overline{Q}$
TO OTHER FLIP-FLOP
PRESET (S_D)
CLEAR (R_D)
K
J
TO OTHER FLIP-FLOP
CLOCK (CP)

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9H108XM/54H108XM			9H108XC/74H108XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Fan Out from Each Output				12.5			12.5	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. W)		10			10			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Fig. X)		15			15			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Fig. X)		16			16			ns
Input Setup Time, t_{setup} (See Clock Waveform)	LOW Level	13			13			ns
	HIGH Level	10			10			
Input Hold Time, t_{hold}		0			0			
Clock Pulse Transition Time, t_0 (See Fig. W)				150			150	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH	46 & 47
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW	46 & 47
V_{OH}	Output HIGH Voltage	2.4	3.2		Volts	V_{CC} = MIN., I_{OH} = –0.5 mA	46
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA	47
I_{IH}	Input HIGH Current at J or K			50	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clock	0		–1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset			100	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Clear			200	µA	V_{CC} = MAX., V_{IN} = 2.4 V	126
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at J, K, or Preset		–1.0	–2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clock		–6.0	–9.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
	Input LOW Current at Clear		–2.0	–4.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	125
I_{OS}	Output Short Circuit Current (Note 3)	–40		–100	mA	V_{CC} = MAX., V_{IN} = 0 V	51
I_{CC}	Supply Current		40	76	mA	V_{CC} = MAX.	126

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{CLOCK}	Maximum Clock Frequency	40	50		MHz	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	W
t_{PLH}	Turn Off Delay Preset or Clear to Output		8.0	12	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock LOW)		23	35	ns		X
t_{PHL}	Turn On Delay Clear or Preset to Output (Clock HIGH)		15	20	ns		X
t_{PLH}	Turn Off Delay Clock to Output	5.0	10	15	ns		W
t_{PHL}	Turn On Delay Clock to Output	8.0	16	20	ns		W

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

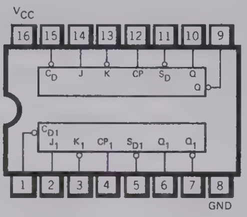
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

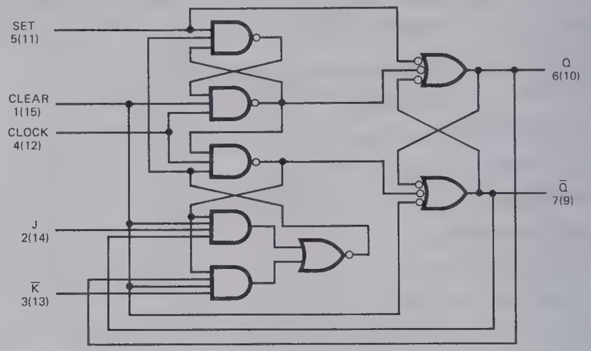
DUAL J$\overline{K}$ FLIP-FLOP

DESCRIPTION — The 9S109 consists of two high speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together. The 9S109 is a pin for pin replacement of the 9024.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

SYNCHRONOUS ENTRY J-$\overline{K}$ MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

L = LOW Logic Level
H = HIGH Logic Level

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
$\overline{S}_D$	$\overline{C}_D$	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S109XM			9S109XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_I = –18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	J$\overline{K}$		1.0	50	µA	V_{CC} = MAX., V_{IN} = 2.7 V
		$\overline{S}_D$		2.0	100		
		$\overline{C}_D$		4.0	200		
I_{IL}	Input LOW Current at	J$\overline{K}$		-1.4	-2.0	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		$\overline{S}_D$		-2.8	-4.0		
		$\overline{C}_D$		-5.6	-8.0		
I_{OS}	Output Short Circuit Current (Note 3)		–40	-65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			32	52	mA	V_{CC} = MAX., (Note 4)

Notes on following page

SWITCHING CHARACTERISTICS ($T_A = 25^\circ C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Clock Frequency		100		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH}	Turn Off Delay Clear or Preset to Output		4.0		ns	
t_{PHL}	Turn On Delay Clear or Preset to Output		7.0		ns	
t_{PLH}	Turn Off Delay Clock to Output		7.0		ns	
t_{PHL}	Turn On Delay Clock to Output		7.0		ns	

NOTES:

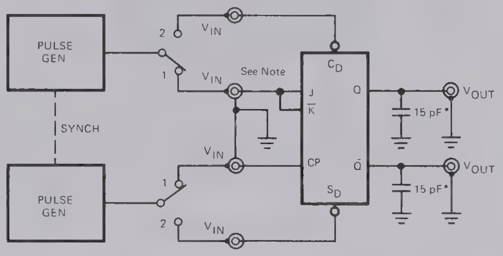
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at $V_{CC} = 5.0$ V, 25°C.

(3) Not more than one output should be shorted at a time.

(4) I_{CC} is measured Clock, Set and $\overline{K}$ inputs grounded.

SWITCHING CHARACTERISTICS


PULSE GEN
SYNCH
PULSE GEN
2
1
1
2
V_{IN}
V_{IN}
V_{IN}
V_{IN}
See Note
C_D
J
$\overline{K}$
CP
S_D
Q
$\overline{Q}$
15 pF*
15 pF*
V_{OUT}
V_{OUT}

*Includes all probe and jig capacitance.

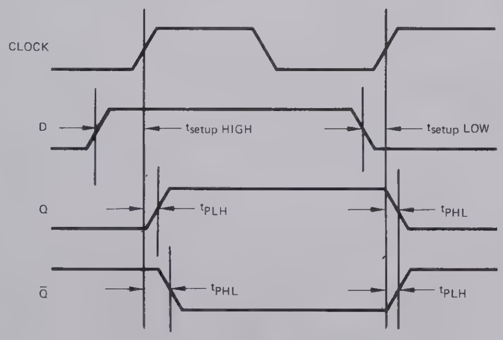
NOTE: For testing 9S109, connect J,$\overline{K}$ pins together to form a D input.

PULSE GENERATOR SETTINGS

CLOCK	J$\overline{K}$	DIRECT SET, CLEAR
f ≈ 1 MHz $t_f = t_r = 2.5$ ns Amp = 0 to 3 V Duty cycle = 50%	f ≈ 500 kHz $t_f = t_r = 2.5$ ns Amp = 0 to 3 V t_{setup} (HIGH) t_{setup} (LOW) Duty cycle = Adjust pulse width to attain t_{setup} (HIGH) and t_{setup} (LOW) relative to clock as shown in waveforms.	f ≈ 1 MHz $t_f = t_r = 2.5$ ns Amp = 0 to 3 V Duty cycle = Adjust pulse width and synch to attain waveforms shown.

SWITCHING WAVEFORMS

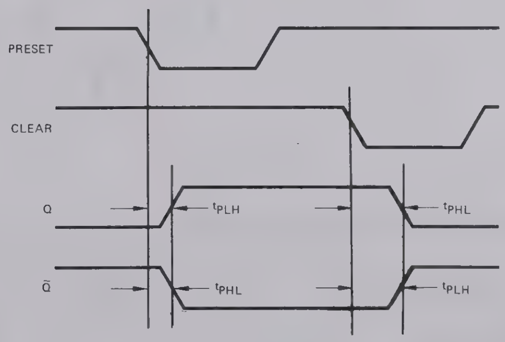
CLOCK TO OUTPUT DELAY†


CLOCK
D
Q
$\overline{Q}$
t_{setup} HIGH
t_{setup} LOW
t_{PLH}
t_{PHL}
t_{PHL}
t_{PLH}

SWITCH IN POSITION 1

†Direct set and clear inputs connected to V_{CC} thru 2 kΩ resistor during test.

DIRECT SET, AND CLEAR TO OUTPUT DELAY

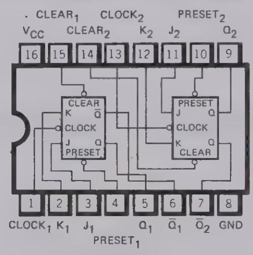

PRESET
CLEAR
Q
$\overline{Q}$
t_{PLH}
t_{PHL}
t_{PHL}
t_{PLH}

SWITCH IN POSITION 2

DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 9S112/54S112, 74S112 dual JK flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



CLEAR₁
CLOCK₂
PRESET₂
VCC
CLEAR₂
K₂
J₂
Q₂
16
15
14
13
12
11
10
9
CLEAR
K
Q̄
CLOCK
J
Q
PRESET
PRESET
J
Q
CLOCK
K
Q
CLEAR
1
2
3
4
5
6
7
8
CLOCK₁
K₁
J₁
PRESET₁
Q₁
Q̄₁
Q̄₂
GND

Positive logic: LOW input to preset sets Q to HIGH level.
LOW input to clear resets Q to LOW level.
Clear and preset are independent of clock.

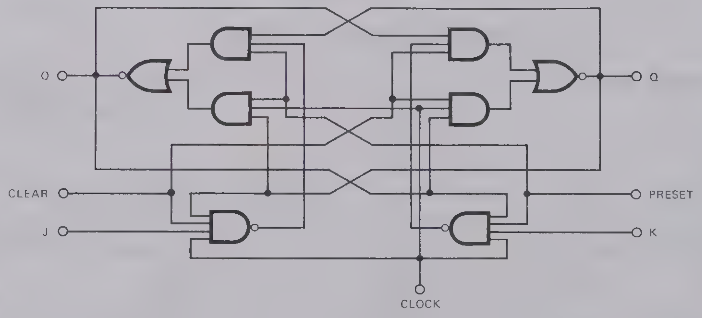
TRUTH TABLES

t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Preset	Clear	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

NOTES:
A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.

LOGIC DIAGRAM
(Each Flip-Flop)



O
Q
CLEAR
PRESET
J
K
CLOCK

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S112XM/54S112XM			9S112XC/74S112XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	75	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.2	Volts	V_{CC} = MIN., $I_I = -18$ mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., $I_{OH} = -1.0$ mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., $I_{OL} = 20$ mA
I_{IH}	Input HIGH Current at	J,K		1.0	50	μA	V_{CC} = MAX., $V_{IN} = 2.7$ V
		Clock Preset Clear		2.0	100		
I_{IL}	Input LOW Current at	J,K		−0.96	−1.6	mA	V_{CC} = MAX., $V_{IN} = 0.5$ V
		Clock		−2.8	−4.0		
		Preset Clear		−4.9	−7.0		
I_{OS}	Output Short Circuit Current (Note 3)		−40	−65	−100	mA	V_{CC} = MAX., $V_{OUT} = 0$V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. (Note 4)

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

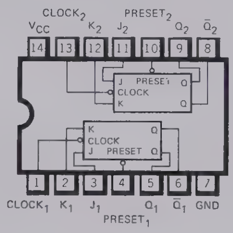
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Clock Frequency	80	125		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH}	Turn Off Delay Clear or Preset to Output			7.0	ns	
t_{PHL}	Turn On Delay Clear or Preset to Output			7.0	ns	
t_{PLH}	Turn Off Delay Clock to Output			7.0	ns	
t_{PHL}	Turn On Delay Clock to Output			7.0	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at $V_{CC} = 5.0$ V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with outputs open, clock grounded and J,K, preset and clear at 4.5 V.

DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION – The 9S113/54S113, 74S113 offer individual J, K, preset, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)


CLOCK$_2$
PRESET$_2$
V$_{CC}$
K$_2$
J$_2$
Q$_2$
$\bar{Q}_2$
14
13
12
11
10
9
8
J PRESET Q
CLOCK
K Q
K Q
CLOCK
J PRESET Q
1
2
3
4
5
6
7
CLOCK$_1$
K$_1$
J$_1$
Q$_1$
$\bar{Q}_1$
GND
PRESET$_1$

Positive logic: LOW input to preset sets Q to HIGH level
Preset is independent of clock

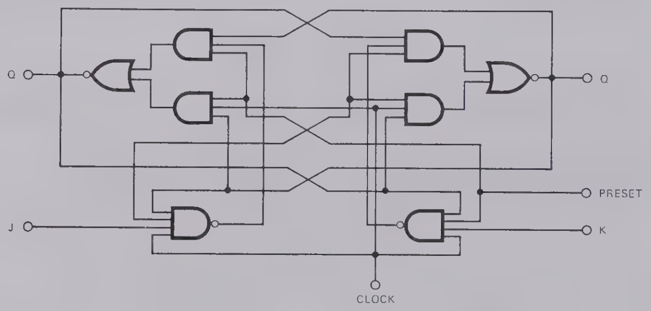
TRUTH TABLES

t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Preset	Q	$\bar{Q}$
L	H	L
H	No Change	

NOTES:
A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.

LOGIC DIAGRAM
(Each Flip-Flop)


Q
Q
J
PRESET
K
CLOCK

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S113XM/54S113XM			9S113XC/74S113XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_I = –18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., I_{OH} = –1.0 mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	J,K		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
		Clock		2.0	100		
		Preset		2.0	100		
I_{IL}	Input LOW Current at	J,K		–0.96	–1.6	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		Clock		–2.8	–4.0		
		Preset		–4.9	–7.0		
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. (Note 4)

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Clock Frequency	80	125		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Turn Off Delay Clear or Preset to Output			7.0	ns	
t_{PHL}	Turn On Delay Clear or Preset to Output			7.0	ns	
t_{PLH}	Turn Off Delay Clock to Output			7.0	ns	
t_{PHL}	Turn On Delay Clock to Output			7.0	ns	

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

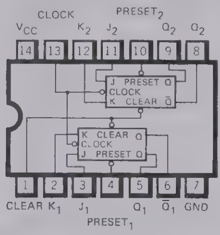
(3) Not more than one output should be shorted at a time.

(4) I_{CC} is measured with outputs open, clock grounded and J,K, preset and clear at 4.5 V.

DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 9S114/54S114, 74S114 offer common clock and common clear inputs and individual J, K, and preset inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)


CLOCK
PRESET2
VCC
K2
J2
Q2
Q̄2
14
13
12
11
10
9
8
J PRESET Q
CLOCK
K CLEAR Q̄
K CLEAR Q
CLOCK
J PRESET Q̄
1
2
3
4
5
6
7
CLEAR
K1
J1
Q1
Q̄1
GND
PRESET1

Positive logic: LOW input to preset sets Q to HIGH level.
LOW input to clear resets Q to LOW level.
Preset and clear are independent of clock.

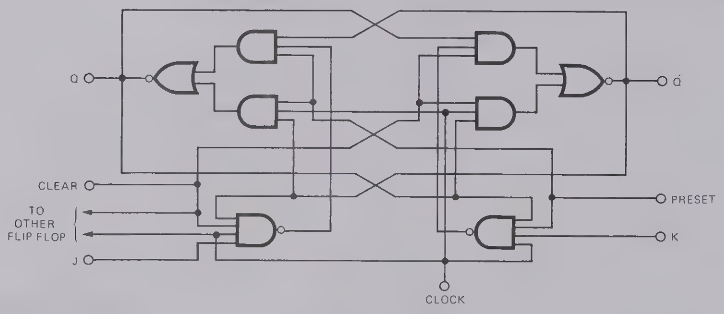
TRUTH TABLES

t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Preset	Clear	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Charge	

NOTES:
A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.

LOGIC DIAGRAM
(Each Flip-Flop)


Q
Q̄
CLEAR
TO OTHER FLIP FLOP
J
PRESET
K
CLOCK

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S114XM/54S114XM			9S114XC/74S114XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 2)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., $I_I = -18$ mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		Volts	V_{CC} = MIN., $I_{OH} = -1.0$ mA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage			0.35	0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA
I_{IH}	Input HIGH Current at	JK		1.0	50	μA	V_{CC} = MAX., V_{IN} = 2.7 V
		Clock		4.0	200		
		Preset		2.0	100		
		Clear		4.0	200		
I_{IL}	Input LOW Current at	JK		–0.96	–1.6	mA	V_{CC} = MAX., V_{IN} = 0.5 V
		Clock		–5.6	–8.0		
		Preset		–4.9	–7.0		
		Clear		–9.8	–14		
I_{OS}	Output Short Circuit Current (Note 3)		–40	–65	–100	mA	V_{CC} = MAX., V_{OUT} = 0V
I_{CC}	Supply Current			30	50	mA	V_{CC} = MAX. (Note 4)

SWITCHING CHARACTERISTICS (T_A = 25° C)

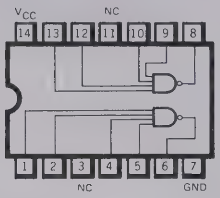
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
f_{max}	Maximum Clock Frequency	80	125		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Turn Off Delay Clear or Preset to Output			7.0	ns	
t_{PHL}	Turn On Delay Clear or Preset to Output			7.0	ns	
t_{PLH}	Turn Off Delay Clock to Output			7.0	ns	
t_{PHL}	Turn On Delay Clock to Output			7.0	ns	

Notes:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with outputs open, clock grounded and J, K, preset and clear at 4.5 V.

DUAL 4-INPUT NAND LINE DRIVER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

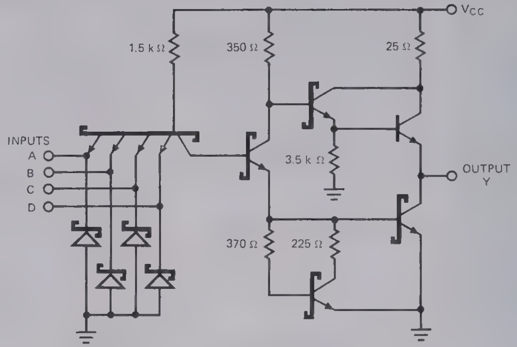


Positive logic: $Y = \overline{ABCD}$

NC—No internal connection.

SCHEMATIC DIAGRAM

(EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9S140XM/54S140XM			9S140XC/74S140XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	75	°C
Fan Out From Each Output			37.5*			37.5*	U.L.

*37.5 (U.L.) is the LOW drive factor and 75 (U.L.) is the HIGH drive factor.
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.2	Volts	V_{CC} = MIN., I_{IN} = -18mA	
V_{OH}	Output HIGH Voltage	XM	2.0	2.8		Volts	V_{CC} = MIN., V_{IN} = 0.5V, R_0 = 50Ω to Gnd	
		XC	2.0	2.8				
V_{OL}	Output LOW Voltage			0.4	0.5	Volts	V_{CC} = MIN., I_{OL} = 60mA, V_{IN} = 2.0V	
I_{IH}	Input HIGH Current			1.0	100	μA	V_{CC} = MAX., V_{IN} = 2.7V	Each Input
					1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V	
I_{IL}	Input LOW Current			–2.5	–4.0	mA	V_{CC} = MAX., V_{IN} = 0.5V	Each Input
I_{OS}	Output Short Circuit Current (Note 3)		–50	–150	–225	mA	V_{CC} = MAX., V_{OUT} = 0V	
I_{CCH}	Supply Current HIGH			8.2	18.0	mA	V_{CC} = MAX., V_{IN} = 0V	
I_{CCL}	Supply Current LOW			27.2	44.0	mA	V_{CC} = MAX., Inputs Open	

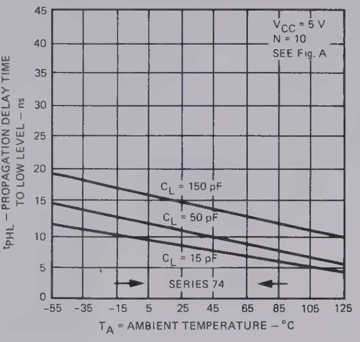
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURES
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output	2.0	4.0	6.5	ns	V_{CC} = 5.0V C_L = 50pF	DD
t_{PHL}	Turn On Delay Input to Output	2.0	4.0	6.5	ns		

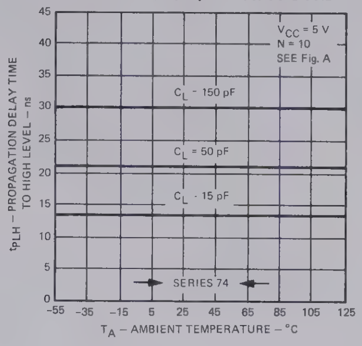
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

9N/54,74
TYPICAL CHARACTERISTICS*

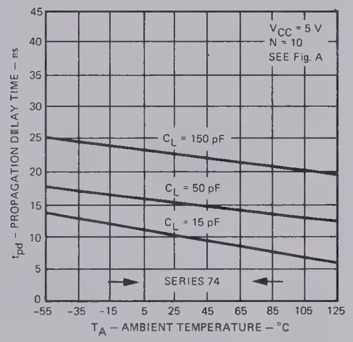
PROPAGATION DELAY TIME TO LOW LEVEL VERSUS AMBIENT TEMPERATURE



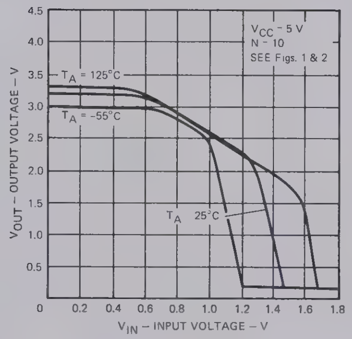
PROPAGATION DELAY TIME TO HIGH LEVEL VERSUS AMBIENT TEMPERATURE



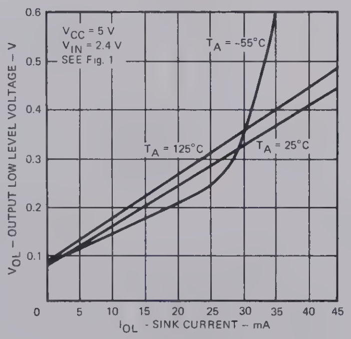
PROPAGATION DELAY TIME VERSUS AMBIENT TEMPERATURE



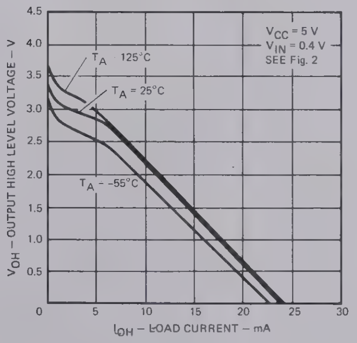
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



LOW LEVEL OUTPUT VOLTAGE VERSUS SINK CURRENT



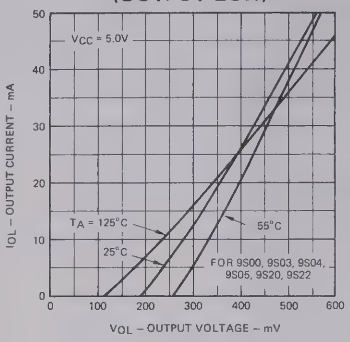
HIGH LEVEL OUTPUT VOLTAGE VERSUS LOAD CURRENT



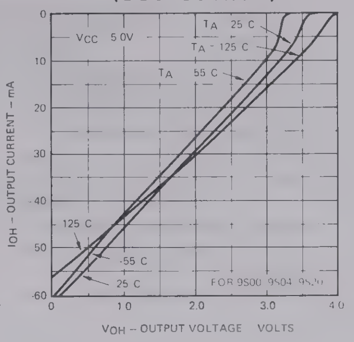
*Unless otherwise noted, data as shown is applicable for: 9N00/5400, 7400; 9N02/5402, 7402; 9N04/5404, 7404; 9N10/5410, 7410; 9N20/5420, 7420; 9N30/5430, 7430; 9N50/5450, 7450; 9N51/5451, 7451; 9N53/5453, 7453; 9N54/5454, 7454.

9S/54S,74S
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

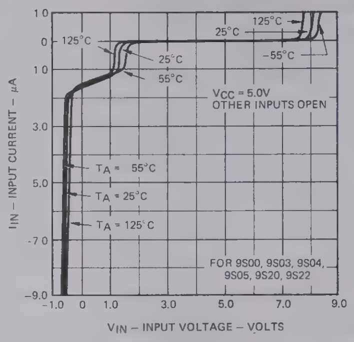
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



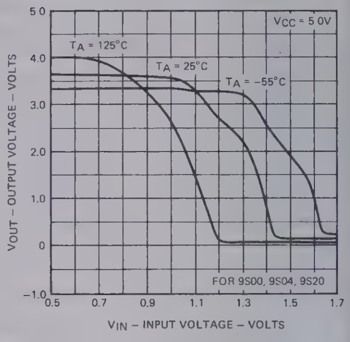
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



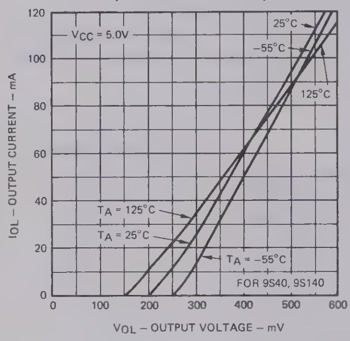
INPUT CURRENT VERSUS INPUT VOLTAGE



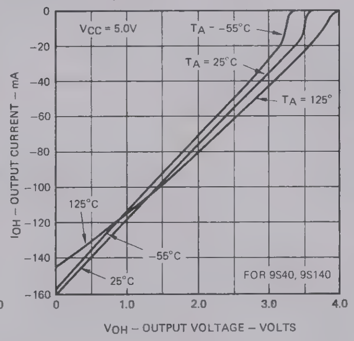
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



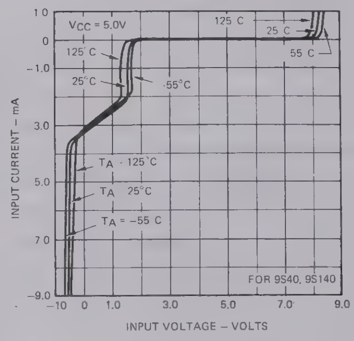
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



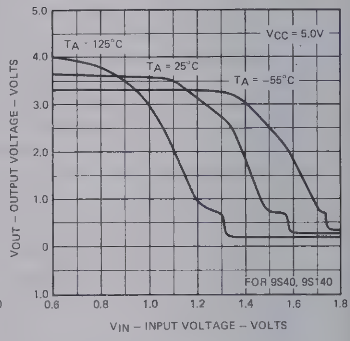
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



INPUT CURRENT VERSUS INPUT VOLTAGE

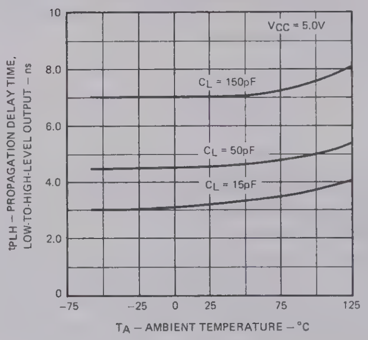


OUTPUT VOLTAGE VERSUS INPUT VOLTAGE

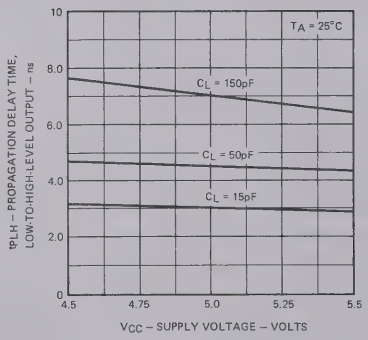


TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS
FOR 9S GATES, BUFFER, AND INVERTER

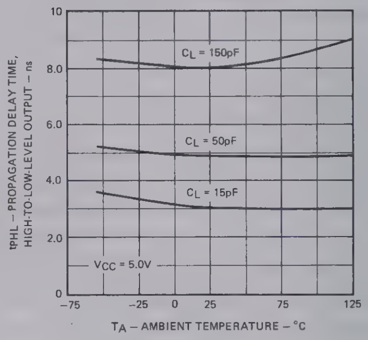
PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUPUT VERSUS FREE-AIR TEMPERATURE



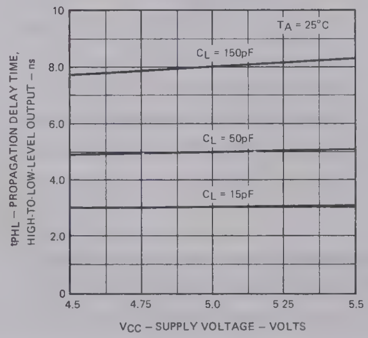
PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT VERSUS SUPPLY VOLTAGE



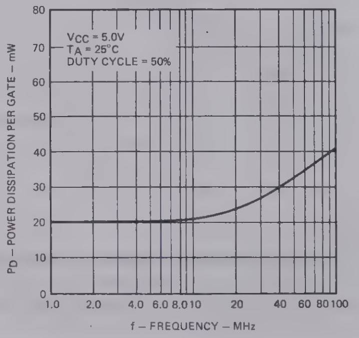
PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT VERSUS FREE-AIR TEMPERATURE

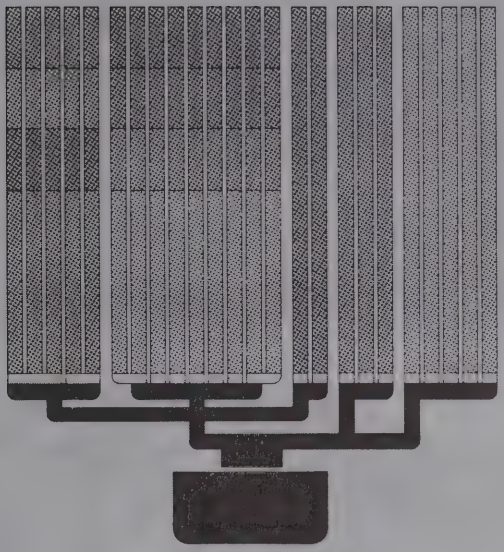


PROPAGATION DELAY TIME, HIGH-TO-LOW LEVEL OUTPUT VERSUS SUPPLY VOLTAGE



POWER DISSIPATION PER GATE VERSUS FREQUENCY

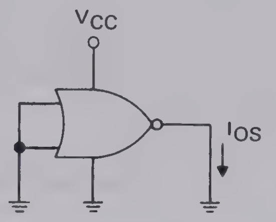




SSI
Switching and dc Test Circuits

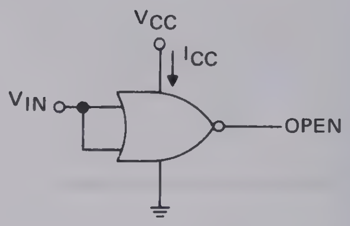
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



1. Each gate is tested separately.

Fig. 13


V_CC
I_CC
V_IN
OPEN

1. Low level and high level conditions are tested.
2. All gates are tested simultaneously.

Fig. 14

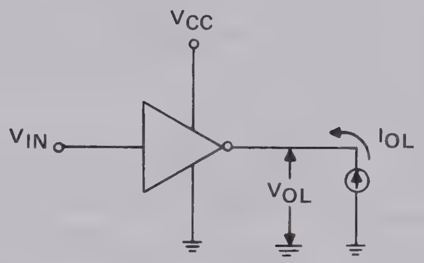

V_CC
V_IN
I_OL
V_OL

Fig. 15

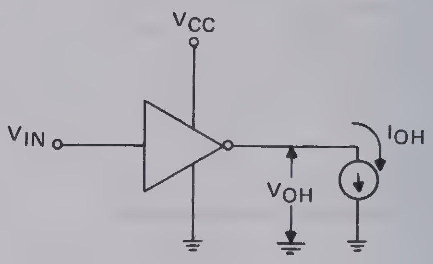

V_CC
V_IN
I_OH
V_OH

Fig. 16

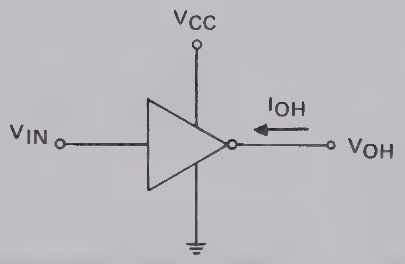

V_CC
I_OH
V_IN
V_OH

Fig. 17

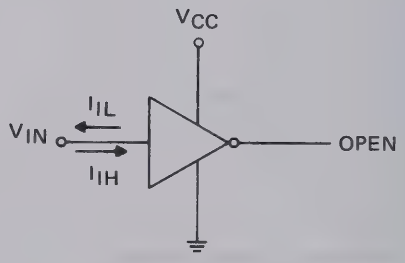
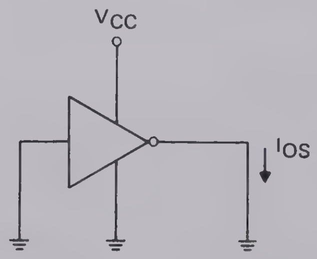
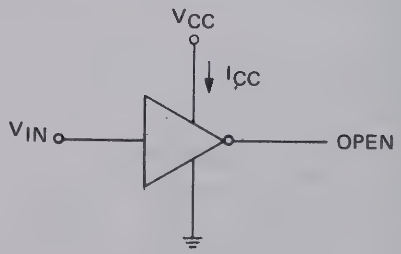

V_CC
I_IL
V_IN
I_IH
OPEN

Fig. 18



1. Each inverter is tested separately.

Fig. 19


V_CC
I_CC
V_IN
OPEN

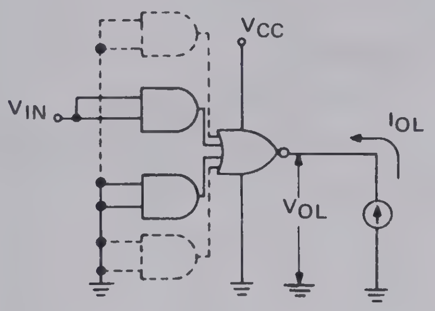
1. All inverters are tested simultaneously.

Fig. 20

*Arrows indicate actual direction of current flow.

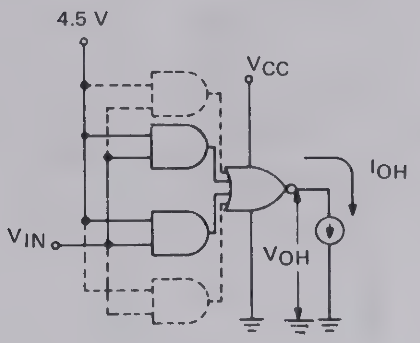
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)


VCC
VIN
IOL
VOL

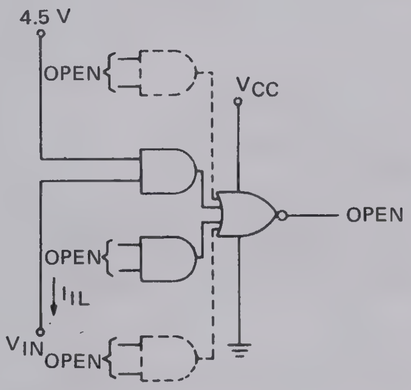
1. Each AND section is tested separately.

Fig. 21


4.5 V
VCC
IOH
VIN
VOH

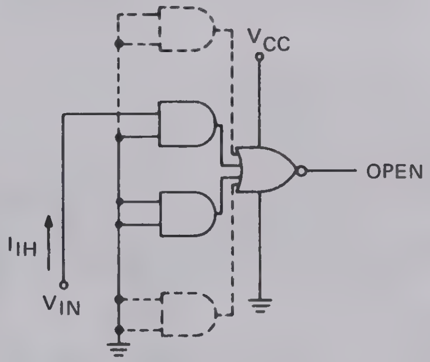
1. Each pair of inputs is tested separately.

Fig. 22


4.5 V
OPEN
VCC
OPEN
OPEN
IIL
VIN
OPEN

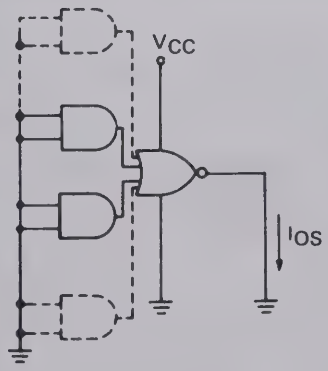
1. Each input is tested separately.

Fig. 23


VCC
OPEN
IIH
VIN

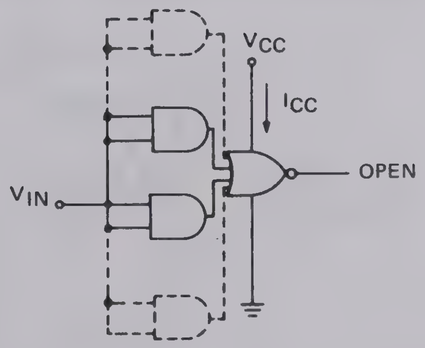
1. Each input is tested separately.

Fig. 24



1. Each gate is tested separately.

Fig. 25


VCC
ICC
OPEN
VIN

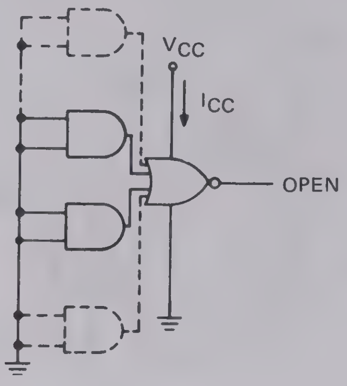
1. All gates are tested simultaneously.

Fig. 26

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

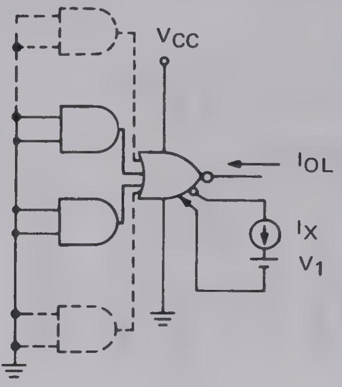
DC TEST CIRCUITS* (Continued)



V_{CC}
I_{CC}
OPEN

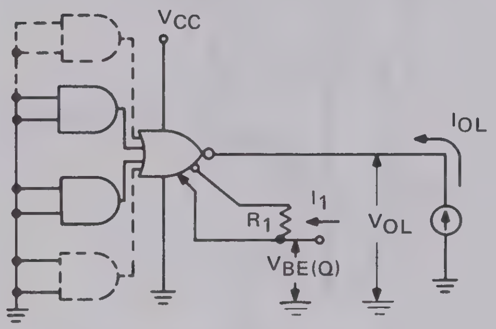
1. All gates are tested simultaneously

Fig. 27



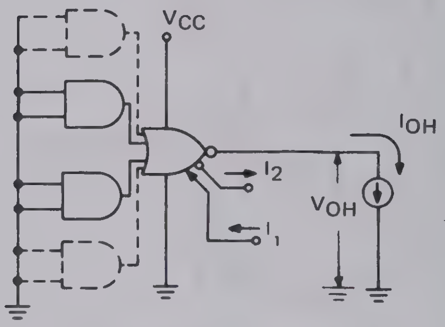
V_{CC}
I_{OL}
I_X
V_1

Fig. 28



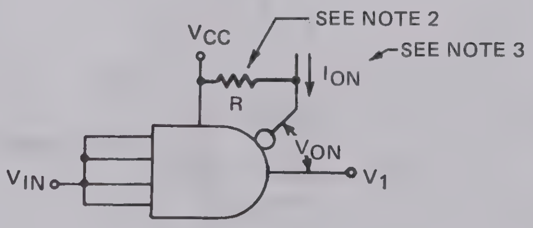
V_{CC}
I_{OL}
I_1
R_1
V_{OL}
$V_{BE(Q)}$

Fig. 29



V_{CC}
I_{OH}
I_2
V_{OH}
I_1

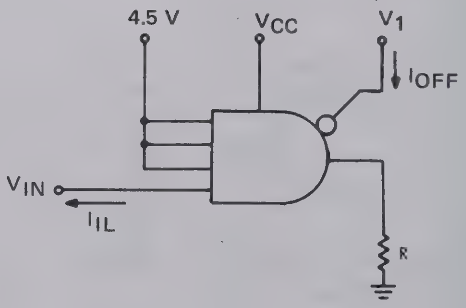
Fig. 30



SEE NOTE 2
V_{CC}
SEE NOTE 3
I_{ON}
R
V_{ON}
V_{IN}
V_1

1. All inputs are tested simultaneously.
2. Deleted on 9H60/5460, 7460
3. Deleted on 9N60/5460, 7460

Fig. 31



4.5 V
V_{CC}
V_1
I_{OFF}
V_{IN}
I_{IL}
R

1. Each input is tested separately.

Fig. 32

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

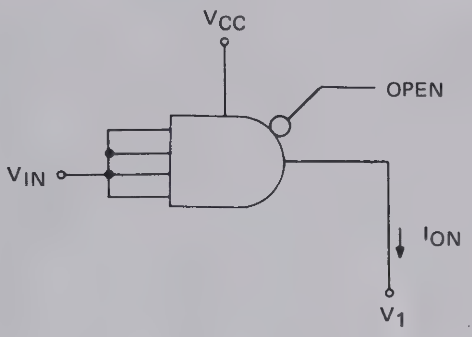
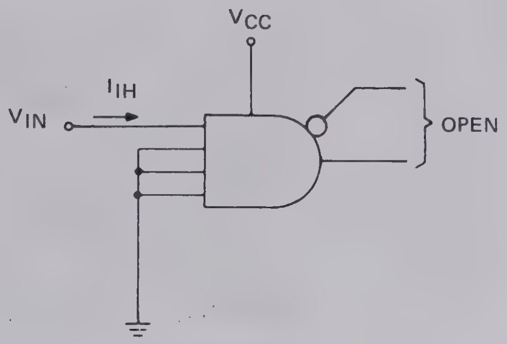
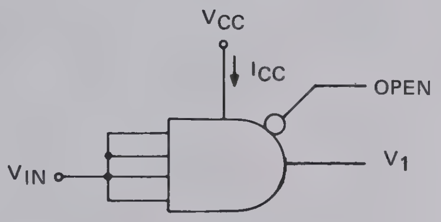

VCC
OPEN
VIN
ION
V1

Fig. 33


VCC
IIH
VIN
OPEN

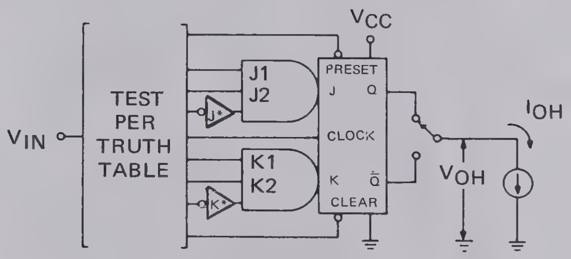
1. Each input is tested separately.

Fig. 34


VCC
ICC
OPEN
VIN
V1

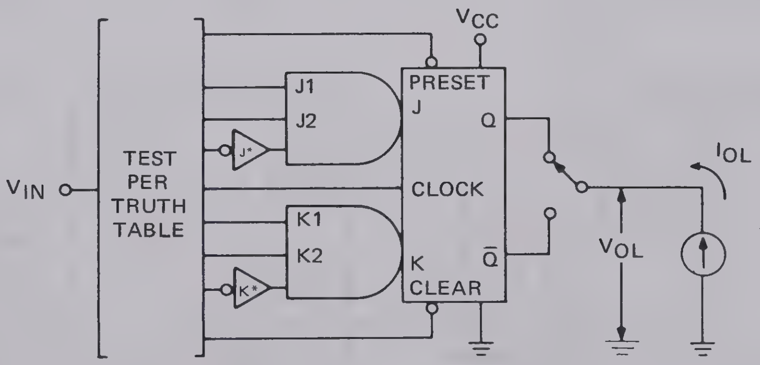
1. "On" and "off" conditions are tested separately.
2. All gates are tested simultaneously

Fig. 35


VCC
VIN
TEST PER TRUTH TABLE
J1
J2
J*
K1
K2
K*
PRESET
J
Q
CLOCK
K
Q̄
CLEAR
IOH
VOH

1. Each output is tested separately.
2. Preset and clear are tested with $V_{IN(clock)} = 0$.

Fig. 36


VCC
VIN
TEST PER TRUTH TABLE
J1
J2
J*
K1
K2
K*
PRESET
J
Q
CLOCK
K
Q̄
CLEAR
IOL
VOL

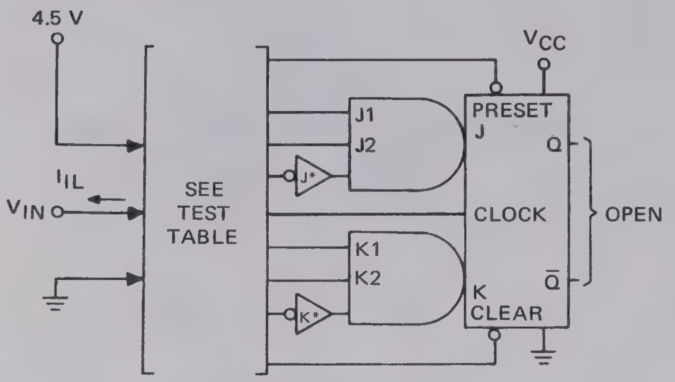
1. Each output is tested separately.

Fig. 37

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

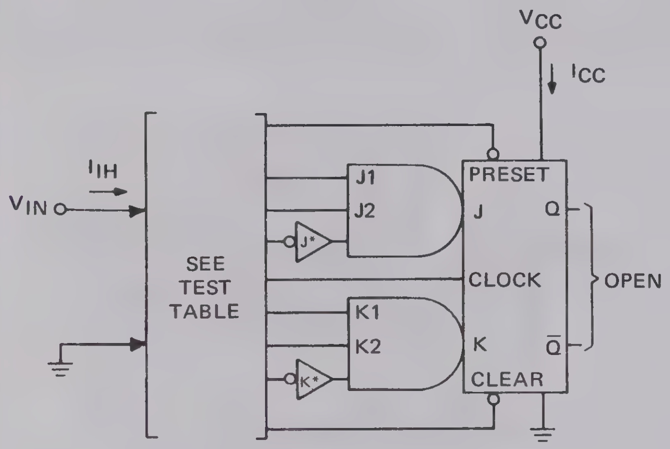

4.5 V
I_{IL}
V_{IN}
SEE TEST TABLE
V_{CC}
J1
J2
J*
PRESET
J
Q
CLOCK
OPEN
K1
K2
K*
K
$\overline{Q}$
CLEAR

TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Ground	Apply Momentary GND, then 4.5 V
J2	J1	J*	Clear
J1	J2	J*	Clear
J*	None	None	None
K2	K1	K*	Preset
K1	K2	K*	Preset
K*	None	None	None
Clock	None	None	None
Preset	K1 and K2	K*	None
Clear	J1 and J2	J*	None

1. Each output is tested separately.

Fig. 38

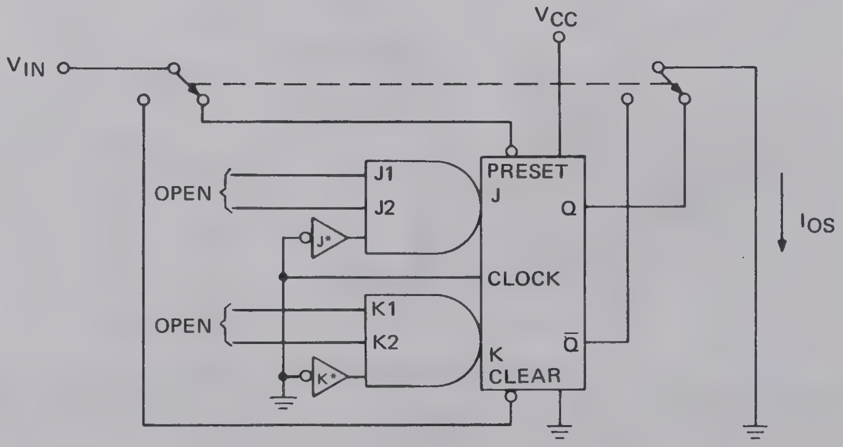

V_{CC}
I_{CC}
I_{IH}
V_{IN}
SEE TEST TABLE
J1
J2
J*
PRESET
J
Q
CLOCK
OPEN
K1
K2
K*
K
$\overline{Q}$
CLEAR

TEST TABLE

Apply V_{IN} (Test I_{IH})	Ground	Apply 4.5 V
J2	J1 and Clear	J*
J1	J2 and Clear	J*
J*	None	None
K2	K1 and Preset	K*
K1	K2 and Preset	K*
K*	None	None
Clock	None	None
Preset	K1 and K2	K*
Clear	J1 and J2	J*

1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

Fig. 39


V_{CC}
V_{IN}
OPEN
J1
J2
J*
PRESET
J
Q
I_{OS}
CLOCK
OPEN
K1
K2
K*
K
$\overline{Q}$
CLEAR

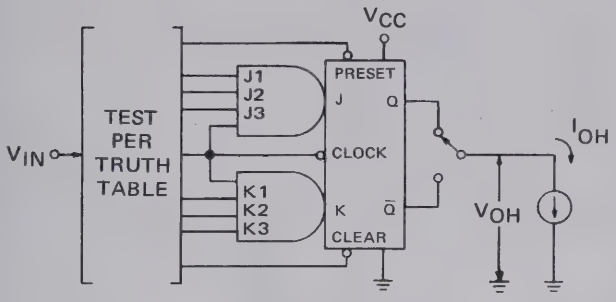
1. Each output is tested separately.

Fig. 40

*Arrows indicate actual direction of current flow.

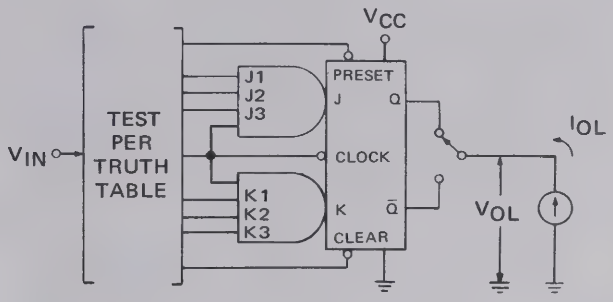
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)


VCC
VIN
TEST PER TRUTH TABLE
J1
J2
J3
K1
K2
K3
PRESET
J
Q
CLOCK
K
Q̄
CLEAR
IOH
VOH

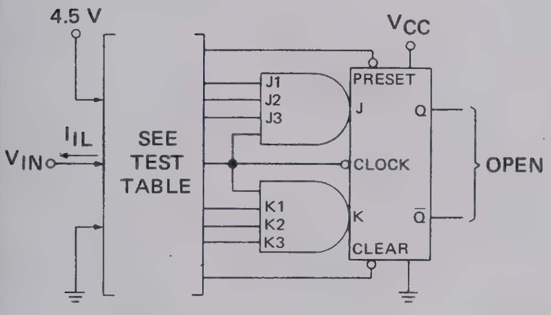
1. Each output is tested separately.

Fig. 41


VCC
VIN
TEST PER TRUTH TABLE
J1
J2
J3
K1
K2
K3
PRESET
J
Q
CLOCK
K
Q̄
CLEAR
IOL
VOL

1. Each output is tested separately.

Fig. 42


4.5 V
VCC
IIL
VIN
SEE TEST TABLE
J1
J2
J3
K1
K2
K3
PRESET
J
Q
CLOCK
K
Q̄
CLEAR
OPEN

1. Each input is tested separately.

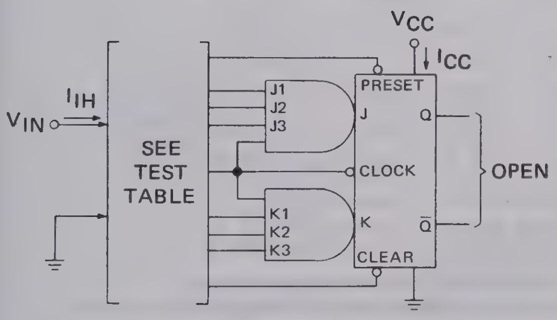
TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

9H102/54H102, 74H102

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Ground
Clock	J1, J2, J3, K1, K2, K3, Clear	Preset
Clock	J1, J2, J3, K1, K2, K3, Preset	Clear
Preset	J1, J2, J3, K1, K2, K3, Clock, Clear	None
Clear	J1, J2, J3, K1, K2, K3, Clock, Preset	None
J1	J2, J3, K1, K2, K3, Clock, Preset	Clear
J2	J1, J3, K1, K2, K3, Clock, Preset	Clear
J3	J1, J3, K1, K2, K3, Clock, Preset	Clear
K1	J1, J2, J3, K2, K3, Clock, Clear	Preset
K2	J1, J2, J3, K1, K3, Clock, Clear	Preset
K3	J1, J2, J3, K1, K2, Clock, Clear	Preset

Fig. 43


VCC
ICC
IIH
VIN
SEE TEST TABLE
J1
J2
J3
K1
K2
K3
PRESET
J
Q
CLOCK
K
Q̄
CLEAR
OPEN

1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

TEST TABLE

Apply V_{IN} (Test I_{IH})	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

9H102/54H102, 74H102

Apply V_{IN} (Test I_{IH})	Ground	4.5V
Clock	J1, J2, J3, K1, K2, K3, Preset	Clear
Clock	J1, J2, J3, K1, K2, K3, Clear	Preset
Preset†	J1, J2, J3, K1, K2, K3, $\overline{Q}$	Clock, Clear
Clear†	J1, J2, J3, K1, K2, K3, $\overline{Q}$	Clock, Preset
J1	J2, J3, Clock, Preset	K1, K2, K3, Clear
J2	J1, J3, Clock, Preset	K1, K2, K3, Clear
J3	J1, J2, Clock, Preset	K1, K2, K3, Clear
K1	K2, K3, Clock, Clear	J1, J2, J3, Preset
K2	K1, K3, Clock, Clear	J1, J2, J3, Preset
K3	K1, K2, Clock, Clear	J1, J2, J3, Preset

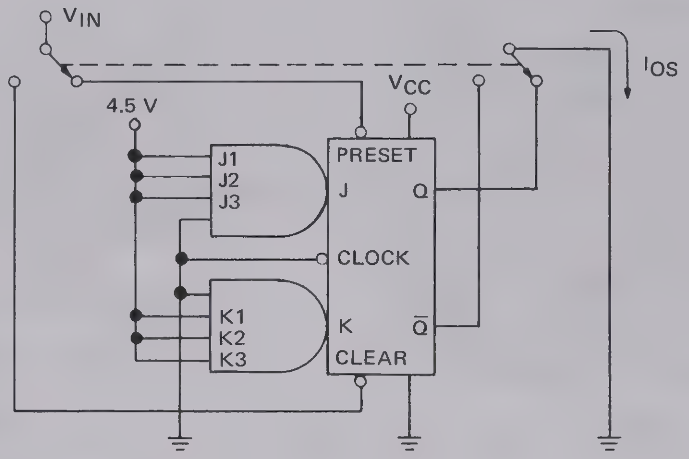
†Duration of this test should not exceed 1 second.

Fig. 44

*Arrows indicate actual direction of current flow.

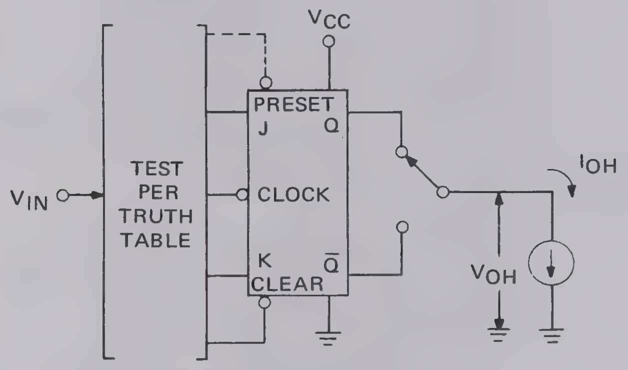
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)


VIN
IOS
VCC
4.5 V
J1
J2
J3
PRESET
J
Q
CLOCK
K1
K2
K3
K
Q̄
CLEAR

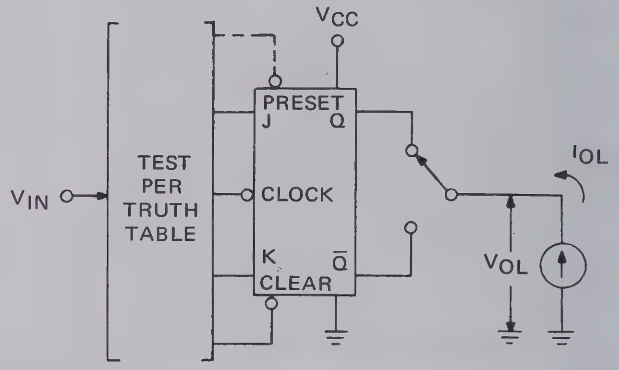
1. Each output is tested separately.

Fig. 45


VCC
PRESET
J
Q
TEST
PER
TRUTH
TABLE
VIN
CLOCK
IOH
K
Q̄
CLEAR
VOH

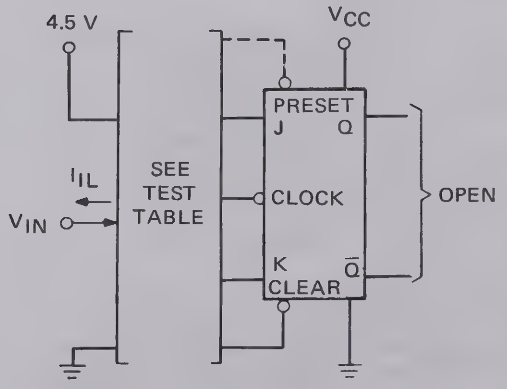
1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for 9H78/54H78, 74H78 only.

Fig. 46


VCC
PRESET
J
Q
TEST
PER
TRUTH
TABLE
VIN
CLOCK
IOL
K
Q̄
CLEAR
VOL

1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for 9H78/54H78, 74H78 only.

Fig. 47


4.5 V
VCC
PRESET
J
Q
IIL
SEE
TEST
TABLE
VIN
CLOCK
OPEN
K
Q̄
CLEAR

TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	Q̄ (See Note 3)	Clock and Clear

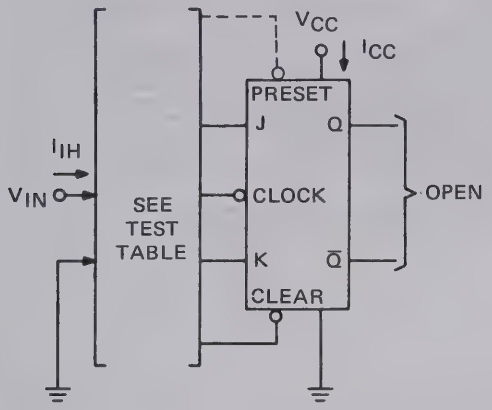
1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground, Q and Q̄ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for 9N76/5476, 7476 circuits only.

Fig. 48

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

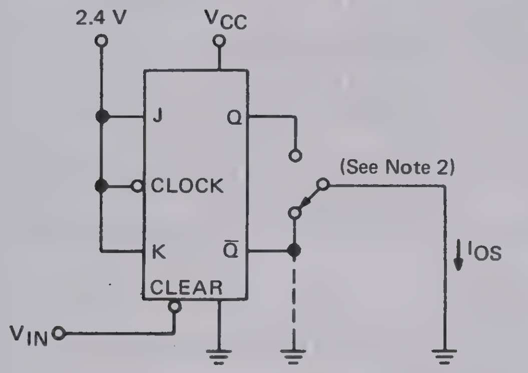

V_{CC}
I_{CC}
PRESET
J
Q
I_{IH}
V_{IN}
SEE
TEST
TABLE
CLOCK
OPEN
K
$\overline{Q}$
CLEAR

TEST TABLE

Apply V_{IN} (Test I_{IH})	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

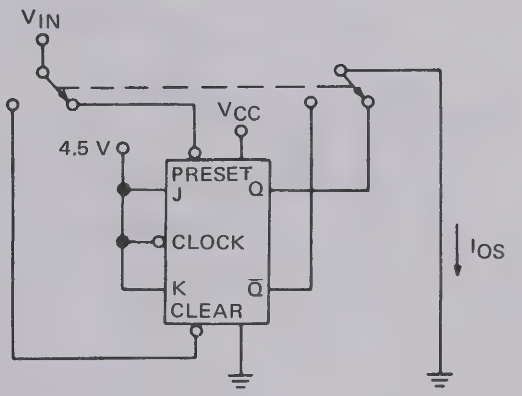
1. Preset is applicable for 9N76/5476, 7476 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = GND. For 9N76/5476, 7476: Preset = 4.5 V.
   b. For 9N73/5473, 7473: J = Clear = 4.5 V, K = GND, and apply momentary 4.5 V, then GND to Clock. For 9N76/5476, 7476: J = K = Clock = Preset = GND, and Clear = 4.5 V.
3. Each flip-flop is tested separately for I_{IH}.

Fig. 49


2.4 V
V_{CC}
J
Q
CLOCK
(See Note 2)
K
$\overline{Q}$
I_{OS}
CLEAR
V_{IN}

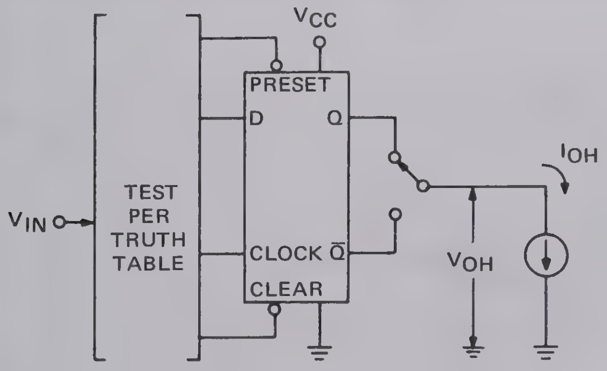
1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\overline{Q}$. When testing Q, apply 2.4 V to Clear, ground $\overline{Q}$, and limit duration of test to 100 ms.

Fig. 50


V_{IN}
V_{CC}
4.5 V
PRESET
J
Q
CLOCK
I_{OS}
K
$\overline{Q}$
CLEAR

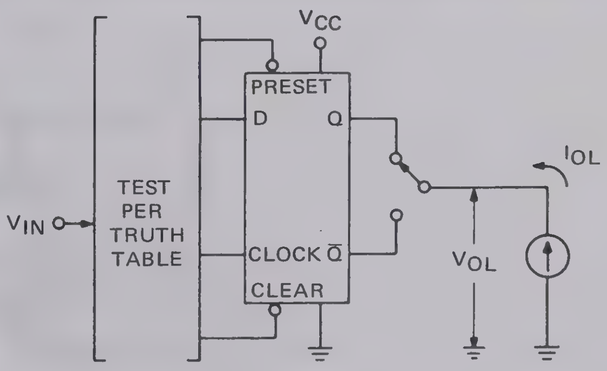
1. Each flip-flop is tested separately.

Fig. 51


V_{CC}
PRESET
D
Q
I_{OH}
V_{IN}
TEST
PER
TRUTH
TABLE
CLOCK $\overline{Q}$
V_{OH}
CLEAR

1. Each flip-flop is tested separately.
2. Each output is tested separately.

Fig. 52


V_{CC}
PRESET
D
Q
I_{OL}
V_{IN}
TEST
PER
TRUTH
TABLE
CLOCK $\overline{Q}$
V_{OL}
CLEAR

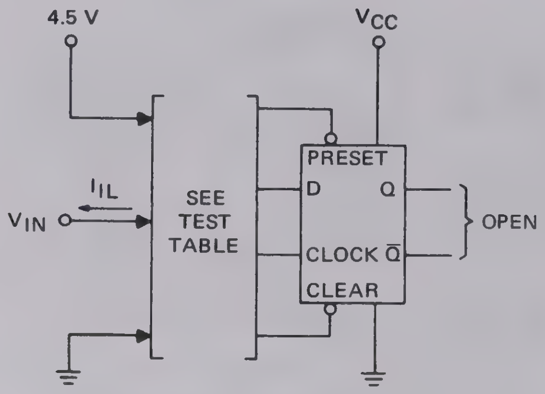
1. Each flip-flop is tested separately.
2. Each output is tested separately.

Fig. 53

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

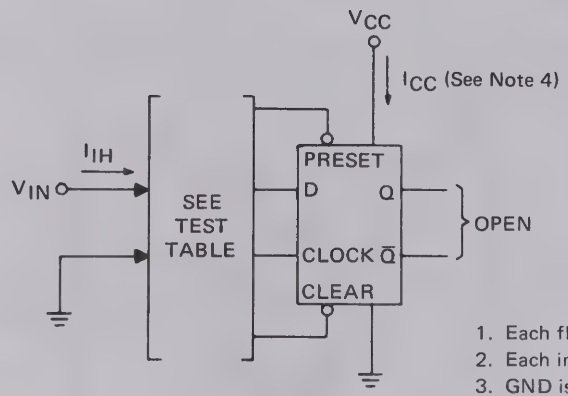

4.5 V
VCC
IIL
VIN
SEE
TEST
TABLE
PRESET
D
Q
CLOCK Q̄
CLEAR
OPEN

TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Apply GND
Clock	Clear	Preset and D
Preset	Clear	Clock and D
Clear	Clock, D, and Preset	None
D	Clear and Clock	Preset

1. Each flip-flop is tested separately.
2. Each input is tested separately.

Fig. 54

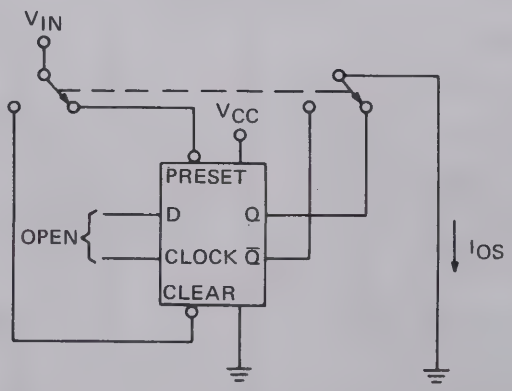

VCC
ICC (See Note 4)
IIH
VIN
SEE
TEST
TABLE
PRESET
D
Q
CLOCK Q̄
CLEAR
OPEN

TEST TABLE

Apply V_{IN} (Test I_{IH})	Apply 4.5 V	Apply GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note 3)
Clear	Preset	Clock, D, and Q
Clear	Preset	D and Clock (See Note 3)
D	Preset and Clock	Clear

1. Each flip-flop is tested seperately.
2. Each input is tested seperately.
3. GND is momentarily applied to clock, then 4.5V.
4. For 9N74/5474, 7474: I_{CC} is measured with D, clock, and preset at GND, then with D, clock, and clear at GND.
5. For 9H74/5474, 74H74: I_{CC} is measured simultaneously for both flip-flops with D. Clock, and Preset at GND, then with D, Clock, and Clear at GND.

Fig. 55


VIN
VCC
PRESET
D
Q
CLOCK Q̄
CLEAR
OPEN
IOS

Each input is tested separately.

Fig. 56

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

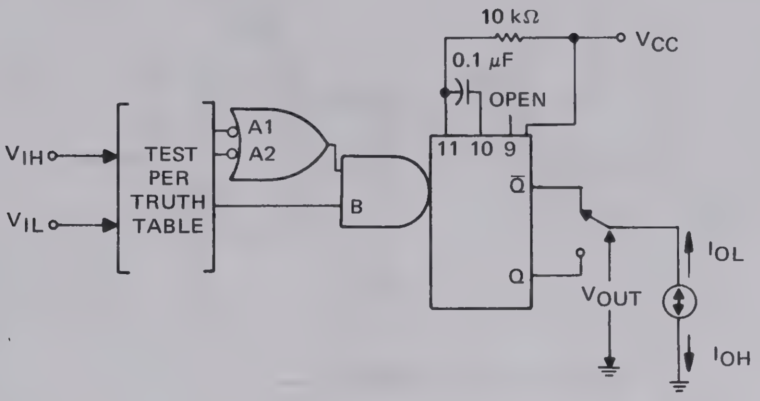
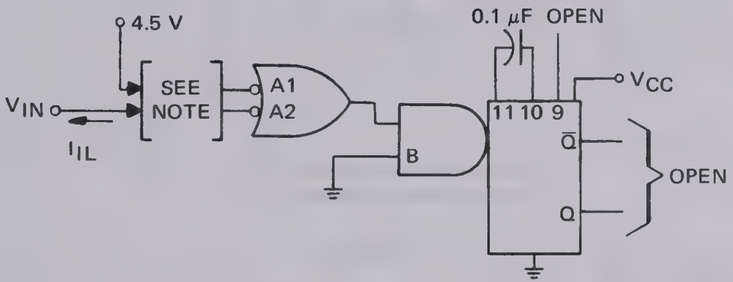

10 kΩ
VCC
0.1 μF
OPEN
VIH
VIL
TEST PER TRUTH TABLE
A1
A2
B
11 10 9
Q̄
Q
VOUT
IOL
IOH

Fig. 57


4.5 V
0.1 μF OPEN
VCC
VIN
IIL
SEE NOTE
A1
A2
B
11 10 9
Q̄
Q
OPEN

1. Each input is tested separately. Input not being tested is at 4.5 V.

Fig. 58

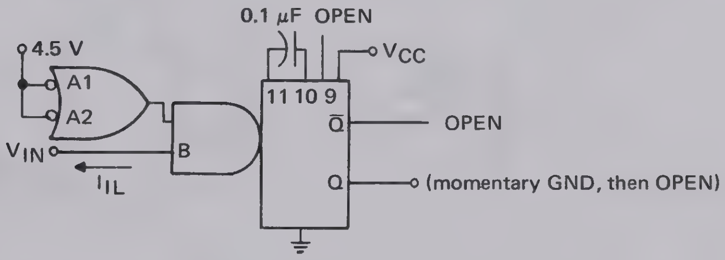
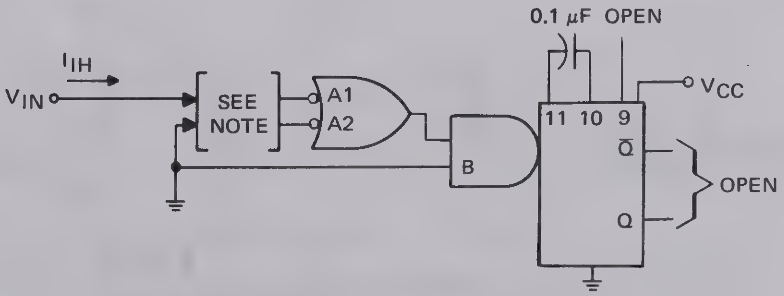

0.1 μF OPEN
4.5 V
VCC
A1
A2
VIN
IIL
B
11 10 9
Q̄
Q
OPEN
(momentary GND, then OPEN)

Fig. 59


0.1 μF OPEN
IIH
VIN
SEE NOTE
A1
A2
B
VCC
11 10 9
Q̄
Q
OPEN

1. Each input is tested separately. Input not being tested is at ground.

Fig. 60

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

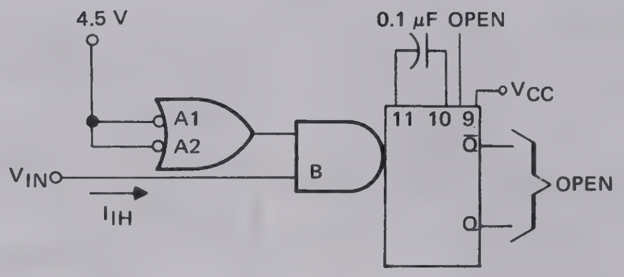
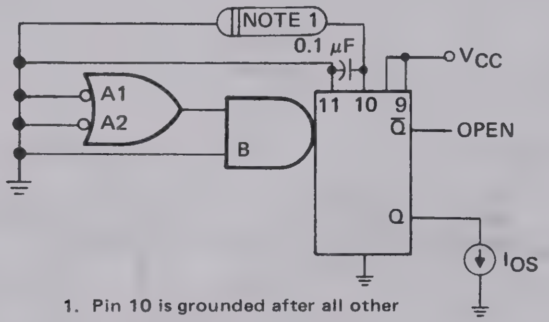

4.5 V
0.1 μF OPEN
VCC
A1
A2
B
11 10 9
Q̄
Q
OPEN
VIN
IIH

Fig. 61


NOTE 1
0.1 μF
VCC
A1
A2
B
11 10 9
Q̄
OPEN
Q
IOS

1. Pin 10 is grounded after all other indicated grounds are made.

Fig. 62

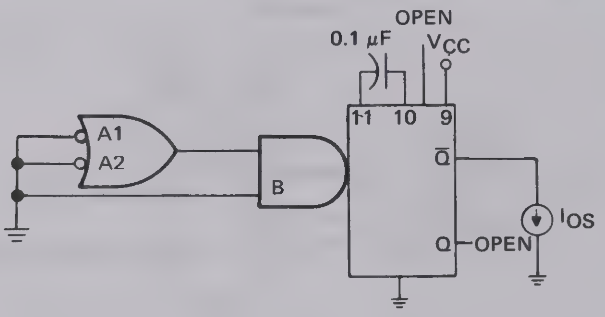
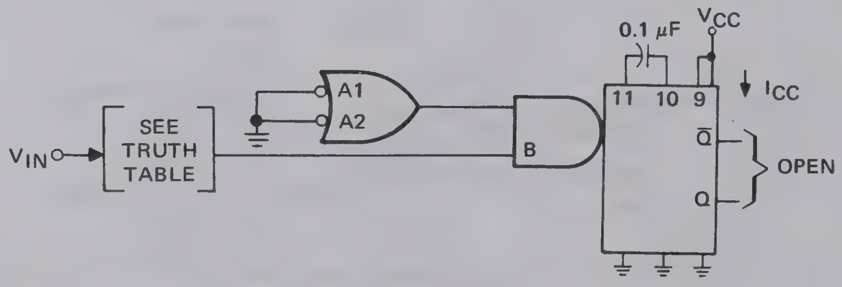

OPEN
0.1 μF
VCC
A1
A2
B
11 10 9
Q̄
Q
OPEN
IOS

Fig. 63


0.1 μF
VCC
ICC
A1
A2
B
11 10 9
Q̄
Q
OPEN
VIN
SEE TRUTH TABLE

1. Quiescent and fired conditions are tested.

Fig. 64

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

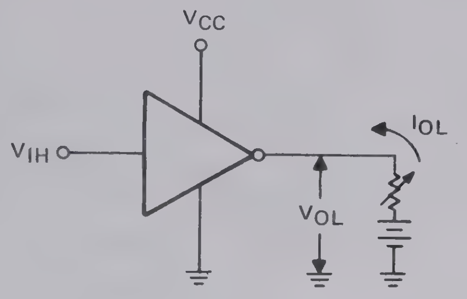

VCC
VIH
IOL
VOL

Fig. 65 V_{IH}, V_{OL}

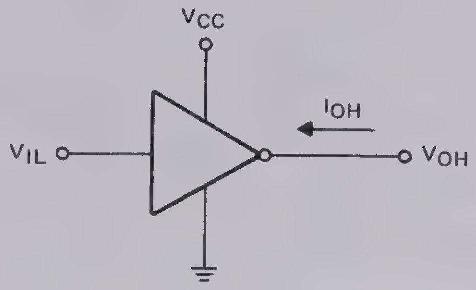

VCC
VIL
IOH
VOH

Fig. 66 V_{IL}, I_{OH}

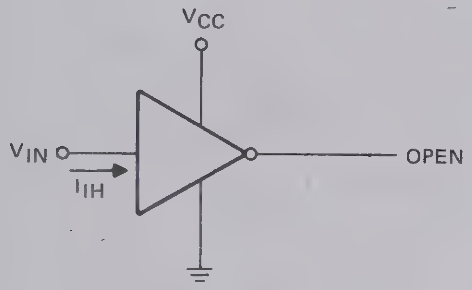

VCC
VIN
IIH
OPEN

Fig. 67 I_{IH}

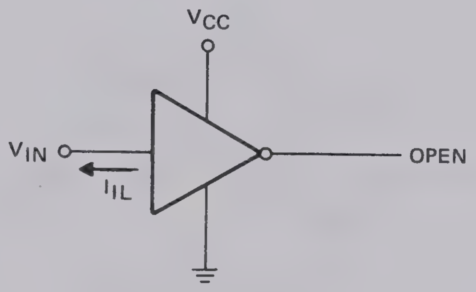
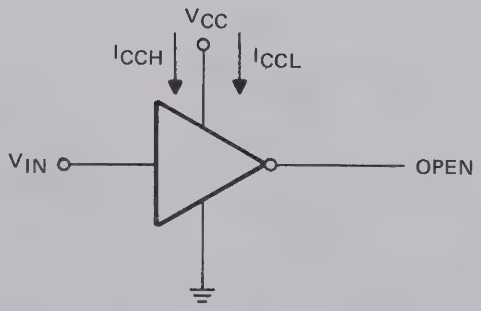

VCC
VIN
IIL
OPEN

Fig. 68 I_{IL}


VCC
ICCH
ICCL
VIN
OPEN

All inverters are tested simultaneously

Fig. 69 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

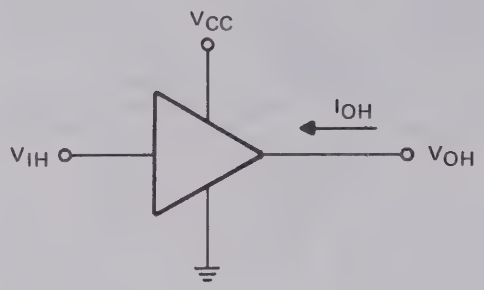

V_{CC}
I_{OH}
V_{IH}
V_{OH}

Fig. 70 V_{IH}, I_{OH}

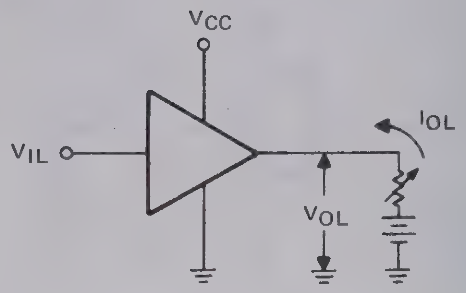

V_{CC}
I_{OL}
V_{IL}
V_{OL}

Fig. 71 V_{IL}, V_{OL}

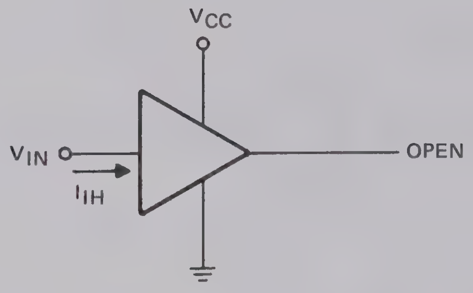

V_{CC}
V_{IN}
I_{IH}
OPEN

Fig. 72 I_{IH}

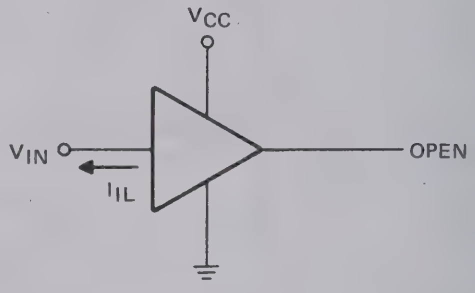
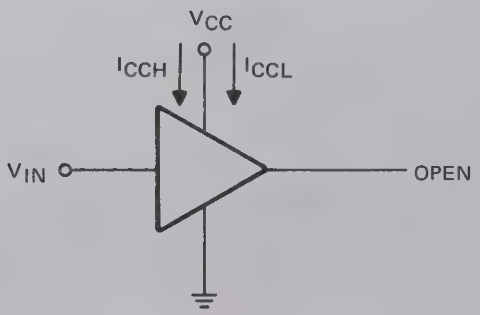

V_{CC}
V_{IN}
I_{IL}
OPEN

Fig. 73 I_{IL}


V_{CC}
I_{CCH}
I_{CCL}
V_{IN}
OPEN

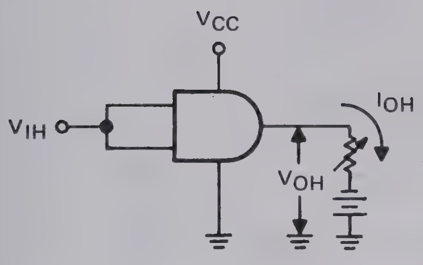
All buffers/drivers are tested simultaneously.

Fig. 74 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)


V_{CC}
V_{IH}
I_{OH}
V_{OH}

Both inputs are tested simultaneously.

Fig. 75 V_{IH}, V_{OH}

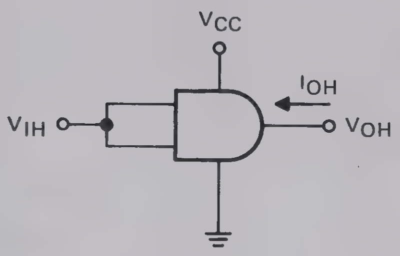
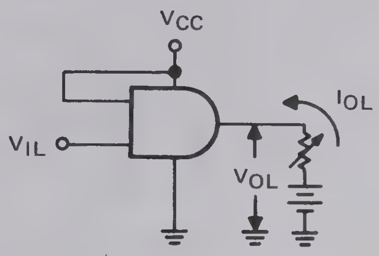
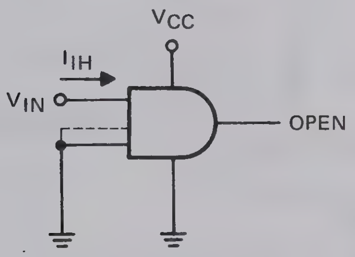

V_{CC}
I_{OH}
V_{IH}
V_{OH}

Fig. 76 V_{IH}, I_{OH}


V_{CC}
I_{OL}
V_{IL}
V_{OL}

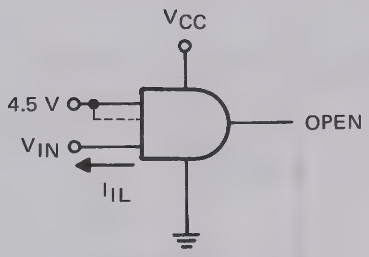
Each input is tested separately.

Fig. 77 V_{IL}, V_{OL}


V_{CC}
I_{IH}
V_{IN}
OPEN

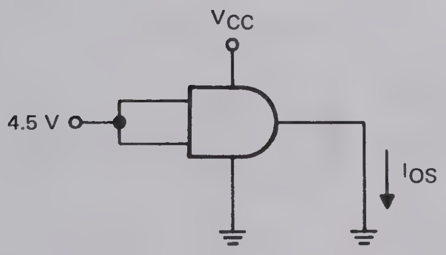
Each input is tested separately.

Fig. 78 I_{IH}


V_{CC}
4.5 V
OPEN
V_{IN}
I_{IL}

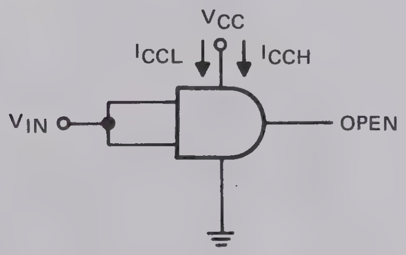
Each input is tested separately.

Fig. 79 I_{IL}



Each gate is tested separately.

Fig. 80 I_{OS}


V_{CC}
I_{CCL}
I_{CCH}
V_{IN}
OPEN

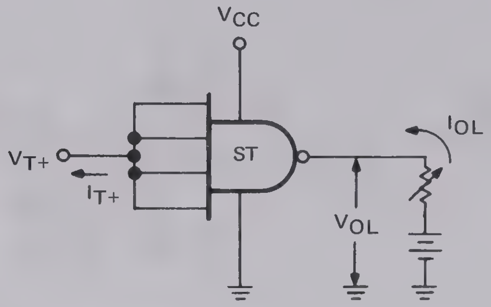
1. HIGH level and LOW level conditions are tested.
2. All gates are tested simultaneously.

Fig. 81 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

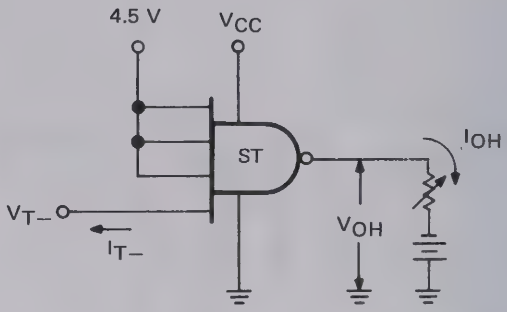
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



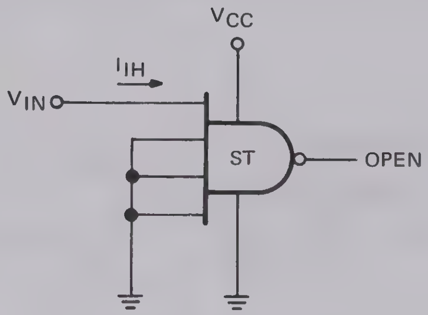
VCC
ST
VT+
IT+
IOL
VOL

Fig. 82 V_{T+}, I_{T+}, V_{OL}



4.5 V
VCC
ST
VT−
IT−
IOH
VOH

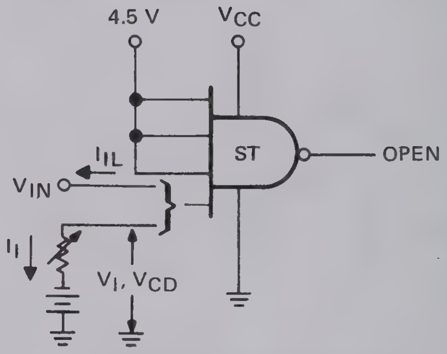
Fig. 83 V_{T-}, I_{T-}, V_{OH}



VCC
IIH
VIN
ST
OPEN

Each input is tested separately.

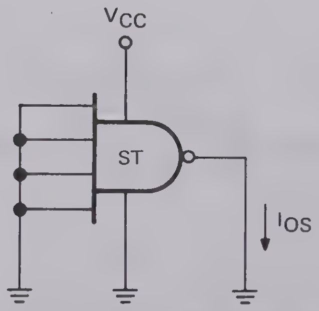
Fig. 84 I_{IH}



4.5 V
VCC
IIL
VIN
ST
OPEN
II
VI, VCD

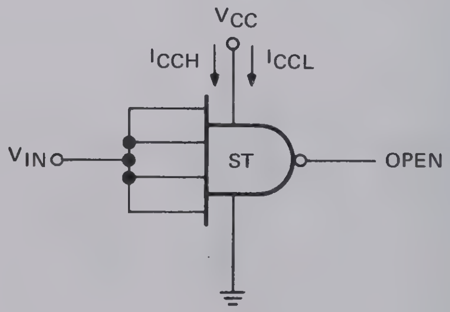
Each input is tested separately.

Fig. 85 V_I, V_{CD}, I_{IL}



Each gate is tested separately.

Fig. 86 I_{OS}



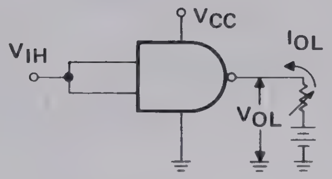
VCC
ICCH
ICCL
VIN
ST
OPEN

Fig. 87 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

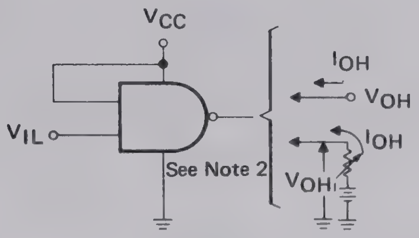
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)


V_{CC}
V_{IH}
I_{OL}
V_{OL}

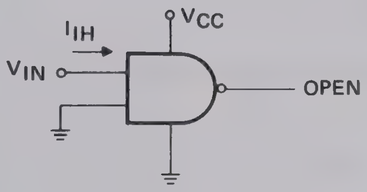
Both inputs are tested simultaneously

Fig. 88 V_{IH}, V_{OL}


V_{CC}
V_{IL}
See Note 2
I_{OH}
V_{OH}
I_{OH}
V_{OH}

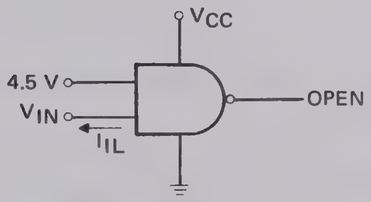
1. Each input is tested separately.
2. I_{OH} is tested at V_{OH} = 12 V and V_{OH} is tested at I_{OH} = 1 mA.

Fig. 89 V_{IL}, V_{OH}, I_{OH}


V_{CC}
I_{IH}
V_{IN}
OPEN

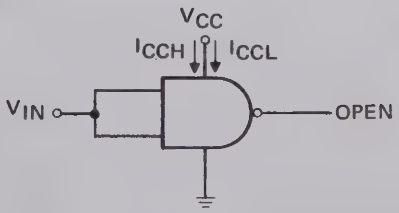
Each input is tested separately.

Fig. 90 I_{IH}


V_{CC}
4.5 V
V_{IN}
I_{IL}
OPEN

Each input is tested separately.

Fig. 91 I_{IL}


V_{CC}
I_{CCH}
I_{CCL}
V_{IN}
OPEN

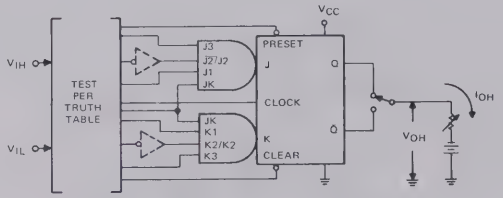
High-level and low-level output conditions are tested.

Fig. 92 I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

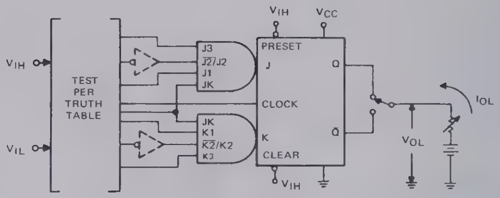
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)


V_{CC}
V_{IH}
V_{IL}
TEST PER TRUTH TABLE
J3
$\overline{J2}$/J2
J1
JK
JK
K1
K2/K2
K3
PRESET
J
Q
CLOCK
K
$\overline{Q}$
CLEAR
I_{OH}
V_{OH}

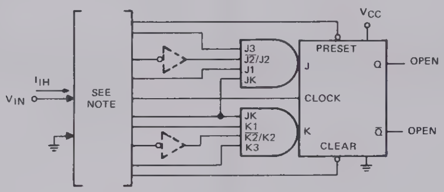
NOTES:
1. Each output is tested separately.
2. V_{OH} is also tested using clear and preset inputs.

Fig. 93 V_{IH}, V_{IL}, V_{OH}


V_{IH}
V_{CC}
V_{IH}
V_{IL}
TEST PER TRUTH TABLE
J3
$\overline{J2}$/J2
J1
JK
JK
K1
$\overline{K2}$/K2
K3
PRESET
J
Q
CLOCK
K
$\overline{Q}$
CLEAR
V_{IH}
I_{OL}
V_{OL}

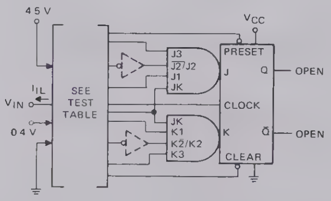
NOTE: Each output is tested separately.

Fig. 94 V_{IH}, V_{IL}, V_{OL}


V_{CC}
I_{IH}
V_{IN}
SEE NOTE
J3
$\overline{J2}$/J2
J1
JK
JK
K1
$\overline{K2}$/K2
K3
PRESET
J
Q
OPEN
CLOCK
K
$\overline{Q}$
OPEN
CLEAR

NOTE: V_{IN} is applied and I_{IH} is measured separately for each input. All other inputs are grounded.

Fig. 95 I_{IH}


4.5 V
V_{CC}
I_{IL}
V_{IN}
0.4 V
SEE TEST TABLE
J3
$\overline{J2}$/J2
J1
JK
JK
K1
K2/K2
K3
PRESET
J
Q
OPEN
CLOCK
K
$\overline{Q}$
OPEN
CLEAR

NOTES:
1. Each input is tested separately.
2. V_{IN} is applied and I_{IL} is measured separately for each input.
3. All unspecified inputs are at 4.5 V.

Fig. 96 I_{IL}

TEST TABLE

Apply V_{IN} (Test I_{IL})	CONDITIONS ON OTHER INPUTS	
	Apply 0.4 V	Apply GND
Clock	None	None
Preset	Clear	Clock
Clear	Preset	Clock
J1	$\overline{J2}$ (OR 4.5 V TO J2)	Clock, Clear
$\overline{J2}$ (OR J2)	None	Clock, Clear
J3	$\overline{J2}$ (OR 4.5 V TO J2)	Clock, Clear
JK	$\overline{J2}$, K2 (OR 4.5 V TO J2, K2)	Clock, Clear
JK	$\overline{J2}$, $\overline{K2}$ (OR 4.5 V TO J2, K2)	Clock, Preset
K1	$\overline{K2}$ (OR 4.5 V TO K2)	Clock, Preset
$\overline{K2}$ (OR K2)	None	Clock, Preset
K3	$\overline{K2}$ (OR 4.5 V TO K2)	Clock, Preset

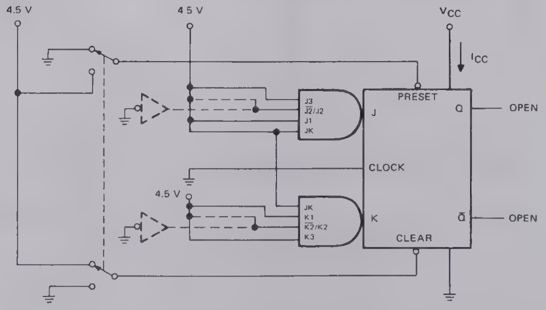
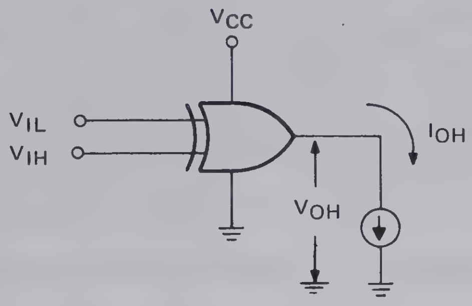

4.5 V
4.5 V
V_{CC}
I_{CC}
J3
$\overline{J2}$/J2
J1
JK
PRESET
J
Q
OPEN
CLOCK
4.5 V
JK
K1
$\overline{K2}$/K2
K3
K
$\overline{Q}$
OPEN
CLEAR

Fig. 97 I_{CC}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

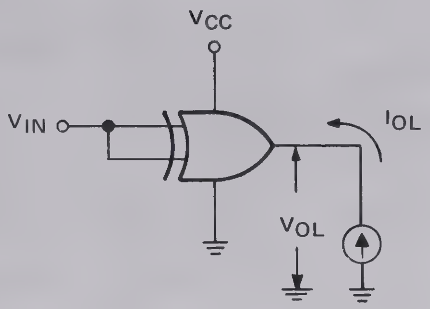
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)


VCC
VIL
VIH
IOH
VOH

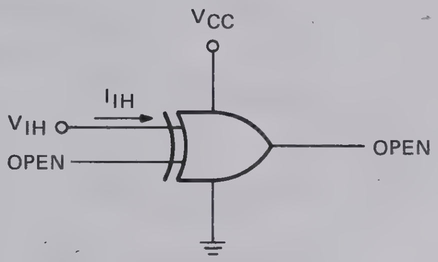
1. Each input is tested separately.

Fig. 98


VCC
VIN
IOL
VOL

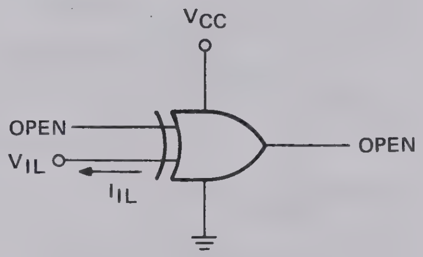
1. Low level and high level input conditions are tested.

Fig. 99


VCC
IIH
VIH
OPEN
OPEN

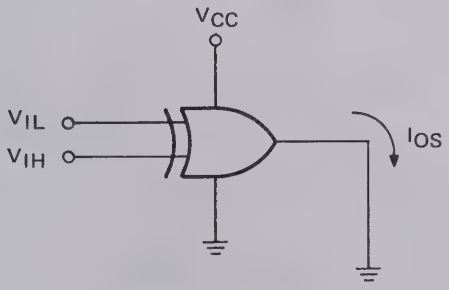
1. Each input is tested separately.

Fig. 100


VCC
OPEN
VIL
IIL
OPEN

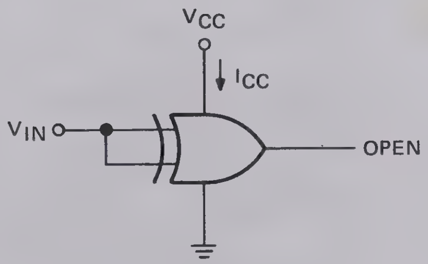
1. Each input is tested separately.

Fig. 101


VCC
VIL
VIH
IOS

1. Each gate is tested separately.

Fig. 102


VCC
ICC
VIN
OPEN

1. Low level and high level input conditions are tested.

Fig. 103

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

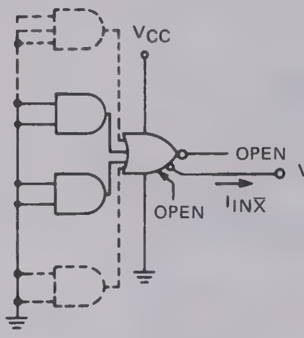
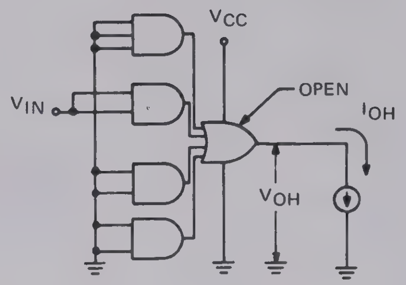
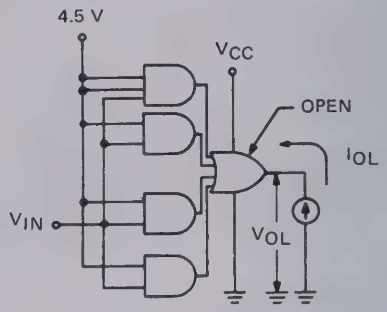

V_{CC}
OPEN
$V_{\overline{X}}$
OPEN
$I_{IN\overline{X}}$

Fig. 104.


V_{CC}
OPEN
I_{OH}
V_{IN}
V_{OH}

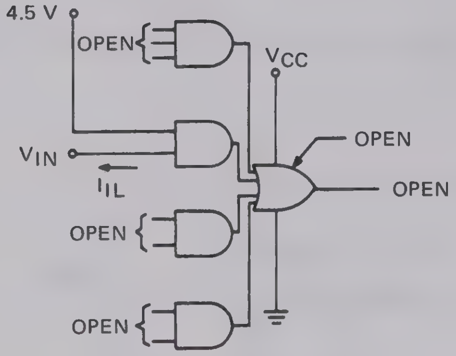
1. Each AND section is tested separately.

Fig. 105.


4.5 V
V_{CC}
OPEN
I_{OL}
V_{IN}
V_{OL}

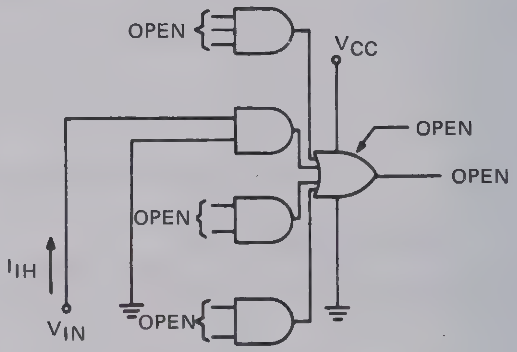
1. Each set of inputs is tested separately.

Fig. 106.


4.5 V
OPEN
V_{CC}
OPEN
V_{IN}
OPEN
I_{IL}
OPEN
OPEN

1. Each input of each AND section is tested separately.

Fig. 107.


OPEN
V_{CC}
OPEN
OPEN
OPEN
I_{IH}
V_{IN}
OPEN

1. Each input of each AND section is tested separately.

Fig. 108.

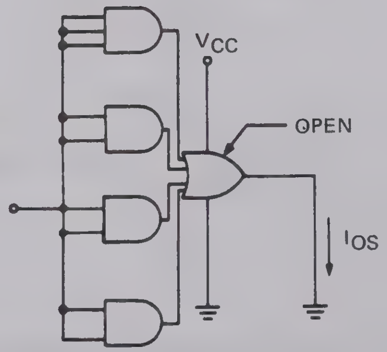
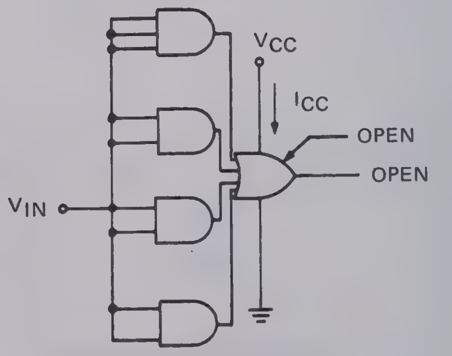

V_{CC}
OPEN
I_{OS}

Fig. 109.


V_{CC}
I_{CC}
OPEN
OPEN
V_{IN}

1. Logical 0 and logical 1 conditions are tested.

Fig. 110.

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)

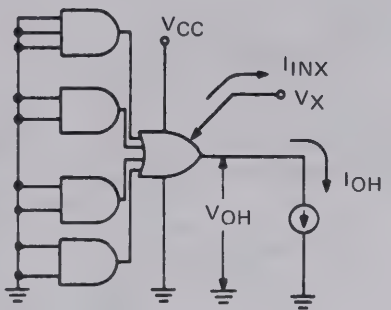

VCC
IINX
VX
IOH
VOH

Fig. 111.

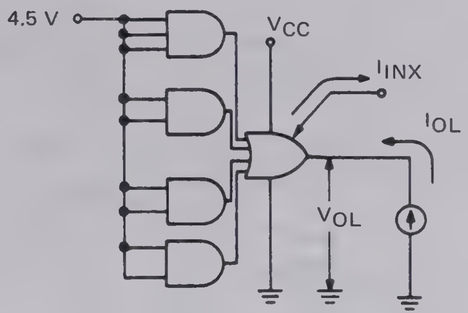
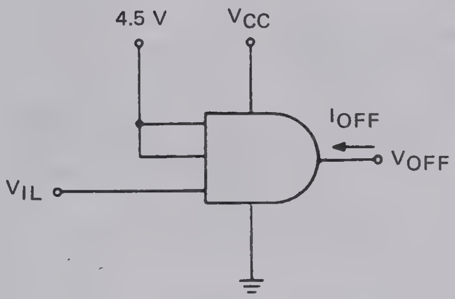
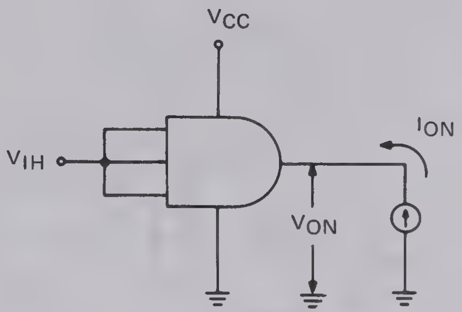

4.5 V
VCC
IINX
IOL
VOL

Fig. 112.


4.5 V
VCC
IOFF
VOFF
VIL

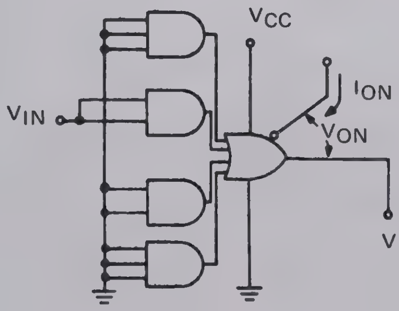
1. Each input is tested separately.

Fig. 113.


VCC
ION
VIH
VON

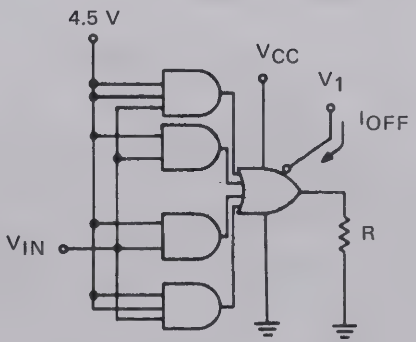
1. All inputs are tested simultaneously.

Fig. 114.


VCC
ION
VIN
VON
V1

1. Each AND section is tested separately.

Fig. 115.


4.5 V
VCC
V1
IOFF
R
VIN

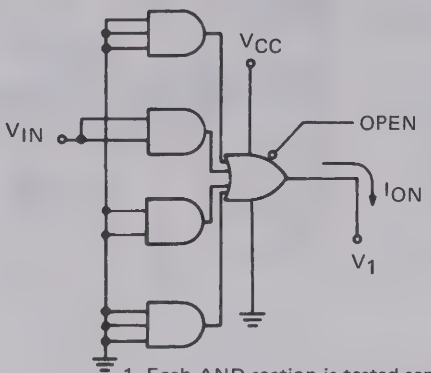
1. Each set of inputs is tested separately.

Fig. 116.

*Arrows indicate actual direction of current flow.

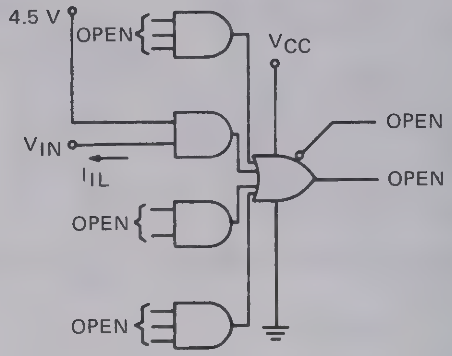
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)


VCC
VIN
OPEN
ION
V1

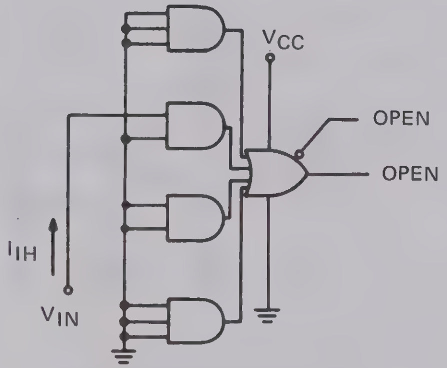
1. Each AND section is tested separately.

Fig. 117.


4.5 V
OPEN
VCC
OPEN
VIN
OPEN
IIL
OPEN
OPEN

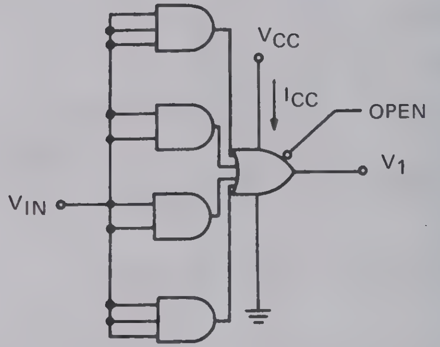
1. Each input is tested separately.

Fig. 118.


VCC
OPEN
OPEN
IIH
VIN

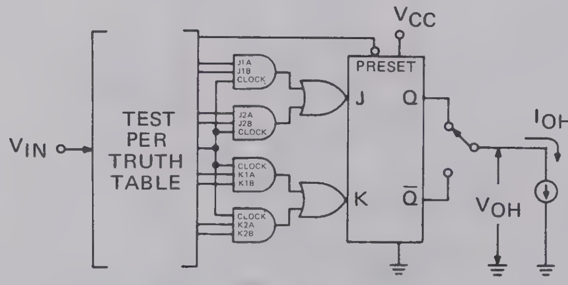
1. Each input is tested separately.

Fig. 119.


VCC
ICC
OPEN
V1
VIN

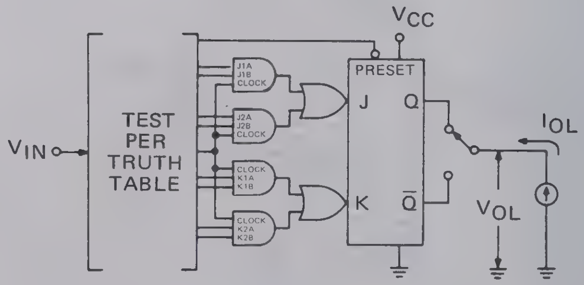
1. On and off conditions are tested separately.

Fig. 120.


VCC
PRESET
J1A
J1B
CLOCK
J2A
J2B
CLOCK
CLOCK
K1A
K1B
CLOCK
K2A
K2B
J
Q
K
Q̄
VIN
TEST PER TRUTH TABLE
IOH
VOH

1. Each output is tested separately.

Fig. 121.


VCC
PRESET
J1A
J1B
CLOCK
J2A
J2B
CLOCK
CLOCK
K1A
K1B
CLOCK
K2A
K2B
J
Q
K
Q̄
VIN
TEST PER TRUTH TABLE
IOL
VOL

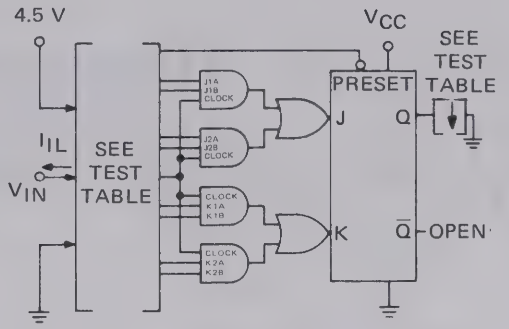
1. Each output is tested separately.

Fig. 122.

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



1. Each input is tested separately.

TEST TABLES[(a)]

9H71/54H71, 74H71

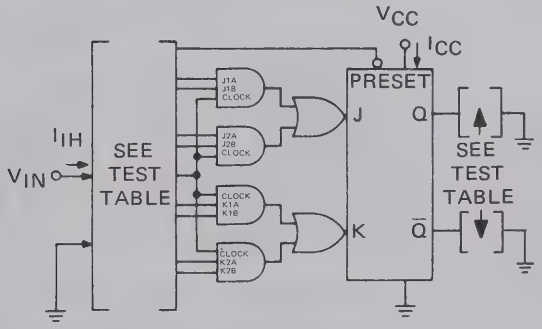
Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Apply Momentary GND then 4.5 V	GND
Clock	J1A,J1B,J2A,J2B,K1A,K1B,K2A, and K2B	Preset	None
Clock[(b)]	J1A,J1B,J2A,J2B,K1A,K1B,K2A,K2B, and Preset	None	Q
Preset	J1A,J1B,J2A,J2B,K1A,K1B,K2A,K2B, and Clock	None	None
J1A[(b)]	J1B and Clock	None	Q
J1B[(b)]	J1A and Clock	None	Q
J2A[(b)]	J2B and Clock	None	Q
J2B[(b)]	J2A and Clock	None	Q
K1A	K1B and Clock	Preset	None
K1B	K1A and Clock	Preset	None
K2A	K2B and Clock	Preset	None
K2B	K2A and Clock	Preset	None

9H101/54H101, 74H101

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	Ground
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B	Preset
Preset	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Clock	None
J1A[(b)]	J1B, J2A, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J1B[(b)]	J1A, J2A, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J2A[(b)]	J1A, J1B, J2B, K1A, K1B, K2A, K2B, Clock, Preset	Q
J2B[(b)]	J1A, J1B, J2A, K1A, K1B, K2A, K2B, Clock, Preset	Q
K1A	J1A, J1B, J2A, J2B, K1B, K2A, K2B, Clock	Preset
K1B	J1A, J1B, J2A, J2B, K1A, K2A, K2B, Clock	Preset
K2A	J1A, J1B, J2A, J2B, K1A, K1B, K2B, Clock	Preset
K2B	J1A, J1B, J2A, J2B, K1A, K1B, K2A, Clock	Preset

(a) Inputs and outputs not specified are open.
(b) Duration of this test should not exceed 1 second.

Fig. 123.



1. Each input is tested separately.
2. I_{CC} is measured for each of the following conditions:
   A) J1A = J1B = J2A = J2B = K1A = K1B = K2A = K2B = Preset = 4.5 V, and Clock = momentary 4.5 V, then Gnd.

TEST TABLES[(a)]

9H71/54H71, 74H71

Apply V_{IN} (Test I_{IH})	Ground
Clock	J1A,J1B,J2A,J2B,K1A,K1B,K2A,K2B, and Preset
Clock[(b)]	J1A,J1B,J2A,J2B,K1A,K1B,K2A,K2B, Preset and Q
Preset	K1A,K1B,K2A,K2B,Clock, and Q
J1A	J1B, Clock, and Preset
J1B	J1A, Clock, and Preset
J2A	J2B, Clock, and Preset
J2B	J2A, Clock, and Preset
K1A[(b)]	K1B, Clock, Preset, and Q
K1B[(b)]	K1A, Clock, Preset, and Q
K2A[(b)]	K2B, Clock, Preset, and Q
K2B[(b)]	K2A, Clock, Preset, and Q

9H101/54H101, 74H101

Apply V_{IN} (Test I_{IH})	Ground	Apply 4.5 V
Clock	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Preset	None
Preset[(b)]	J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, Q̄	Clock
J1A	J1B, J2A, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J1B	J1A, J2A, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J2A	J1A, J1B, J2B, Preset, Clock	K1A, K1B, K2A, K2B
J2B	J1A, J1B, J2A, Preset, Clock	K1A, K1B, K2A, K2B
K1A	K1B, K2A, K2B, Clock	Preset J1A, J1B, J2A, J2B
K1B	K1A, K2A, K2B, Clock	Preset J1A, J1B, J2A, J2B
K2A	K1A, K1B, K2B, Clock	Preset J1A, J1B, J2A, J2B
K2B	K1A, K1B, K2B, Clock	Preset J1A, J1B, J2A, J2B

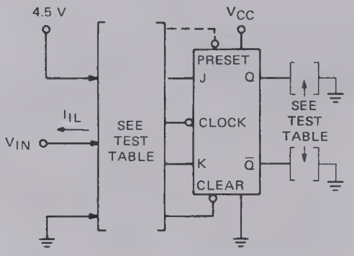
(a) Inputs and outputs not specified are open.
(b) Duration of this test should not exceed 1 second.

Fig. 124.

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground (<1 second), Q and $\overline{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is not applicable for 9H73/54H73, 74H73.
6. Apply the same conditions simultaneously to both flip-flops when testing the 9H108/54H108, 74H108.

TEST TABLES

9H73/54H73, 74H73
9H76/54H76, 74H76
9H78/54H78, 74H78

Apply V_{IN} (Test I_{IL})	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\overline{Q}$ (See Note 3)	Clock and Clear

9H103/54H103, 74H103

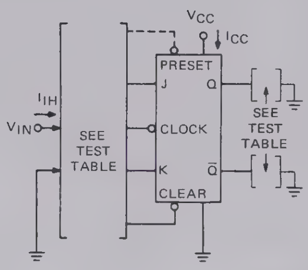
Apply V_{IN} (Test I_{IL})	Apply GND	Apply 4.5 V
Clock	Clear	J, K
Clear	None	Clock, J, K
J	Clear	Clock, K
K†	Q	Clock, Clear, J

†Duration of this test should not exceed 1 second.

9H106/54H106, 74H106
9H108/54H108, 74H108

Apply V_{IN} (Test I_{IL})	Apply GND	Apply 4.5 V
Clock	Clear	J, K, Preset,(Note 6)
Clock	Preset	J, K, Clear,(Note 6)
Clear	None	Clock, Preset, J, K,(Note 6)
Preset	None	Clock, Clear, J, K
J	Clear	Clock, K Preset
K	Preset	Clock, Clear, J

Fig. 125.



1. Preset is not applicable to 9H73/54H73, 74H73; 9H103/54H103, 74H103.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = Gnd.
      Preset (when applicable) = 4.5 V.
   b. For 9H73/54H73, 74H73 and 9H103/54H103, 74H103. J = Clear = 4.5 V, K = Gnd, and apply momentary 4.5 V, then Gnd, to Clock. For 9H76/54H76, 74H76; 9H78/54H78, 74H78; 9H108/54H108, 74H108: J = K = Clock = Preset = Gnd, and Clear = 4.5 V.
3. Each flip-flop is tested separately except where Note 4 is referenced.
4. Apply the same conditions to both flip-flops when testing the 9H108/54H108, 74H108.

TEST TABLES

9H73/54H73, 74H73
9H76/54H76, 74H76
9H78/54H78, 74H78

Apply V_{IN} (Test I_{IH})	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

9H103/54H103, 74H103

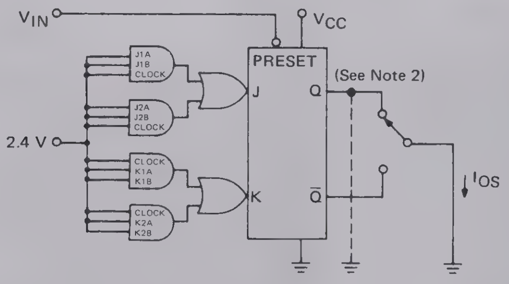
Apply V_{IN} (Test I_{IH})	Apply GND	Apply 4.5 V
Clock	Clear, J, K	None
Clear†	Q, J, K	Clock
J	Clock	Clear, K
K	Clock, Clear	J

9H106/54H106, 74H106
9H108/54H108, 74H108

Apply V_{IN} (Test I_{IH})	Apply GND	Apply 4.5 V
Clock	Clear, J, K	Preset,(Note 4)
Clock	Preset, J, K	Clear,(Note 4)
Clear†	Q, J, K	Preset, Clock(Note 4)
Preset†	$\overline{Q}$, J, K	Clear, Clock
J	Clock, Preset	Clear, K
K	Clock, Clear	Preset, J

†Duration of this test should not exceed 1 second.

Fig. 126.

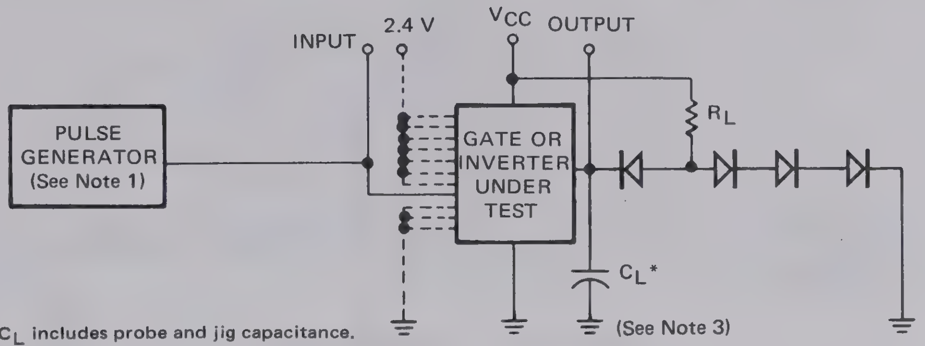


1. Each output is tested separately.
2. Test circuit shows setup for testing Q. When testing $\overline{Q}$, apply 2.4 V to Preset, ground Q, and limit duration of test to 100 ms.

Fig. 127.

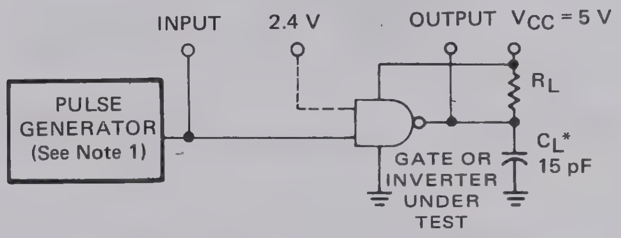
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS

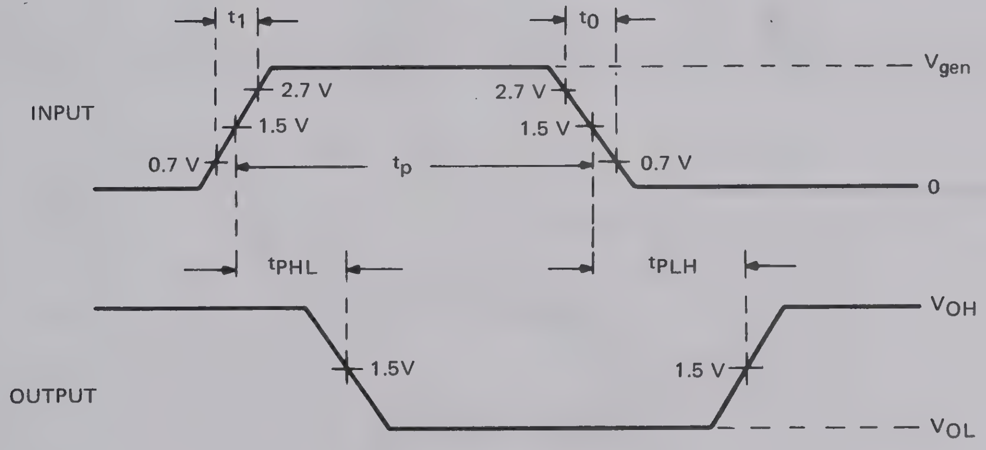

INPUT
2.4 V
V_{CC}
OUTPUT
PULSE GENERATOR (See Note 1)
GATE OR INVERTER UNDER TEST
R_L
C_L*
(See Note 3)

*C_L includes probe and jig capacitance.

TEST CIRCUIT FOR 9N00/5400, 7400; 9N02/5402, 7402; 9N04/5404, 7404; 9N10/5410, 7410; 9N20/5420, 7420; 9N30/5430, 7430; 9N40/5440, 7440; 9N50/5450, 7450; 9N51/5451, 7451; 9N53/5453, 7453 and 9N54/5454, 7454


INPUT
2.4 V
OUTPUT
$V_{CC} = 5$ V
PULSE GENERATOR (See Note 1)
R_L
C_L*
15 pF
GATE OR INVERTER UNDER TEST

TEST CIRCUIT FOR 9N01/5401, 7401; 9N03/5403, 7403; 9N05/5405, 7405; 9N39/5439, 7439


t_1
t_0
V_{gen}
INPUT
2.7 V
1.5 V
0.7 V
2.7 V
1.5 V
0.7 V
t_p
0
t_{PHL}
t_{PLH}
V_{OH}
OUTPUT
1.5V
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

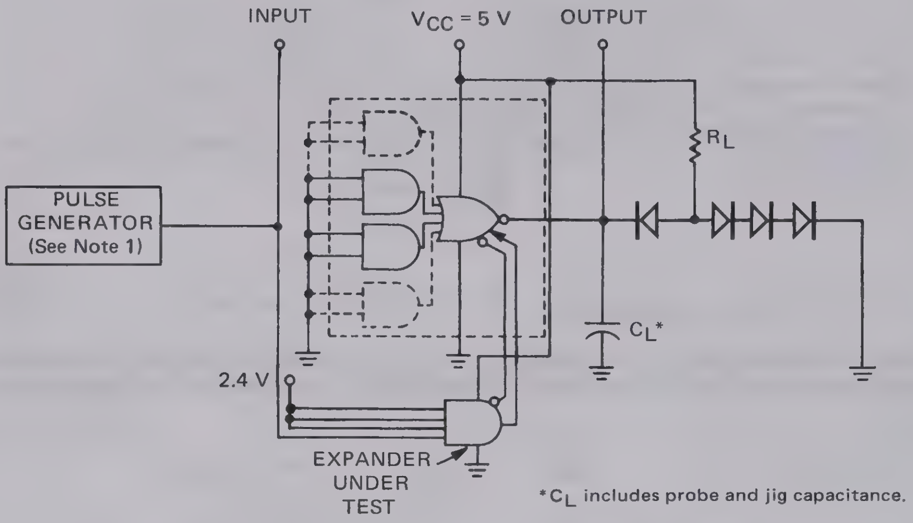
NOTES:

1. The generator has the following characteristics: $V_{gen} = 3.5$ V, $t_0 = 5$ ns, $t_1 = 10$ ns, $t_p = 0.5$ µs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation Delay = $\frac{t_{PHL} + t_{PLH}}{2}$
3. When testing 9N00/5400, 7400 through 9N40/5440, 7440 (except 9N02/5402, 7402), connect all unused inputs to 2.4 V. When testing the 9N02/5402, 7402 or 9N50/5450, 7450 through 9N54/5454, 7454, apply the input pulse to one input of one AND section and 2.4 V to all unused inputs of that AND section. All inputs or unused AND sections are grounded.

Fig. A GATE PROPAGATION DELAY TIMES

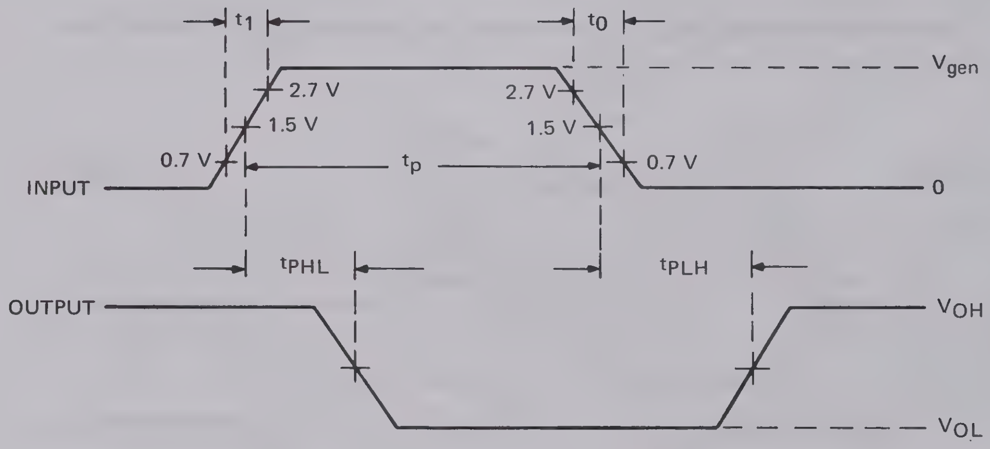
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


INPUT
V_{CC} = 5 V
OUTPUT
R_L
PULSE GENERATOR (See Note 1)
C_L*
2.4 V
EXPANDER UNDER TEST

*C_L includes probe and jig capacitance.

TEST CIRCUIT


t_1
t_0
V_{gen}
2.7 V
2.7 V
1.5 V
1.5 V
0.7 V
0.7 V
t_p
INPUT
0
t_{PHL}
t_{PLH}
OUTPUT
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS

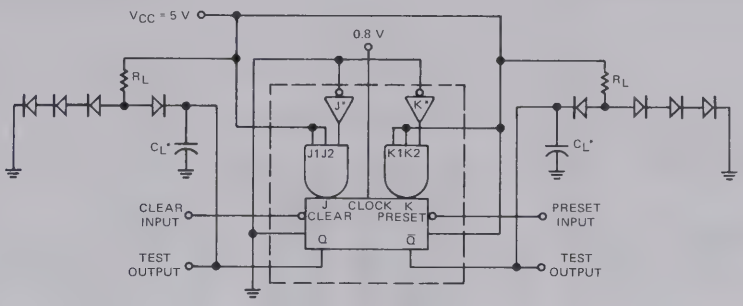
NOTES:

1. The generator has the following characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation Delay $= \dfrac{t_{PHL} + t_{PLH}}{2}$

Fig. B EXPANDER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

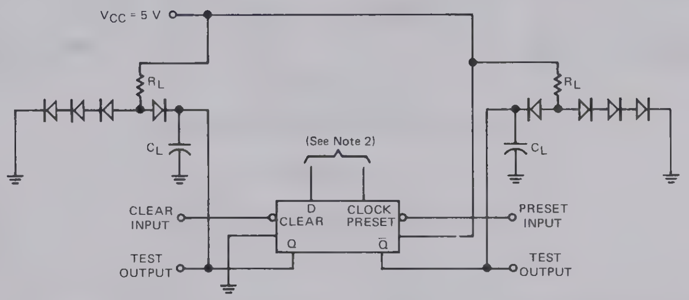
SWITCHING CHARACTERISTICS (Continued)



V_{CC} = 5 V
0.8 V
R_L
R_L
J*
K*
J1J2
K1K2
C_L*
C_L*
J CLOCK K
CLEAR PRESET
Q
$\overline{Q}$
CLEAR INPUT
PRESET INPUT
TEST OUTPUT
TEST OUTPUT

*C_L includes probe and jig capacitance.

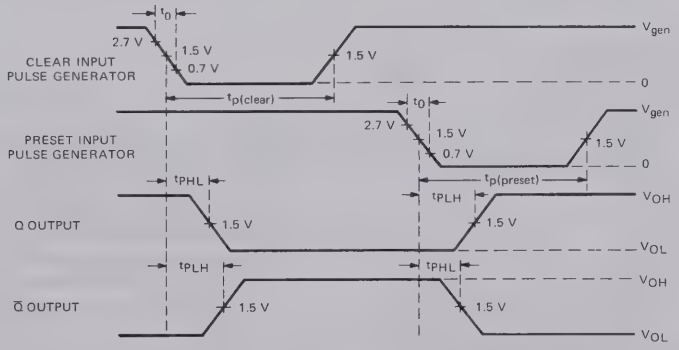
9N70/5470, 7470 TEST CIRCUIT



V_{CC} = 5 V
R_L
R_L
C_L
C_L
(See Note 2)
D CLOCK
CLEAR PRESET
Q
$\overline{Q}$
CLEAR INPUT
PRESET INPUT
TEST OUTPUT
TEST OUTPUT

9N74/5474, 7474 TEST CIRCUIT

NOTES:
1. Preset or clear function of the 9N70/5470, 7470 can occur only when clock input is low. Gated inputs are inhibited.
2. Clear and preset inputs of the 9N74/5474, 7474 dominate regardless of the state of clock or D inputs.



t_0
2.7 V
1.5 V
0.7 V
1.5 V
V_{gen}
0
CLEAR INPUT PULSE GENERATOR
$t_{p(clear)}$
t_0
2.7 V
1.5 V
0.7 V
1.5 V
V_{gen}
0
PRESET INPUT PULSE GENERATOR
$t_{p(preset)}$
t_{PHL}
t_{PLH}
Q OUTPUT
1.5 V
1.5 V
V_{OH}
V_{OL}
t_{PLH}
t_{PHL}
$\overline{Q}$ OUTPUT
1.5 V
1.5 V
V_{OH}
V_{OL}

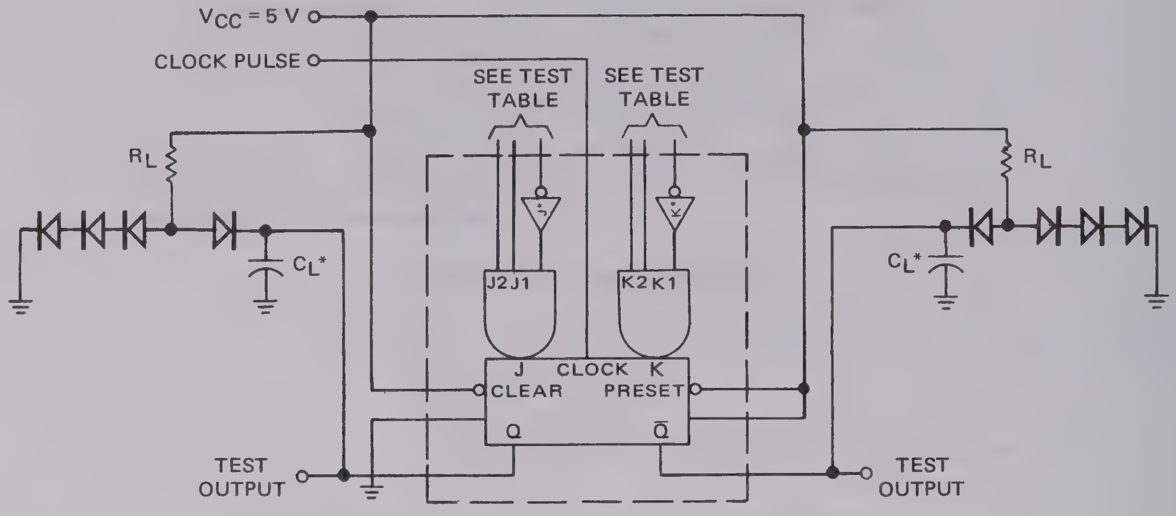
VOLTAGE WAVEFORMS

NOTE:
3. Clear or preset input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns, t_p = 25 ns for the 9N70/5470, 7470 and t_p = 30 ns for 9N74/5474, 7474.

Fig. C 9N70/5470, 7470 and 9N74/5474, 7474 PRESET/CLEAR PROPAGATION DELAY TIMES

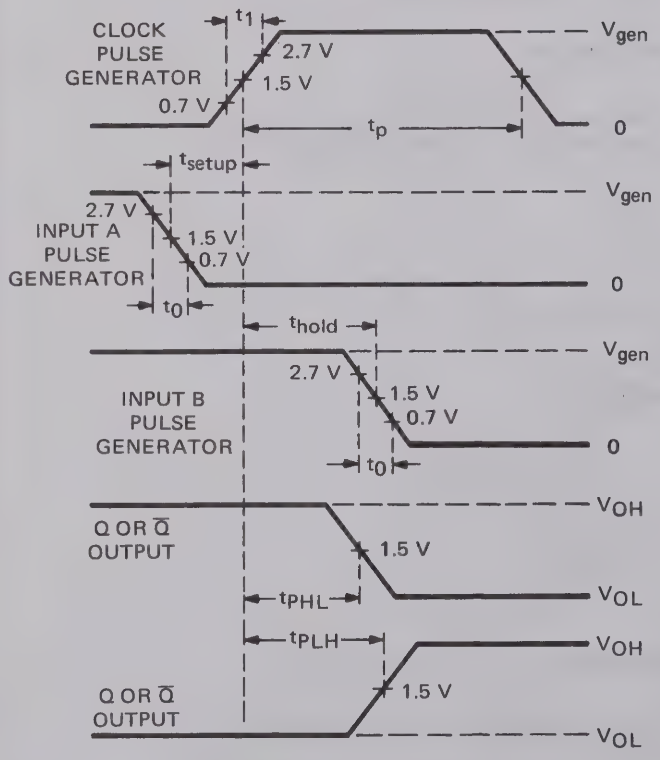
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


V_{CC} = 5 V
CLOCK PULSE
SEE TEST TABLE
SEE TEST TABLE
R_L
R_L
C_L*
C_L*
J2 J1
K2 K1
J CLOCK K
CLEAR PRESET
Q $\overline{Q}$
TEST OUTPUT
TEST OUTPUT

*C_L includes probe and jig capacitance.

TEST CIRCUIT


CLOCK PULSE GENERATOR
t_1
2.7 V
1.5 V
0.7 V
V_{gen}
0
t_p
t_{setup}
INPUT A PULSE GENERATOR
2.7 V
1.5 V
0.7 V
V_{gen}
0
t_0
t_{hold}
INPUT B PULSE GENERATOR
2.7 V
1.5 V
0.7 V
V_{gen}
0
t_0
Q OR $\overline{Q}$ OUTPUT
1.5 V
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Q OR $\overline{Q}$ OUTPUT
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS

TEST TABLE

Test No.	Test	Input A	Input B	Apply 2.4 V	GND
1	t_{setup} at J*	J*	None	J1, J2, K1, K2	K*
2	t_{hold} at J1, J2	None	J1, J2	K1, K2	J* and K*
3	t_{setup} at K*	K*	None	J1, J2, K1, K2	J*
4	t_{hold} at K1, K2	None	K1, K2	J1, J2	J* and K*

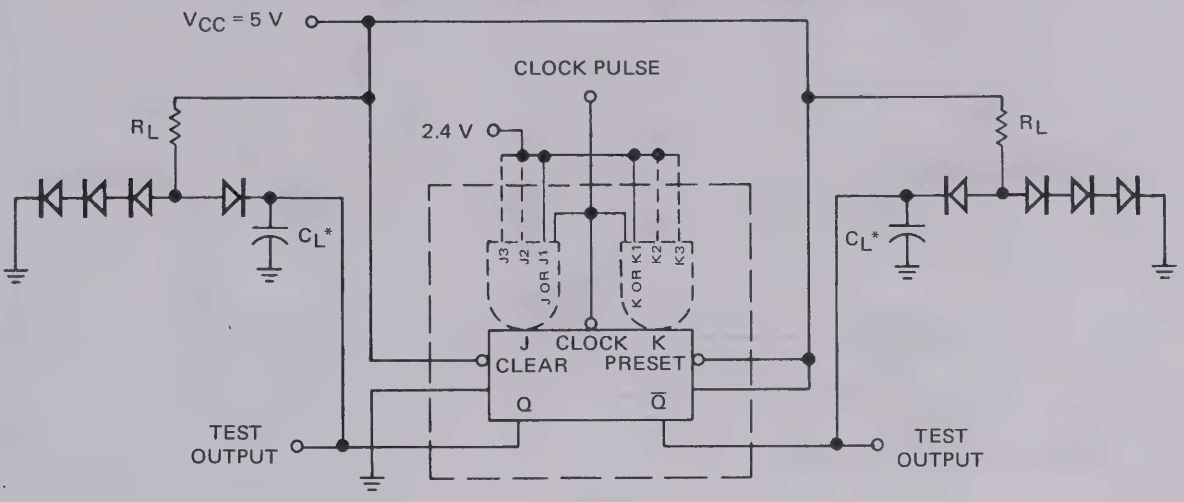
NOTES:

1. Clock pulse (see note 3), input A, and input B are used to measure t_{setup} and t_{hold}.
2. Clock frequency, t_{PLH} and t_{PHL} (from clock to output) are measured in the toggle mode. Hold J = K = high level per truth table and apply clock pulse (see note 3).
3. Clock pulse characteristics: V_{gen} = 3.5 V, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
4. Input pulse characteristics: V_{gen} = 3.5 V, t_0 = 5 ns.

Fig. D 9N70/5470, 7470 FLIP-FLOP SWITCHING TIMES

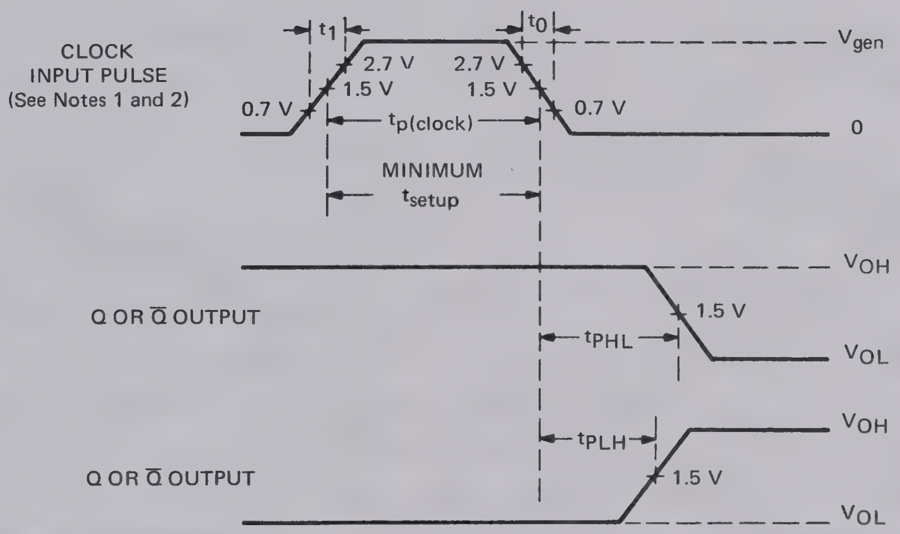
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


V_{CC} = 5 V
CLOCK PULSE
2.4 V
R_L
R_L
C_L*
C_L*
J3
J2
J OR J1
K OR K1
K2
K3
J
CLOCK
K
CLEAR
PRESET
Q
$\overline{Q}$
TEST OUTPUT
TEST OUTPUT

*C_L includes probe and jig capacitance.

TEST CIRCUIT


CLOCK INPUT PULSE (See Notes 1 and 2)
t_1
t_0
V_{gen}
2.7 V
2.7 V
1.5 V
1.5 V
0.7 V
0.7 V
0
$t_{p(clock)}$
MINIMUM t_{setup}
Q OR $\overline{Q}$ OUTPUT
V_{OH}
1.5 V
t_{PHL}
V_{OL}
Q OR $\overline{Q}$ OUTPUT
V_{OH}
t_{PLH}
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

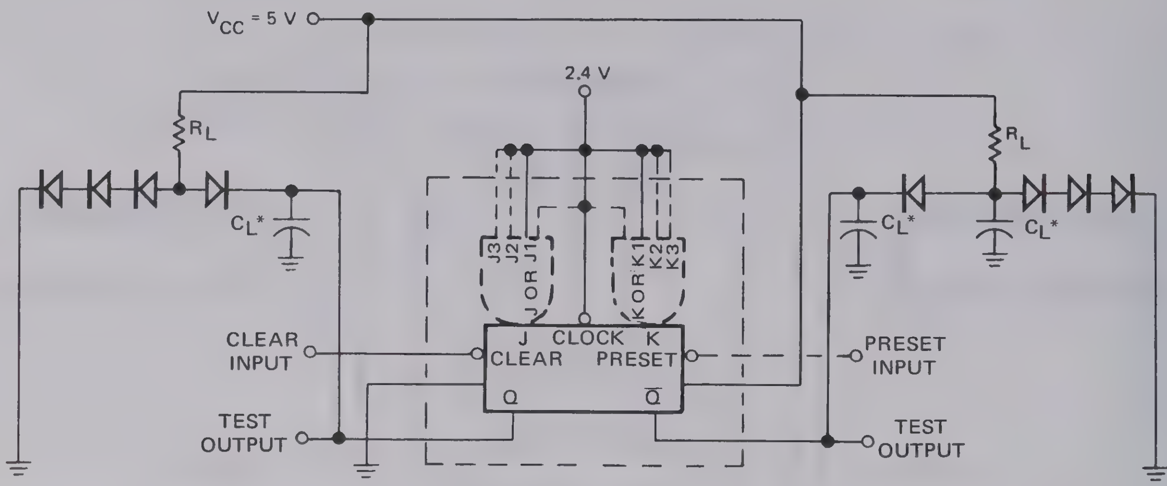
NOTES:

1. Clock, J, and K input pulse characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
2. For 9N72/5472, 7472, J = J1 · J2 · J3; and K = K1 · K2 · K3.
3. Gated inputs (shown with dotted lines) are for the 9N72/5472, 7472 only. The 9N73/5473, 7473; 9N107/54107, 74107 and 9N76/5476, 7476. Dual Flip-Flops have direct J and K inputs, and preset is not available on the 9N73/5473, 7473 and 9N107/54107, 74107.

Fig. E 9N72/5472, 7472; 9N73/5473, 7473; 9N76/5476, 7476; 9N107/54107, 74107 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

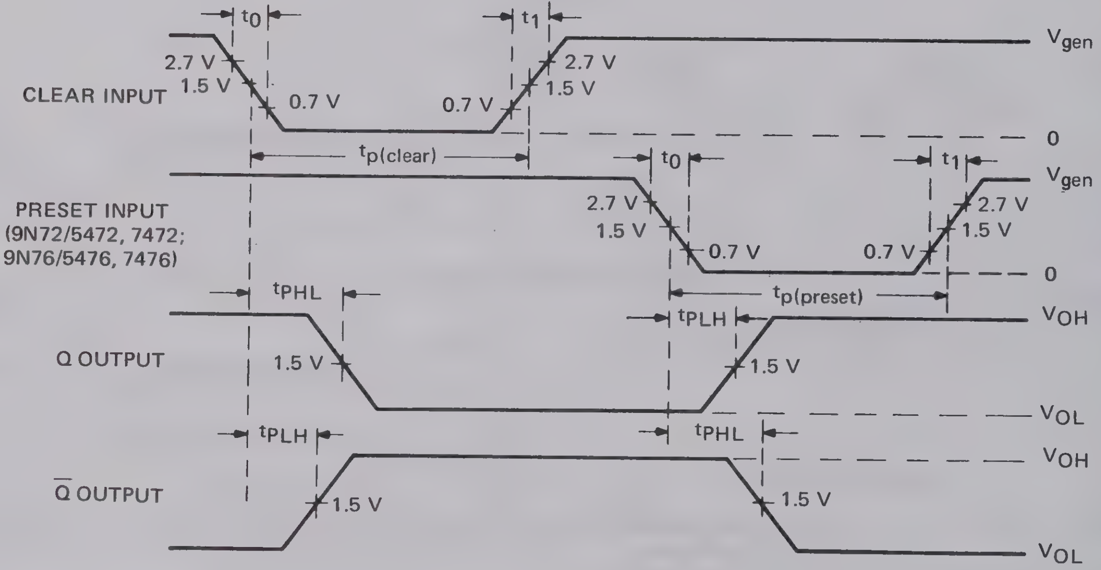
SWITCHING CHARACTERISTICS (Continued)



V_{CC} = 5 V
2.4 V
R_L
R_L
C_L*
C_L*
C_L*
J3
J2
J1
J OR
K OR
K1
K2
K3
J
CLOCK
K
CLEAR
PRESET
Q
$\overline{Q}$
CLEAR INPUT
PRESET INPUT
TEST OUTPUT
TEST OUTPUT

*C_L includes probe and jig capacitance

TEST CIRCUIT



t_0
t_1
V_{gen}
2.7 V
1.5 V
0.7 V
0
$t_{p(clear)}$
CLEAR INPUT
PRESET INPUT (9N72/5472, 7472; 9N76/5476, 7476)
$t_{p(preset)}$
t_{PHL}
t_{PLH}
Q OUTPUT
$\overline{Q}$ OUTPUT
V_{OH}
V_{OL}

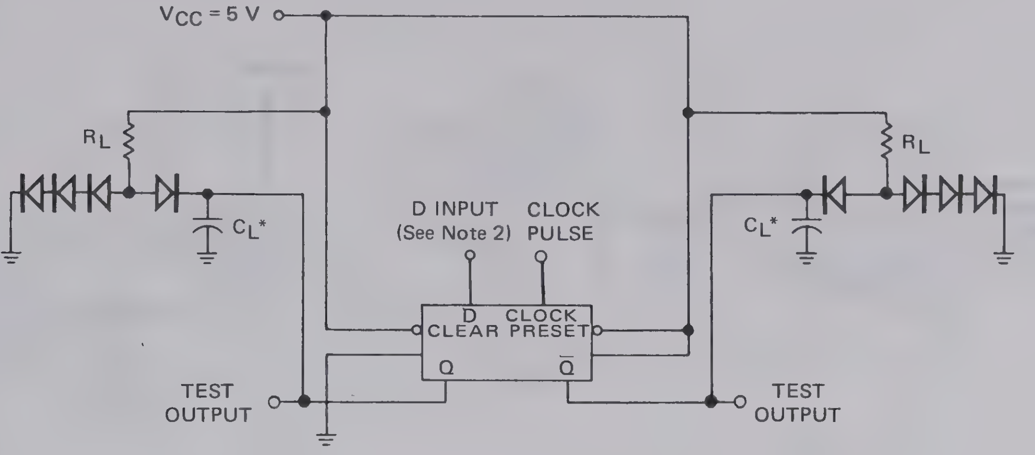
VOLTAGE WAVEFORMS

NOTES:
1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: V_{CC} = 3.5 V, t_0 = 5 ns, t_1 = 10 ns, $t_{p(clear)} = t_{p(preset)}$ = 25 ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
3. Gates inputs (shown with dotted lines) are for the 9N72/5472, 7472 only. The 9N73/5473, 7473; 9N76/5476, 7476 and 9N107/54107, 74107 Dual Flip-Flops have direct J and K inputs, and preset is not available on the 9N73/5473, 7473 or 9N107/54107, 74107.

Fig. F 9N72/5472, 7472; 9N73/5473, 7473; 9N76/5476, 7476; 9N107/54107, 74107 PRESET/CLEAR PROPAGATION DELAY TIMES

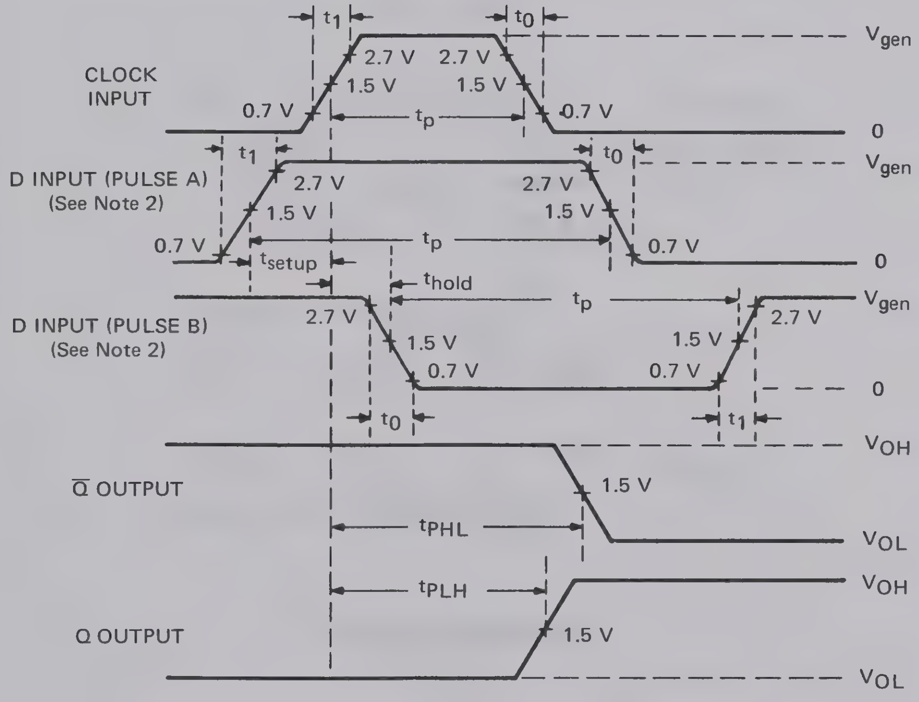
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


V_{CC} = 5 V
R_L
R_L
C_L*
C_L*
D INPUT
(See Note 2)
CLOCK
PULSE
D
CLOCK
CLEAR
PRESET
Q
$\overline{Q}$
TEST
OUTPUT
TEST
OUTPUT

*C_L includes probe and jib capacitance

TEST CIRCUIT


t_1
t_0
V_{gen}
CLOCK
INPUT
2.7 V
2.7 V
1.5 V
1.5 V
0.7 V
t_p
0.7 V
0
t_1
t_0
V_{gen}
D INPUT (PULSE A)
(See Note 2)
2.7 V
2.7 V
1.5 V
1.5 V
0.7 V
t_p
0.7 V
0
t_{setup}
t_{hold}
t_p
V_{gen}
D INPUT (PULSE B)
(See Note 2)
2.7 V
2.7 V
1.5 V
1.5 V
0.7 V
0.7 V
0
t_0
t_1
V_{OH}
$\overline{Q}$ OUTPUT
1.5 V
t_{PHL}
V_{OL}
t_{PLH}
V_{OH}
Q OUTPUT
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

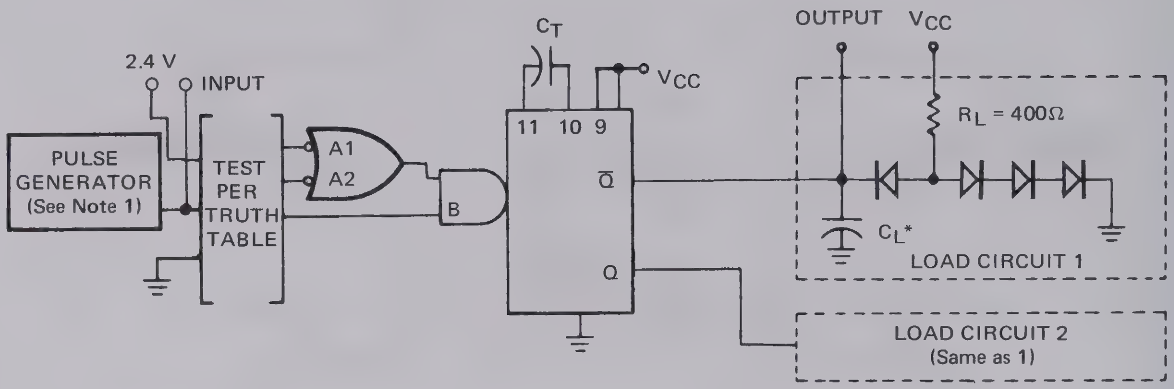
NOTES:

1. Clock input pulse has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_p = 30 ns, and PRR = 1 MHz. When testing f_{max}, vary PRR.
2. D input (pulse A) has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_{setup} = 20 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: V_{gen} = 3.5 V, t_0 = 10 ns, t_1 = 10 ns, t_{hold} = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.

Fig. G 9N74/5474, 7474 FLIP-FLOP SWITCHING TIMES

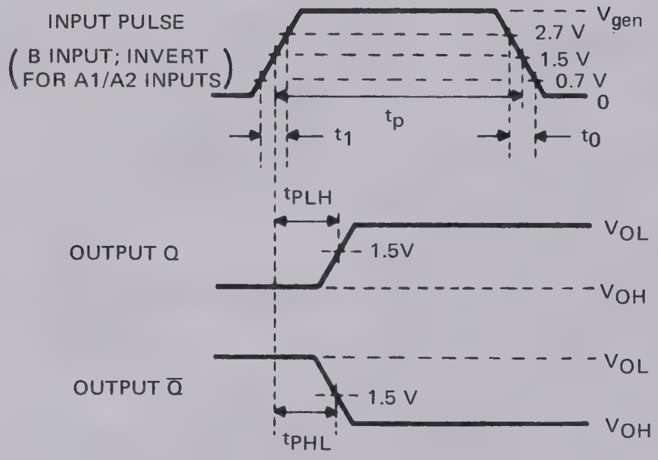
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


2.4 V
INPUT
PULSE GENERATOR (See Note 1)
TEST PER TRUTH TABLE
A1
A2
B
C_T
11 10 9
V_{CC}
$\overline{Q}$
Q
OUTPUT
V_{CC}
$R_L = 400\Omega$
C_L*
LOAD CIRCUIT 1
LOAD CIRCUIT 2 (Same as 1)

*C_L includes probe and jig capacitance

TEST CIRCUIT


INPUT PULSE
(B INPUT; INVERT FOR A1/A2 INPUTS)
V_{gen}
2.7 V
1.5 V
0.7 V
0
t_p
t_1
t_0
t_{PLH}
OUTPUT Q
1.5V
V_{OL}
V_{OH}
OUTPUT $\overline{Q}$
1.5 V
V_{OL}
V_{OH}
t_{PHL}

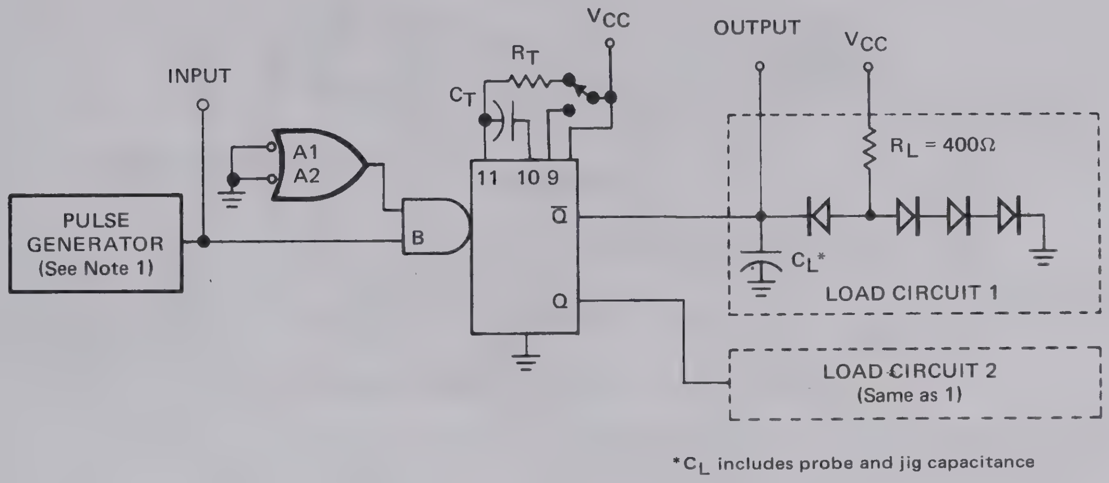
VOLTAGE WAVEFORMS

NOTE:
1. The pulse generator has the following characteristics: $V_{gen} = 3.5$ V, $t_0 = 5$ ns, $t_1 = 10$ ns, $t_p \geq 50$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.

Fig. H 9N121/54121, 74121 SWITCHING TIMES

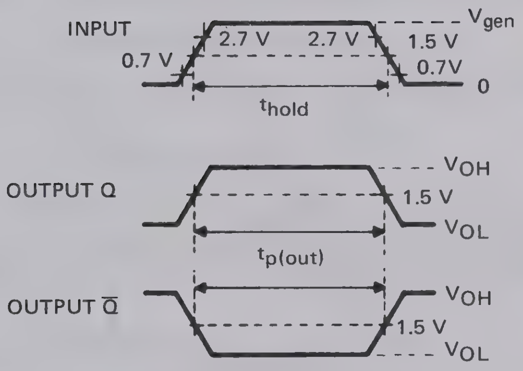
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


INPUT
PULSE GENERATOR (See Note 1)
A1
A2
B
C_T
R_T
V_{CC}
11 10 9
$\overline{Q}$
Q
OUTPUT
V_{CC}
$R_L = 400\Omega$
C_L*
LOAD CIRCUIT 1
LOAD CIRCUIT 2 (Same as 1)

*C_L includes probe and jig capacitance

TEST CIRCUIT


INPUT
0.7 V
2.7 V
2.7 V
1.5 V
0.7V
V_{gen}
0
t_{hold}
OUTPUT Q
V_{OH}
1.5 V
V_{OL}
$t_{p(out)}$
OUTPUT $\overline{Q}$
V_{OH}
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

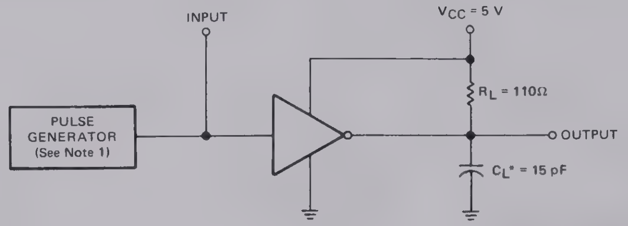
NOTE:

1. The pulse generator has the following characteristics: $V_{gen} = 3.5$ V, $t_0 = 5$ ns, $t_1 = 10$ ns, $t_p = 50$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.

Fig. 1 $t_{p(out)}$ (internal/minimum), t_{hold}

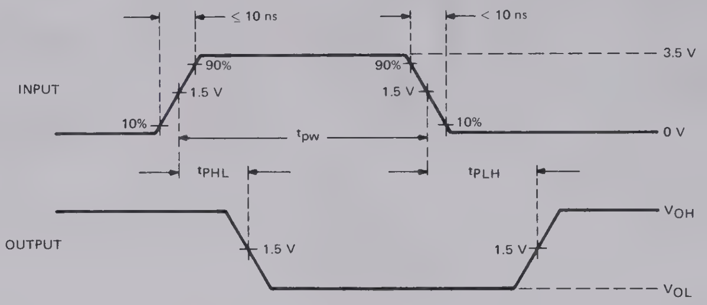
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


INPUT
V_{CC} = 5 V
R_L = 110Ω
PULSE GENERATOR (See Note 1)
OUTPUT
C_L* = 15 pF

*C_L includes probe and jig capacitance

TEST CIRCUIT

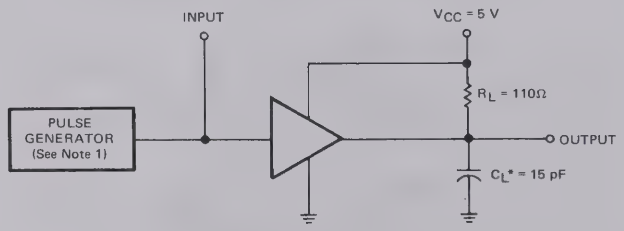

≤ 10 ns
< 10 ns
3.5 V
INPUT
90%
90%
1.5 V
1.5 V
10%
10%
0 V
t_{pw}
t_{PHL}
t_{PLH}
V_{OH}
OUTPUT
1.5 V
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

NOTE:

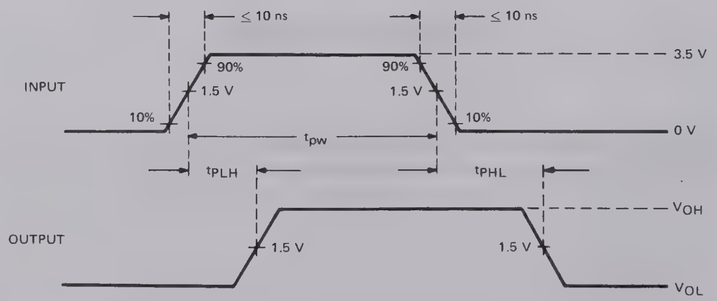
1. The generator has the following characteristics: t_{pw} = 0.5 μs, PRR = 1 MHz, Z_{out} ≈ 50Ω.

Fig. J PROPAGATION DELAY TIMES


INPUT
V_{CC} = 5 V
R_L = 110Ω
PULSE GENERATOR (See Note 1)
OUTPUT
C_L* = 15 pF

*C_L includes probe and jig capacitance.

TEST CIRCUIT


≤ 10 ns
≤ 10 ns
3.5 V
INPUT
90%
90%
1.5 V
1.5 V
10%
10%
0 V
t_{pw}
t_{PLH}
t_{PHL}
V_{OH}
OUTPUT
1.5 V
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

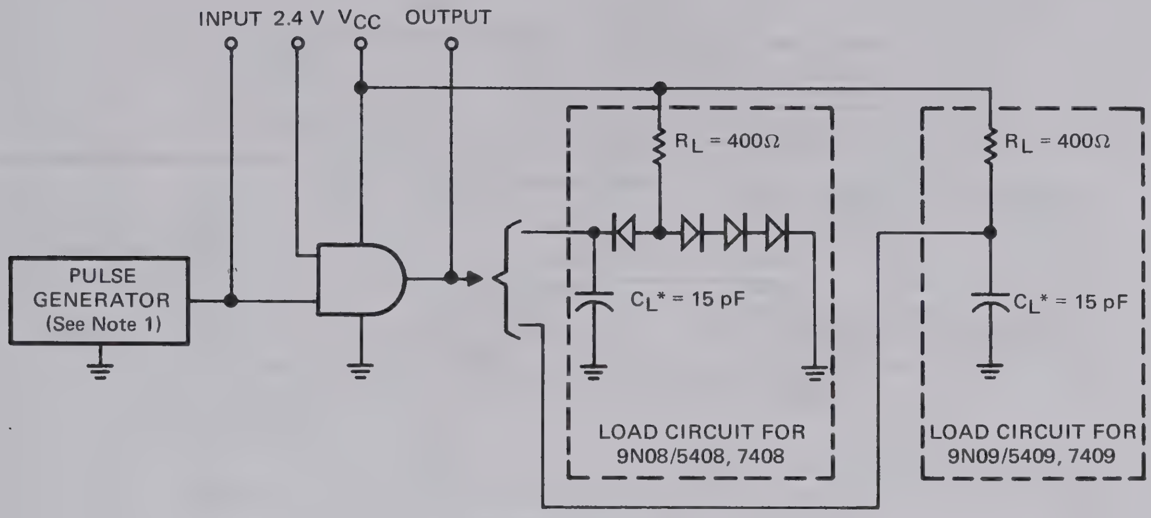
NOTE:

1. The generator has the following characteristics: t_{pw} = 0.5 μs, PRR = 1 MHz, Z_{out} ≈ 50Ω.

Fig. K PROPAGATION DELAY TIMES

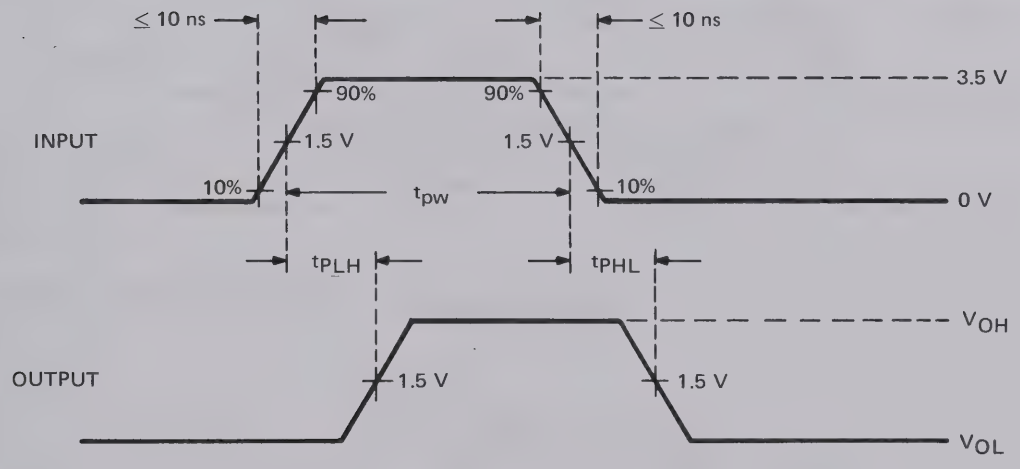
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


INPUT
2.4 V
V_{CC}
OUTPUT
PULSE GENERATOR (See Note 1)
$R_L = 400\Omega$
$C_L^* = 15$ pF
LOAD CIRCUIT FOR 9N08/5408, 7408
$R_L = 400\Omega$
$C_L^* = 15$ pF
LOAD CIRCUIT FOR 9N09/5409, 7409

*C_L includes probe and jig capacitance.

TEST CIRCUIT


≤ 10 ns
≤ 10 ns
3.5 V
90%
90%
INPUT
1.5 V
1.5 V
10%
10%
t_{pw}
0 V
t_{PLH}
t_{PHL}
V_{OH}
OUTPUT
1.5 V
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

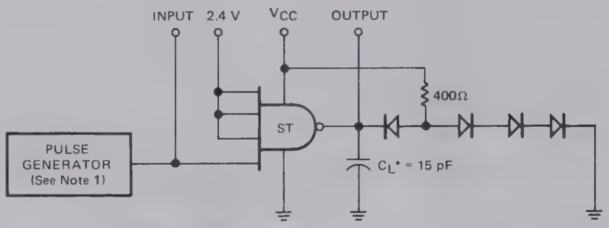
NOTE:

1. The generator has the following characteristics: $t_{pw} = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

Fig. L PROPAGATION DELAY TIMES

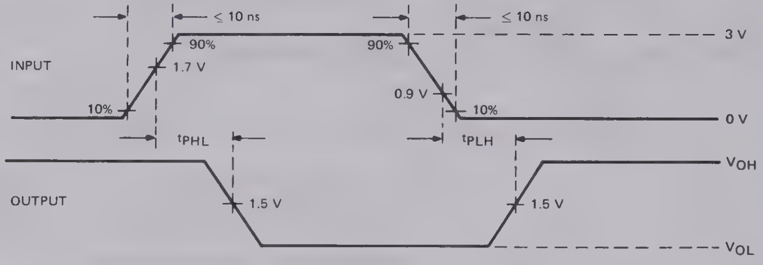
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


INPUT
2.4 V
VCC
OUTPUT
400Ω
ST
PULSE GENERATOR (See Note 1)
CL* = 15 pF

*C_L includes probe and jig capacitance

TEST CIRCUIT

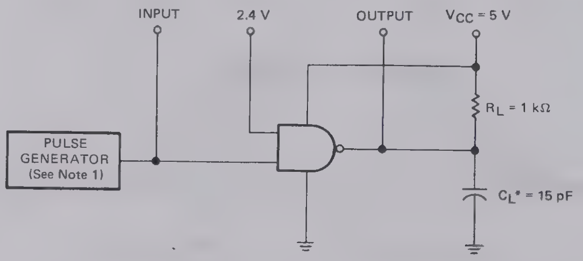

≤ 10 ns
≤ 10 ns
3 V
INPUT
90%
90%
1.7 V
0.9 V
10%
10%
0 V
tPHL
tPLH
VOH
OUTPUT
1.5 V
1.5 V
VOL

VOLTAGE WAVEFORMS

NOTE:

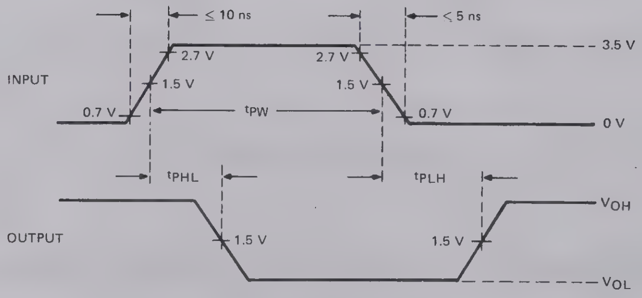
1. The pulse generator has the following characteristics: $t_{pw} = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

Fig. M PROPAGATION DELAY TIMES


INPUT
2.4 V
OUTPUT
VCC = 5 V
RL = 1 kΩ
PULSE GENERATOR (See Note 1)
CL* = 15 pF

*C_L includes probe and jig capacitance.

TEST CIRCUIT


≤ 10 ns
< 5 ns
3.5 V
INPUT
2.7 V
2.7 V
1.5 V
1.5 V
0.7 V
0.7 V
tPW
0 V
tPHL
tPLH
VOH
OUTPUT
1.5 V
1.5 V
VOL

VOLTAGE WAVEFORMS

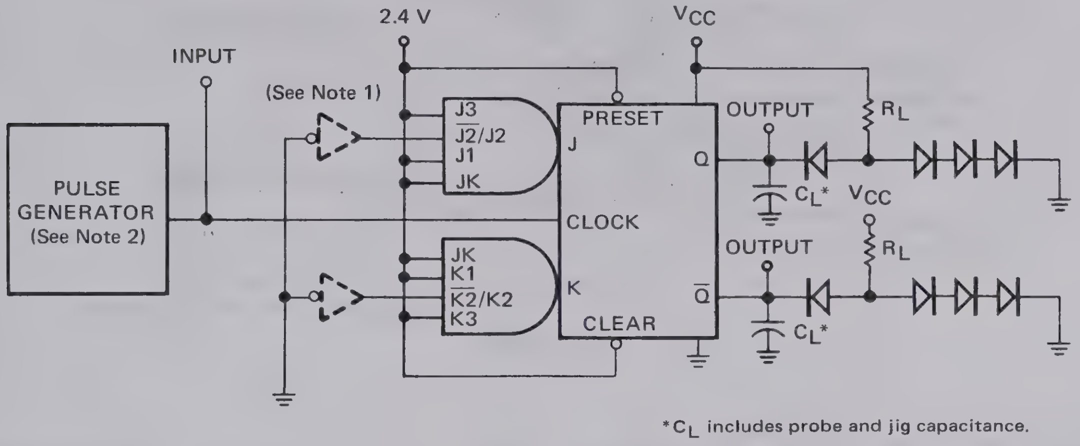
NOTE:

1. The generator has the following characteristics: $t_{pw} = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

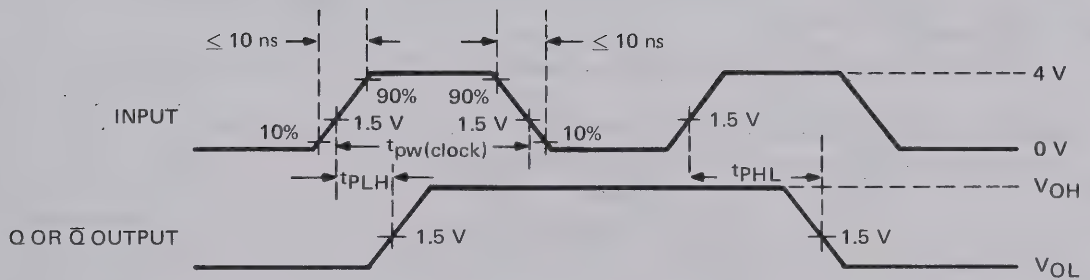
Fig. N PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


2.4 V
VCC
INPUT
(See Note 1)
PULSE GENERATOR (See Note 2)
J3
J2/J2
J1
JK
K1
K2/K2
K3
PRESET
J
CLOCK
K
CLEAR
Q
Q̄
OUTPUT
RL
CL*
VCC
*CL includes probe and jig capacitance.

TEST CIRCUIT


≤ 10 ns
≤ 10 ns
INPUT
10%
90%
90%
1.5 V
1.5 V
10%
tpw(clock)
1.5 V
4 V
0 V
tPLH
tPHL
VOH
Q OR Q̄ OUTPUT
1.5 V
1.5 V
VOL

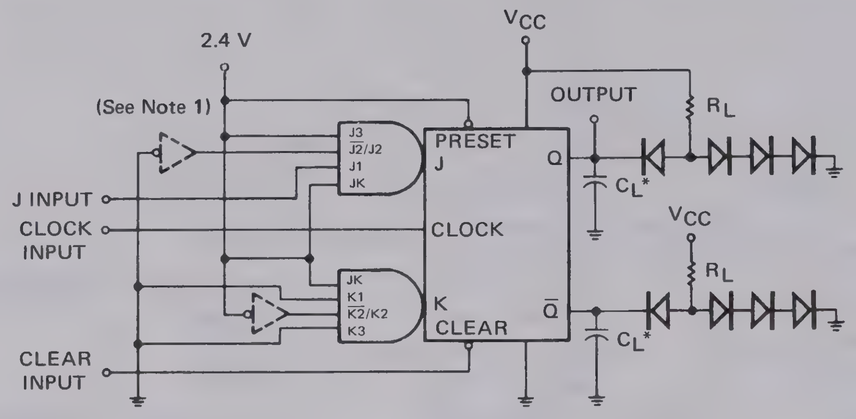
VOLTAGE WAVEFORMS

NOTES:
1. Test circuit shown is for the 9N105/54105, 74105. When testing 9N104/54104, 74104, the J2 and K2 inputs are connected in parallel with the other J and K inputs.
2. The pulse generator has the following characteristics: $t_{pw(clock)} = 250$ ns, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

Fig. O PROPAGATION DELAY TIMES

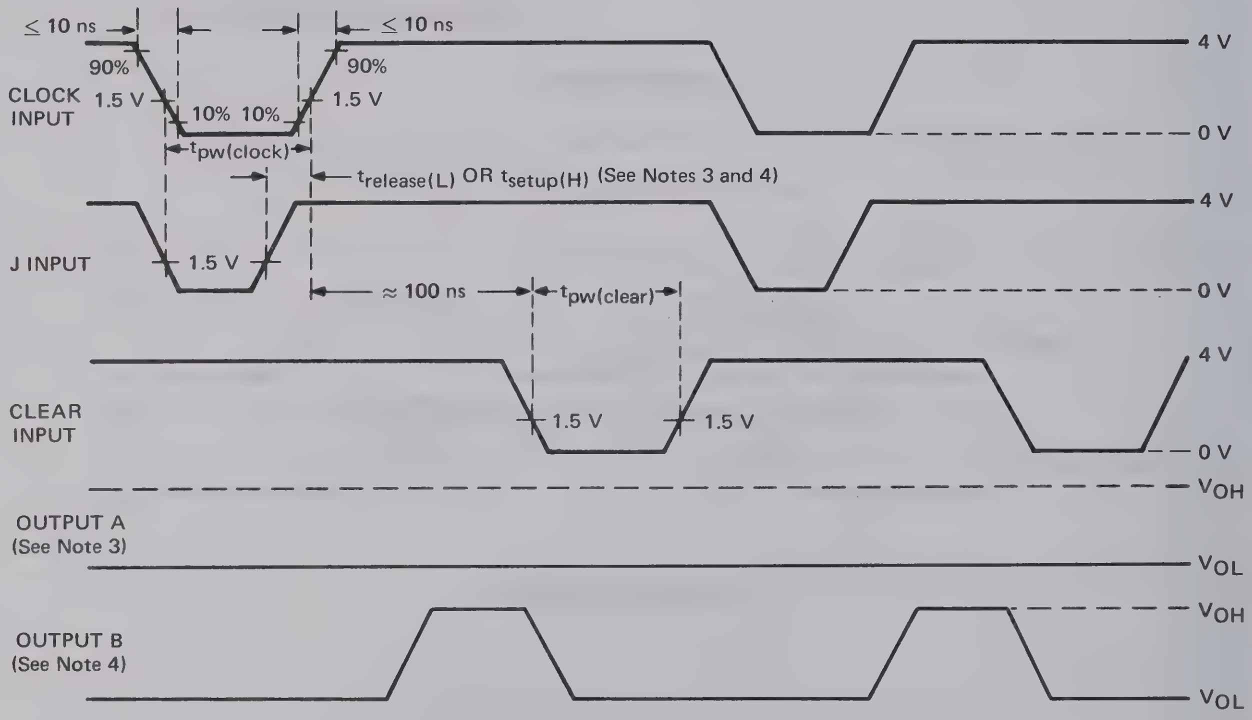
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


2.4 V
(See Note 1)
VCC
OUTPUT
RL
J3
J2/J2
J1
JK
PRESET
J
Q
CL*
J INPUT
CLOCK INPUT
CLOCK
VCC
RL
JK
K1
K2/K2
K3
K
CLEAR
Q̄
CL*
CLEAR INPUT

*C_L includes probe and jig capacitance

TEST CIRCUIT


≤ 10 ns
≤ 10 ns
90%
90%
CLOCK INPUT
1.5 V
1.5 V
10%
10%
tpw(clock)
trelease(L) OR tsetup(H) (See Notes 3 and 4)
4 V
0 V
4 V
J INPUT
1.5 V
≈ 100 ns
tpw(clear)
0 V
4 V
CLEAR INPUT
1.5 V
1.5 V
0 V
VOH
OUTPUT A (See Note 3)
VOL
VOH
OUTPUT B (See Note 4)
VOL

VOLTAGE WAVEFORMS

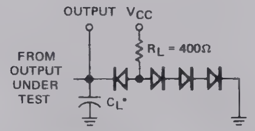
NOTES:

1. Test circuit shown is for the 9N105/54105, 74105. When testing 9N104/54104, 74104, the J2 input is connected in parallel with the other J inputs and K2 is grounded.
2. The input pulses have the following characteristics: PRR = 1 MHz, $t_{pw(clock)} = 100$ ns, and $t_{w(clear)} = 100$ ns. For duration of the J-input pulse, see Notes 3 and 4.
3. Output A is valid for: 9N104/54104, 74104, $t_{release(L)} \leq 10$ ns; 9N105/54105, 74105, $t_{release(L)} \leq 1$ ns.
4. Output B is valid for: 9N104/54104, 74104, $t_{setup(H)} \geq 35$ ns; 9N105/54105, 74105, $t_{setup(H)} \geq 10$ ns.

Fig. P INPUT SETUP/RELEASE TIMES

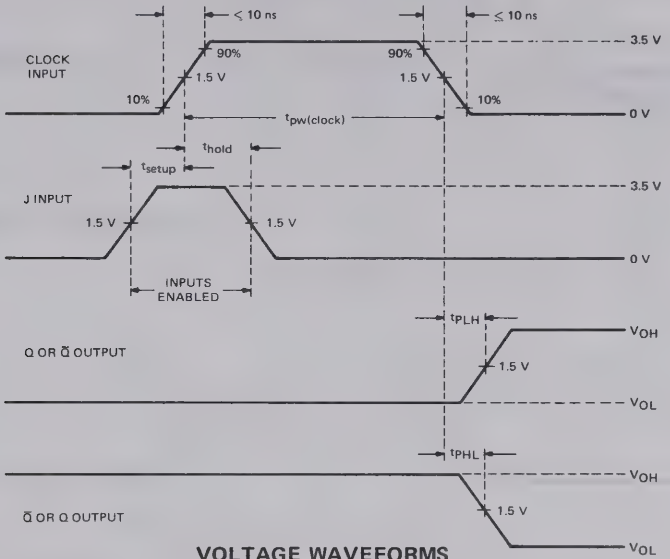
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


OUTPUT
V_{CC}
$R_L = 400\Omega$
FROM OUTPUT UNDER TEST
C_L*

*C_L includes probe and jig capacitance.

LOAD FOR OUTPUT UNDER TEST

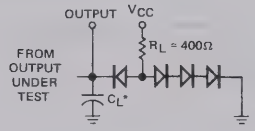

≤ 10 ns
≤ 10 ns
3.5 V
CLOCK INPUT
90%
90%
1.5 V
1.5 V
10%
10%
0 V
$t_{pw(clock)}$
t_{hold}
t_{setup}
3.5 V
J INPUT
1.5 V
1.5 V
0 V
INPUTS ENABLED
t_{PLH}
V_{OH}
Q OR $\bar{Q}$ OUTPUT
1.5 V
V_{OL}
t_{PHL}
V_{OH}
$\bar{Q}$ OR Q OUTPUT
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

NOTE:

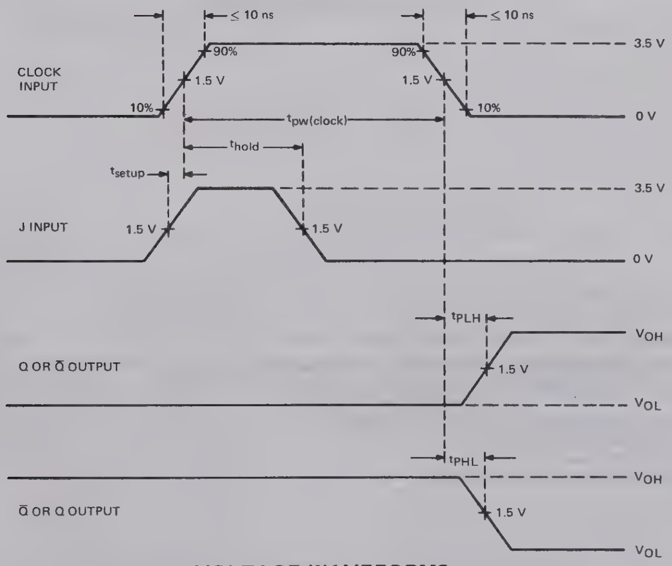
1. Both input pulses are supplied by generators with the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\Omega$. Clock duty cycle = 50%.

Fig. Q


OUTPUT
V_{CC}
$R_L = 400\Omega$
FROM OUTPUT UNDER TEST
C_L*

*C_L includes probe and jig capacitance.

LOAD FOR OUTPUT UNDER TEST


≤ 10 ns
≤ 10 ns
3.5 V
CLOCK INPUT
90%
90%
1.5 V
1.5 V
10%
10%
0 V
$t_{pw(clock)}$
t_{hold}
t_{setup}
3.5 V
J INPUT
1.5 V
1.5 V
0 V
t_{PLH}
V_{OH}
Q OR $\bar{Q}$ OUTPUT
1.5 V
V_{OL}
t_{PHL}
V_{OH}
$\bar{Q}$ OR Q OUTPUT
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

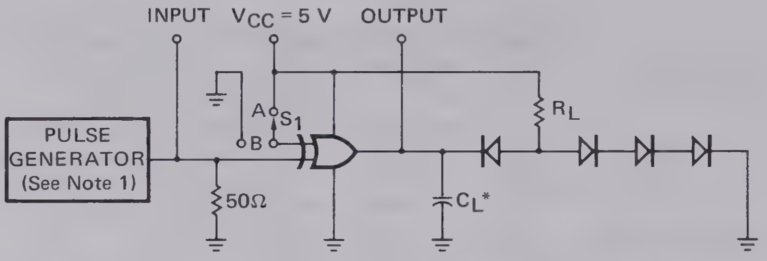
NOTE:

1. Both input pulses are supplied by generators with the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\Omega$, clock duty cycle = 50%.

Fig. R

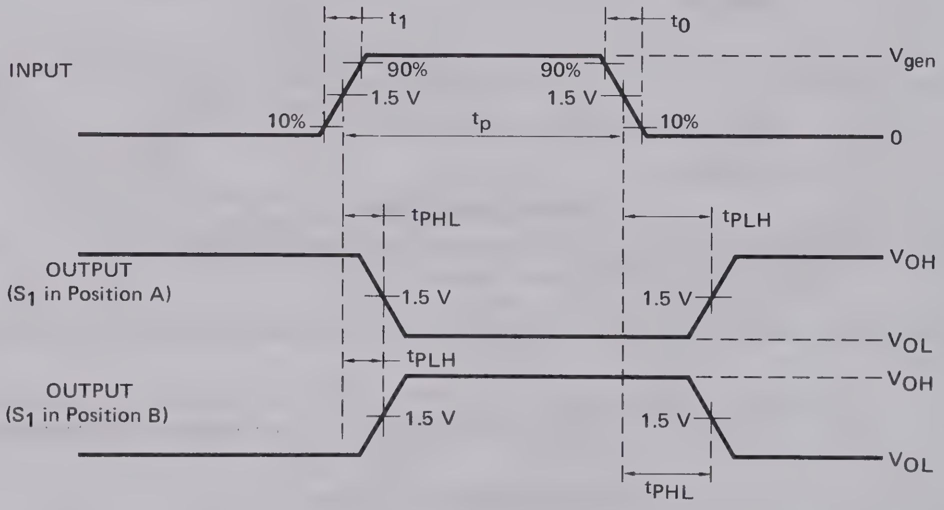
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


INPUT
$V_{CC} = 5$ V
OUTPUT
PULSE GENERATOR (See Note 1)
A
B
S_1
50Ω
R_L
C_L*

*C_L includes probe and jig capacitance

TEST CIRCUIT


t_1
t_0
INPUT
V_{gen}
90%
90%
1.5 V
1.5 V
10%
10%
t_p
0
t_{PHL}
t_{PLH}
OUTPUT (S_1 in Position A)
1.5 V
1.5 V
V_{OH}
V_{OL}
t_{PLH}
OUTPUT (S_1 in Position B)
1.5 V
1.5 V
V_{OH}
V_{OL}
t_{PHL}

VOLTAGE WAVEFORMS

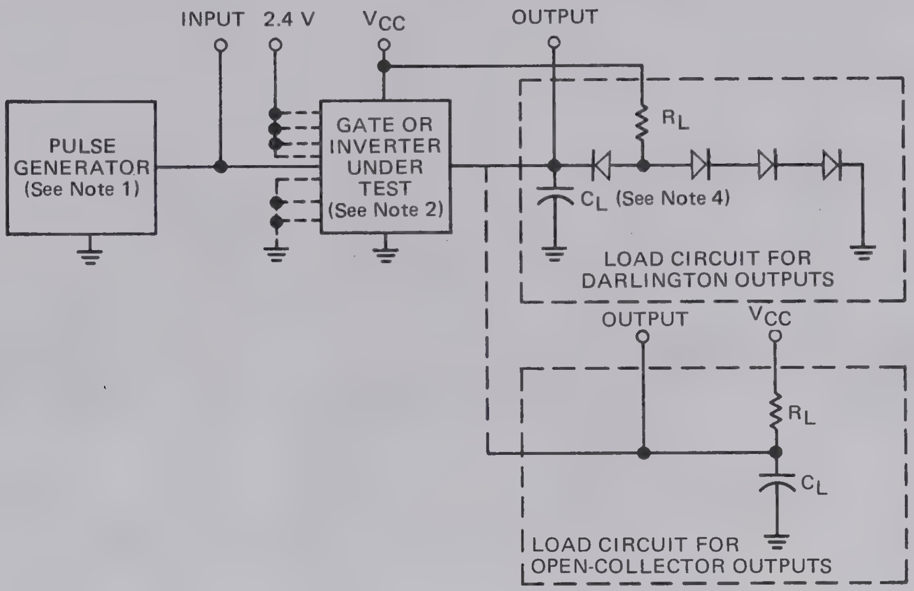
NOTES:

1. The generator has the following characteristics: $V_{gen} = 3.0$ V, $t_0 = t_1 \leq 15$ ns $t_p = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation Delay $= \dfrac{t_{PHL} + t_{PLH}}{2}$
3. Each gate tested separately.

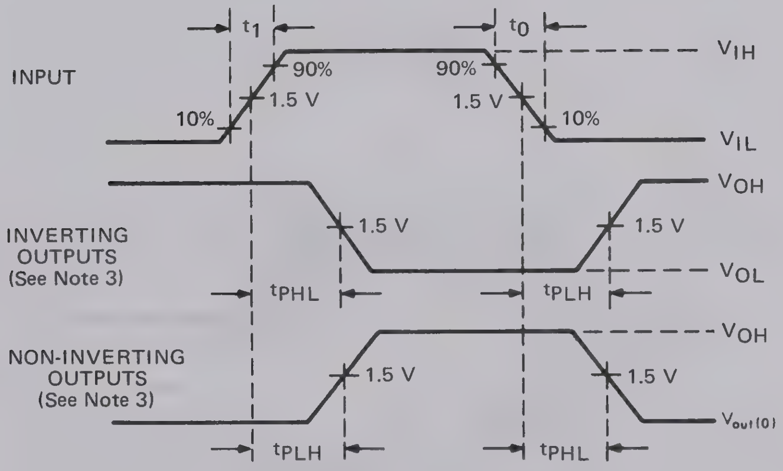
Fig. S

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS


INPUT
2.4 V
V_CC
OUTPUT
PULSE GENERATOR (See Note 1)
GATE OR INVERTER UNDER TEST (See Note 2)
R_L
C_L (See Note 4)
LOAD CIRCUIT FOR DARLINGTON OUTPUTS
OUTPUT
V_CC
R_L
C_L
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

TEST CIRCUIT


t1
t0
V_IH
INPUT
90%
90%
1.5 V
1.5 V
10%
10%
V_IL
V_OH
INVERTING OUTPUTS (See Note 3)
1.5 V
1.5 V
V_OL
tPHL
tPLH
V_OH
NON-INVERTING OUTPUTS (See Note 3)
1.5 V
1.5 V
V_out(0)
tPLH
tPHL

VOLTAGE WAVEFORMS

NOTES:

1 The pulse generator has the following characteristics: $V_{IH} = 3$ V, $V_{IL} = 0$ V, $t_1 = t_0 = 7$ ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{OUT} \approx 50\Omega$.

2 Input conditions are established for each gate as follows:
  - a. Input pulse is applied to one input and 2.4 V is applied to all unused inputs of the 9H00/54H00, 74H00; 9H01/54H01, 74H01; 9H04/54H04, 74H04; 9H05/54H05, 74H05; 9H10/54H10, 74H10; 9H11/54H11, 74H11; 9H20/54H20, 74H20; 9H21/54H21, 74H21; 9H22/54H22, 74H22; 9H30/54H30, 74H30; or 9H40/54H40, 74H40 gate.
  - b. Input pulse is applied to one input of one AND section, and 2.4 V is applied to all unused inputs of that AND section of the 9H50/54H50, 74H50; 9H51/54H51, 74H51; 9H52/54H52, 74H52; 9H53/54H53, 74H53; 9H54/54H54, 74H54; or 9H55/54H55, 74H55 gate. All inputs of all unused AND sections are grounded.

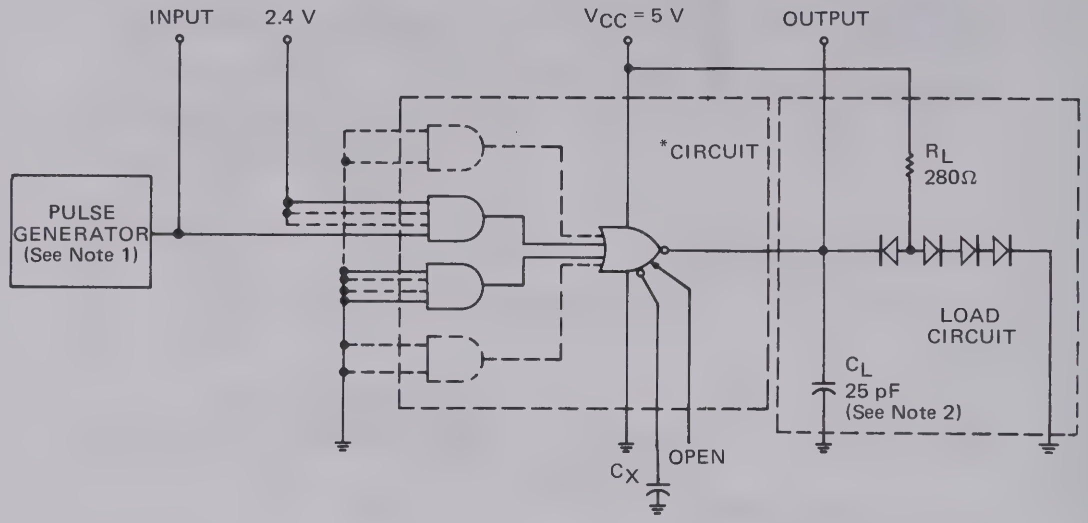
3 All gates are inverting except the 9H11/54H11, 74H11; 9H21/54H21, 74H21; and 9H52/54H52, 74H52 only.

4 C_L includes probe and jig capacitance.

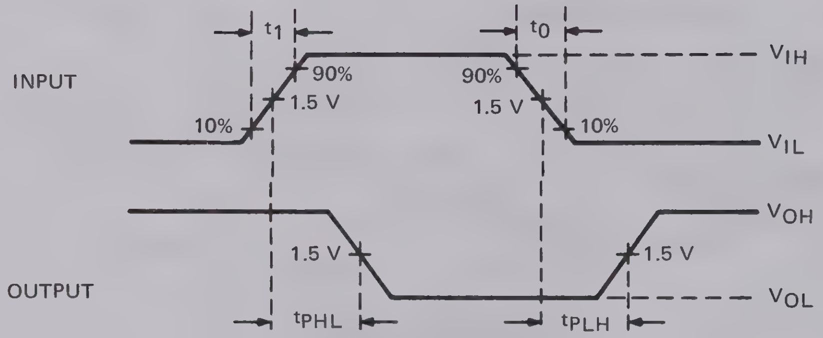
Fig. T GATE PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


INPUT
2.4 V
VCC = 5 V
OUTPUT
PULSE GENERATOR (See Note 1)
*CIRCUIT
RL 280Ω
LOAD CIRCUIT
CL 25 pF (See Note 2)
CX
OPEN

TEST CIRCUIT


t1
t0
INPUT
VIH
VIL
90%
1.5 V
10%
OUTPUT
VOH
VOL
tPHL
tPLH

VOLTAGE WAVEFORMS

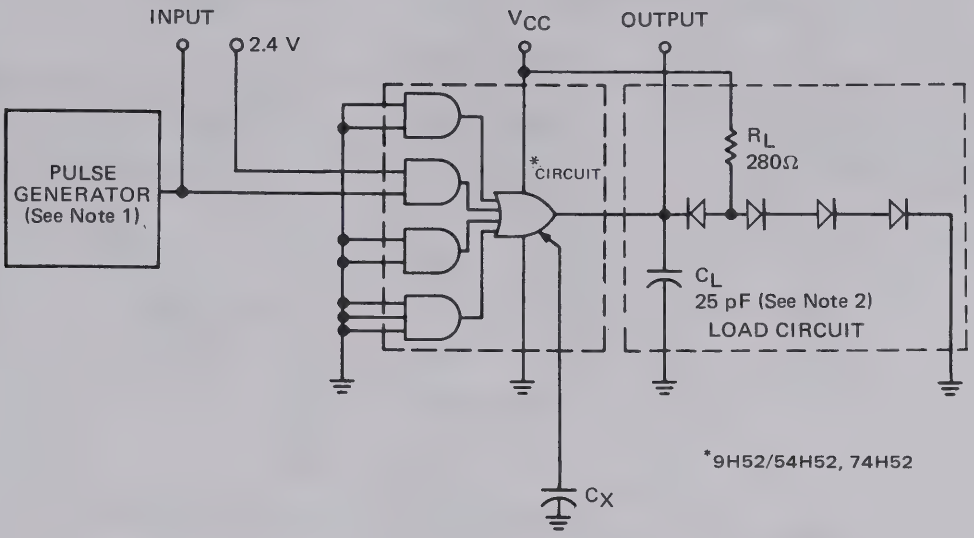
NOTES:
1 The generator has the following characteristics: $V_{IH} = 3$ V, $V_{IL} = 0$ V, $t_0 = t_1 = 7$ ns, duty cycle = 50%, PRR = 1 MHz $Z_{OUT} \approx 50\Omega$.
2 C_L includes probe and jig capacitance
3 C_X includes jig capacitance.

*9H50/54H50, 74H50; 9H53/54H53, 74H53; 9H55/54H55, 74H55

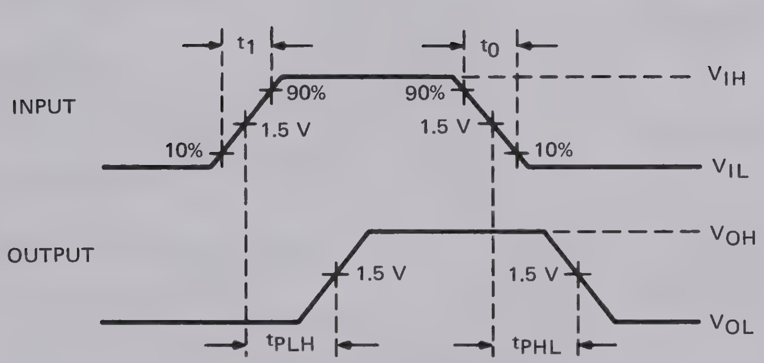
Fig. U PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


INPUT
2.4 V
V_{CC}
OUTPUT
PULSE GENERATOR (See Note 1)
*CIRCUIT
R_L 280Ω
C_L 25 pF (See Note 2)
LOAD CIRCUIT
*9H52/54H52, 74H52
C_X

TEST CIRCUIT


t_1
t_0
V_{IH}
INPUT
90%
90%
1.5 V
1.5 V
10%
10%
V_{IL}
OUTPUT
V_{OH}
1.5 V
1.5 V
V_{OL}
t_{PLH}
t_{PHL}

VOLTAGE WAVEFORMS

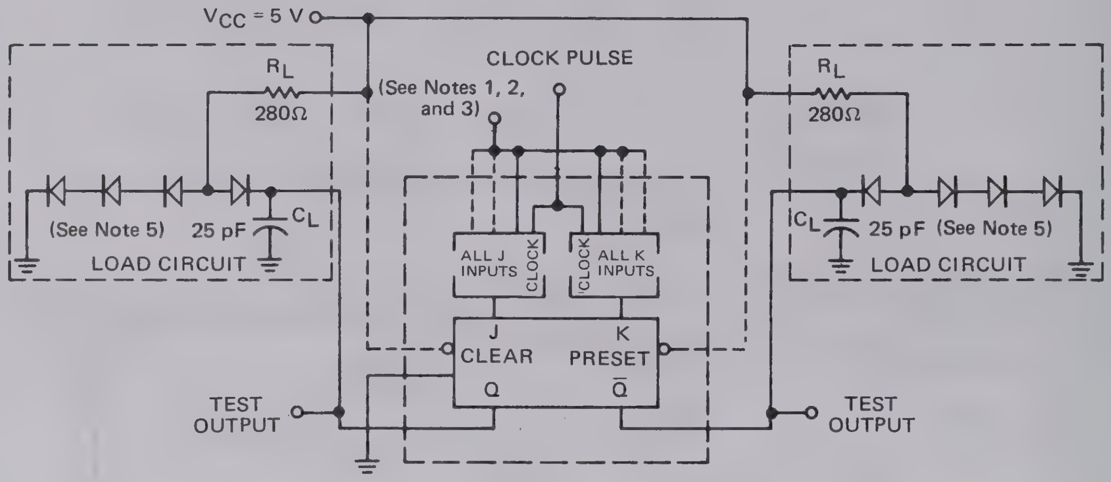
NOTES:

1 The generator has the following characteristics: $V_{IH} = 3$ V, $V_{IL} = 0$ V, $t_0 = t_1 = 7$ ns, duty cycle = 50%, PRR = 1 MHz, $V_{OUT} \approx 50\Omega$.
2 C_L includes probe and jig capacitance.
3 C_X includes jig capacitance.

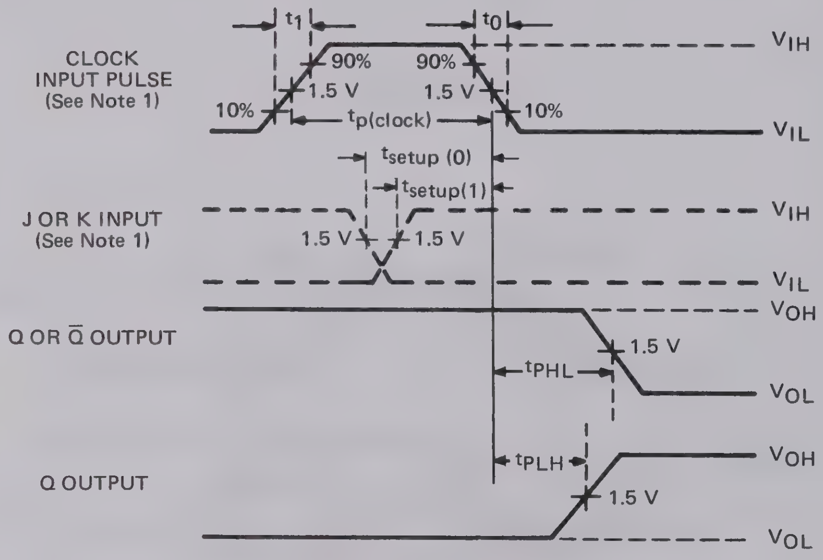
Fig. V PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


VCC = 5 V
RL
280Ω
CLOCK PULSE
(See Notes 1, 2, and 3)
(See Note 5)
25 pF
CL
LOAD CIRCUIT
ALL J INPUTS
CLOCK
ALL K INPUTS
J
K
CLEAR
PRESET
Q
Q̄
TEST OUTPUT

TEST CIRCUIT


t1
t0
VIH
CLOCK INPUT PULSE (See Note 1)
90%
1.5 V
10%
tp(clock)
VIL
tsetup (0)
tsetup(1)
J OR K INPUT (See Note 1)
Q OR Q̄ OUTPUT
VOH
VOL
tPHL
tPLH
Q OUTPUT

VOLTAGE WAVEFORMS

NOTES:

1 When testing t_{PHL} and t_{PLH} (all types), the clock input pulse characteristics are: $V_{IH} = 3$ V, $V_{IL} = 0$ V, $t_1 = t_0 = 7$ ns, $t_{p(clock)} = 20$ ns, and PRR = 1 MHz. When testing 9H71/54H71, 74H71; 9H72/54H72, 74H72; 9H73/54H73, 74H73; 9H76/54H76, 74H76 and 9H78/54H78, 74H78 all J and K inputs are at 2.4 V. When testing 9H101/54H101, 74H101; 9H102/54H102, 74H102; 9H103/54H103, 74H103; 9H106/54H106, 74H106 and 9H108/54H108, 74H108 conditions are established to ensure that minimum setup times are verified.

2 When testing f_{clock} of 9H71/54H71, 74H71; 9H72/54H72, 74H72; 9H73/54H73, 74H73; 9H76/54H76, 74H76 and 9H78/54H78, 74H78, the clock input characteristics are: $V_{IH} = 3$ V, $V_{IL} = 0$ V, $t_1 = t_0 = 3$ ns, $t_{p(clock)} = 12$ ns, and PRR = 25 MHz. All J and K inputs are at 2.4 V.

3 When testing f_{clock} of 9H101/54H101, 74H101; 9H102/54H102, 74H102; 9H103/54H103, 74H103; 9H106/54H106, 74H106 and 9H108/54H108, 74H018, the clock input characteristics are: $V_{IH} = 3$ V, $V_{IL} = 0$, $t_1 = t_0 = 3$ ns, $t_{p(clock)} = 10$ ns and PRR = 40 MHz. All J and K inputs are at 2.4 V.

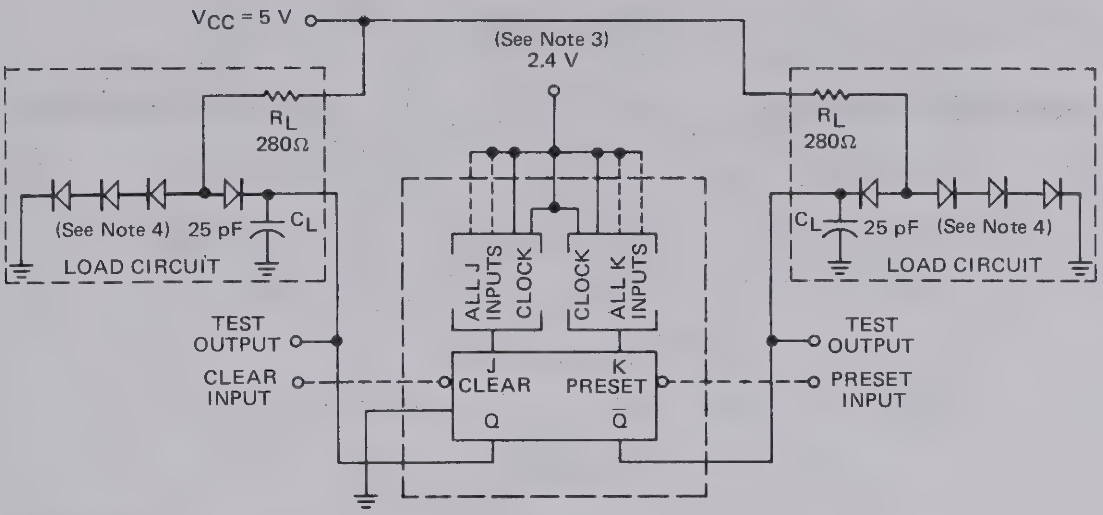
4 See applicable circuit type for actual J and K input configuration and presence of preset or clear functions.

5 C_L includes probe and jig capacitance.

Fig. W FLIP-FLOP PROPAGATION DELAY TIMES

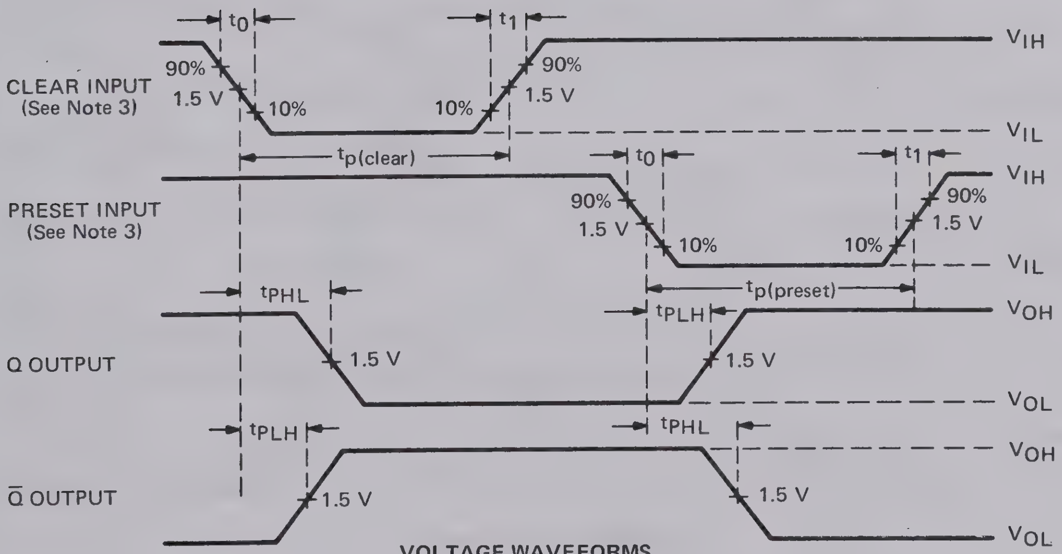
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



V_{CC} = 5 V
(See Note 3)
2.4 V
R_L
280Ω
R_L
280Ω
(See Note 4)
25 pF
C_L
C_L
25 pF
(See Note 4)
LOAD CIRCUIT
LOAD CIRCUIT
ALL J INPUTS
CLOCK
CLOCK
ALL K INPUTS
TEST OUTPUT
CLEAR INPUT
J
CLEAR
K
PRESET
Q
$\overline{Q}$
TEST OUTPUT
PRESET INPUT

TEST CIRCUIT



CLEAR INPUT
(See Note 3)
t_0
t_1
90%
1.5 V
10%
10%
90%
1.5 V
V_{IH}
V_{IL}
$t_{p(clear)}$
t_0
t_1
PRESET INPUT
(See Note 3)
90%
1.5 V
10%
10%
90%
1.5 V
V_{IH}
V_{IL}
$t_{p(preset)}$
t_{PHL}
t_{PLH}
Q OUTPUT
1.5 V
1.5 V
V_{OH}
V_{OL}
t_{PLH}
t_{PHL}
$\overline{Q}$ OUTPUT
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS

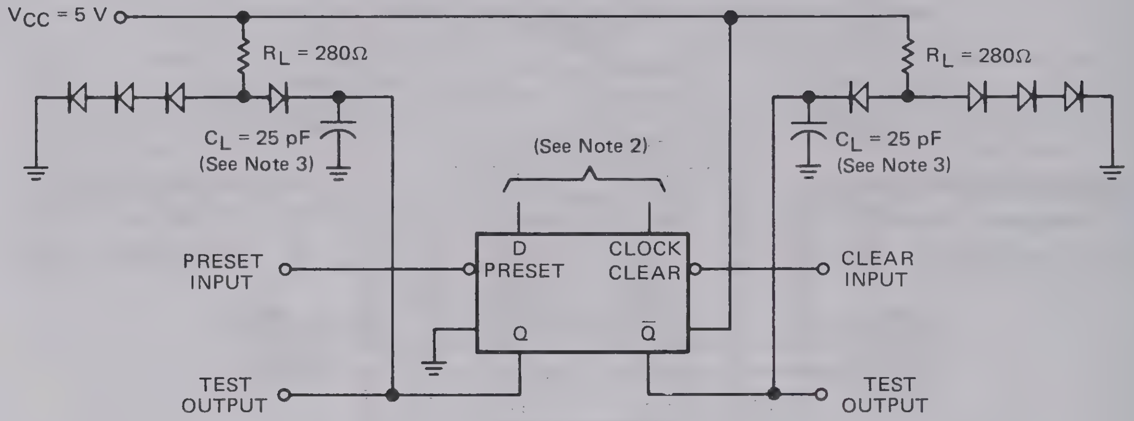
NOTES:

1 Clear or Preset inputs dominate regardless of the state of Clock or J-K inputs.
2 Clear or Preset input pulse characteristics: $V_{IH} = 3$ V, $V_{IL} = 0$ V, $t_1 = t_0 = 7$ ns, $t_{p(clear)} = t_{p(preset)} = 16$ ns, and PRR = 1 MHz.
3 See applicable circuit type for actual J and K input configuration and presence of Preset or Clear functions.
4 C_L includes probe and jig capacitance.

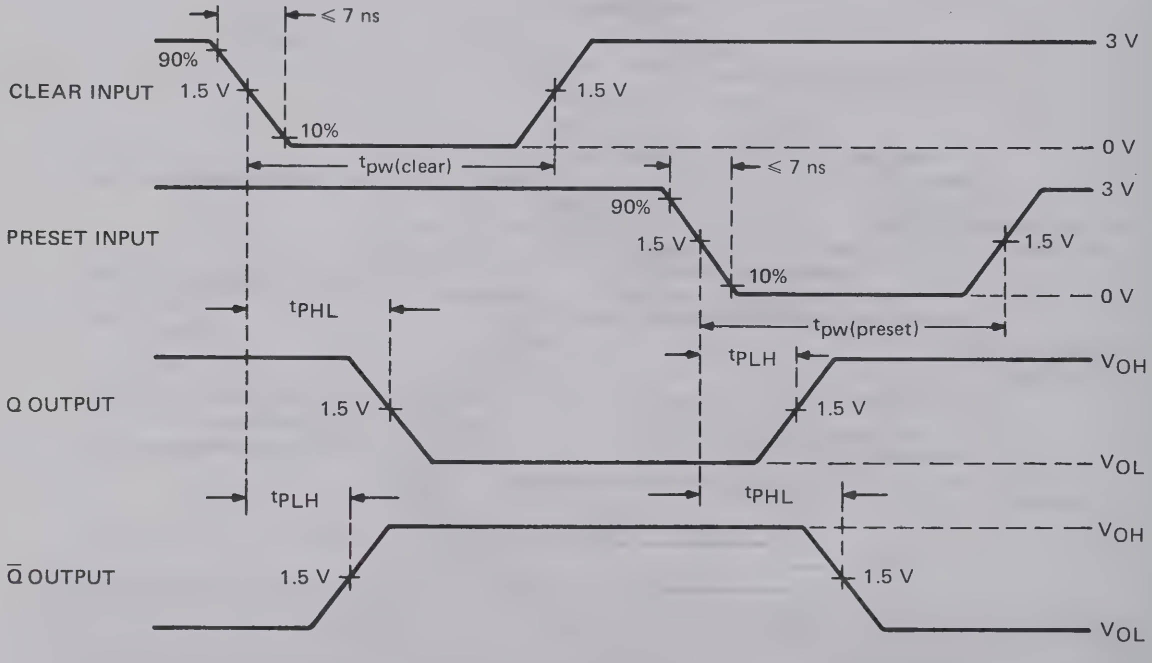
Fig. X FLIP-FLOP PRESET/CLEAR PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


VCC = 5 V
RL = 280Ω
CL = 25 pF
(See Note 3)
(See Note 2)
D
CLOCK
PRESET
CLEAR
Q
Q̄
PRESET INPUT
CLEAR INPUT
TEST OUTPUT
RL = 280Ω
CL = 25 pF
(See Note 3)
TEST OUTPUT

TEST CIRCUIT


≤ 7 ns
3 V
90%
CLEAR INPUT
1.5 V
1.5 V
10%
0 V
tpw(clear)
≤ 7 ns
3 V
90%
PRESET INPUT
1.5 V
1.5 V
10%
0 V
tpw(preset)
tPHL
tPLH
VOH
Q OUTPUT
1.5 V
1.5 V
VOL
tPLH
tPHL
VOH
Q̄ OUTPUT
1.5 V
1.5 V
VOL

VOLTAGE WAVEFORMS

NOTES:

1 Clear or Preset input pulse characteristics: $t_{pw(clear)} = t_{pw(preset)} = 25$ ns, PRR = 1 MHz.

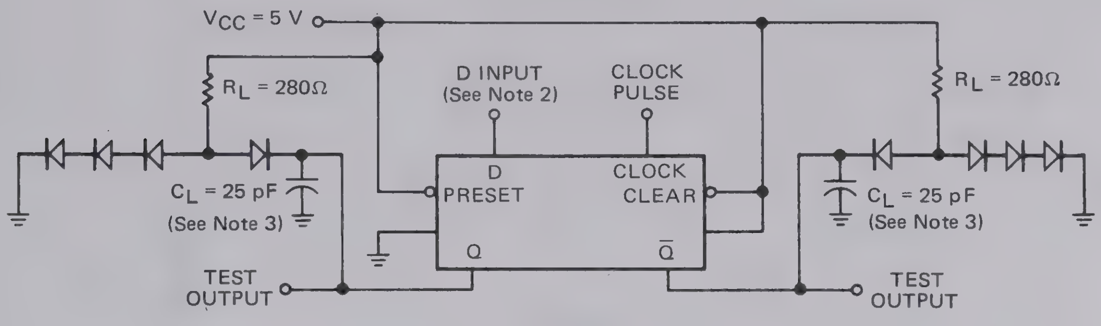
2 Clear and Preset inputs dominate regardless of the state of Clock or D inputs.

3 C_L includes probe and jig capacitance.

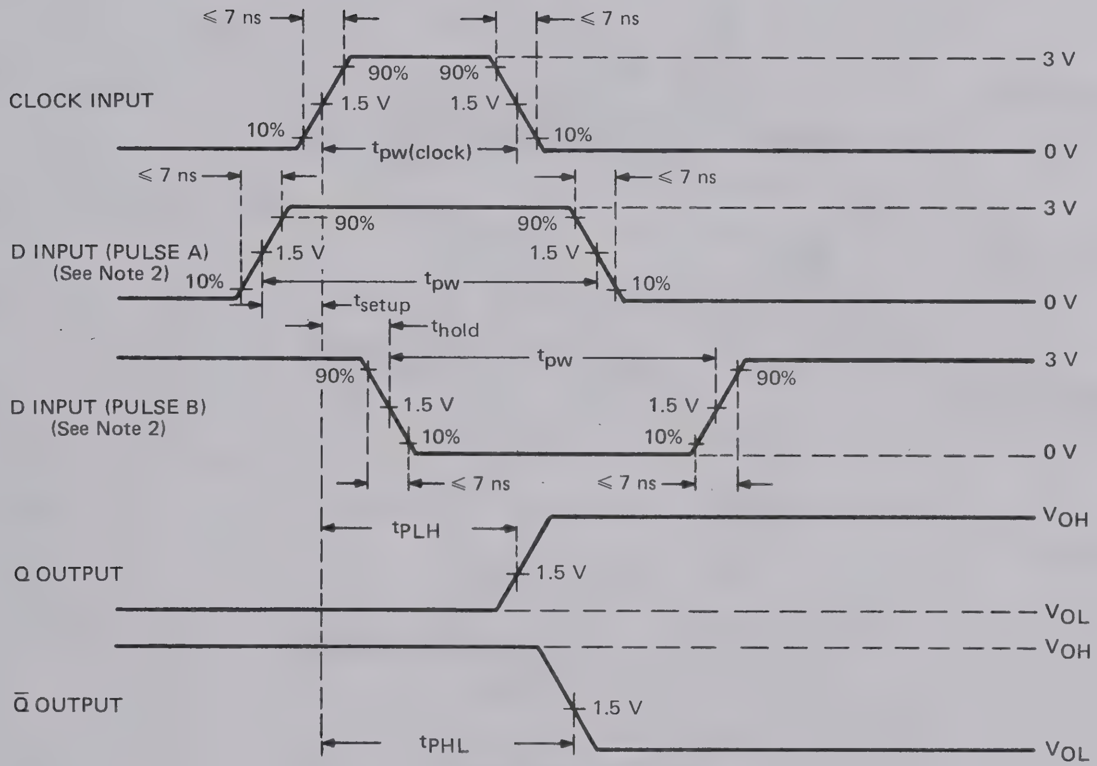
Fig. Y ASYNCHRONOUS INPUTS SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)


VCC = 5 V
RL = 280Ω
D INPUT (See Note 2)
CLOCK PULSE
RL = 280Ω
D
CLOCK
PRESET
CLEAR
Q
Q̄
CL = 25 pF (See Note 3)
CL = 25 pF (See Note 3)
TEST OUTPUT
TEST OUTPUT

TEST CIRCUIT


≤ 7 ns
≤ 7 ns
3 V
CLOCK INPUT
90%
90%
1.5 V
1.5 V
10%
10%
tpw(clock)
0 V
≤ 7 ns
≤ 7 ns
3 V
90%
90%
D INPUT (PULSE A) (See Note 2)
1.5 V
1.5 V
10%
tpw
10%
0 V
tsetup
thold
tpw
3 V
90%
90%
D INPUT (PULSE B) (See Note 2)
1.5 V
1.5 V
10%
10%
0 V
≤ 7 ns
≤ 7 ns
tPLH
VOH
Q OUTPUT
1.5 V
VOL
VOH
Q̄ OUTPUT
1.5 V
tPHL
VOL

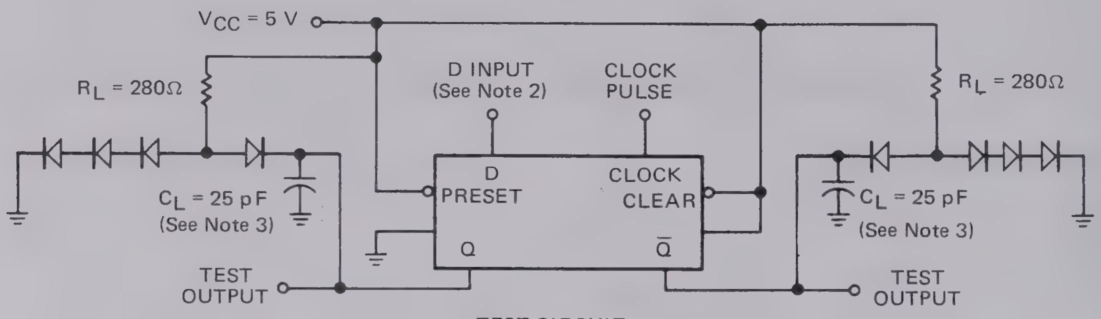
VOLTAGE WAVEFORMS

NOTES:
1 Clock input pulse has the following characteristics: $t_{pw(clock)}$ = 20 ns and PRR = 1 MHz. When testing f_{clock}, vary PRR.
2 D input (pulse A) has the following characteristics: t_{setup} = 10 ns, t_{pw} = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_{pw} = 60 ns, and PRR is 50% of the clock PRR.
3 C_L includes probe and jig capacitance.

Fig. Z SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (HIGH-LEVEL DATA)

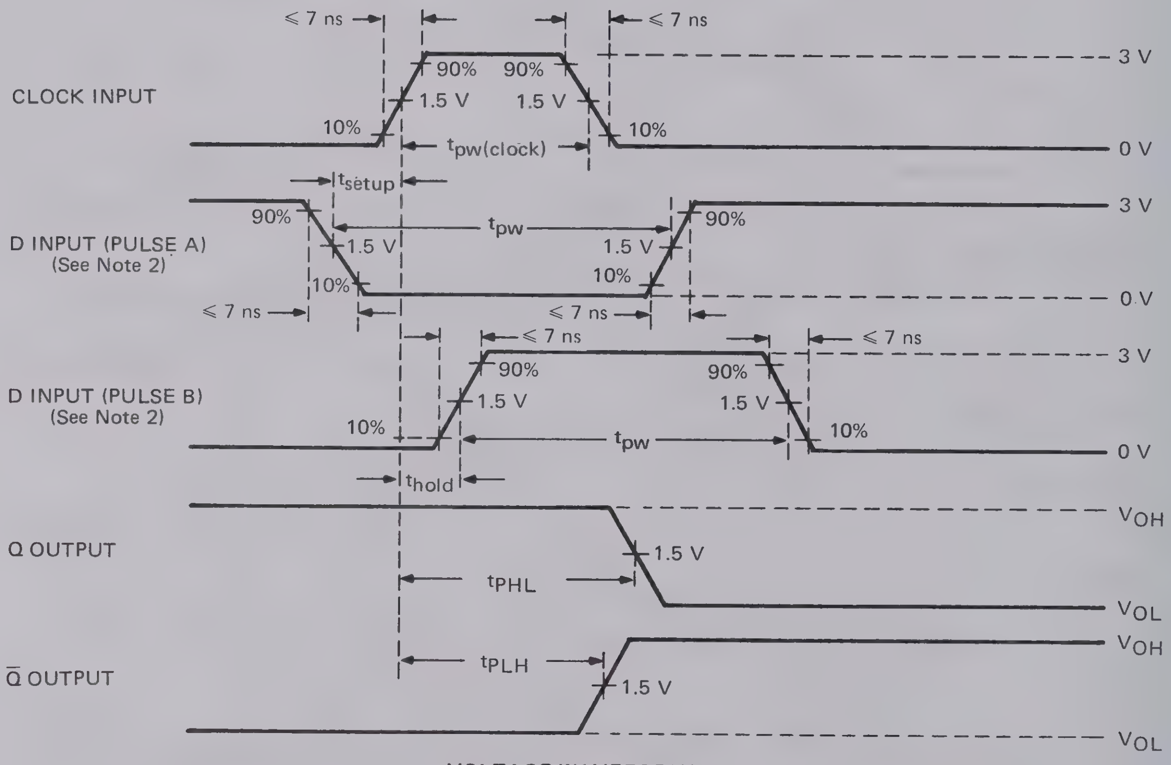
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



V_CC = 5 V
R_L = 280Ω
D INPUT
(See Note 2)
CLOCK
PULSE
D
PRESET
CLOCK
CLEAR
Q
Q̄
R_L = 280Ω
C_L = 25 pF
(See Note 3)
C_L = 25 pF
(See Note 3)
TEST
OUTPUT
TEST
OUTPUT

TEST CIRCUIT



≤ 7 ns
≤ 7 ns
3 V
CLOCK INPUT
90%
90%
1.5 V
1.5 V
10%
10%
t_pw(clock)
0 V
t_setup
3 V
90%
t_pw
90%
D INPUT (PULSE A)
(See Note 2)
1.5 V
1.5 V
10%
10%
0 V
≤ 7 ns
≤ 7 ns
≤ 7 ns
≤ 7 ns
3 V
90%
90%
D INPUT (PULSE B)
(See Note 2)
1.5 V
1.5 V
10%
t_pw
10%
0 V
t_hold
V_OH
Q OUTPUT
1.5 V
t_PHL
V_OL
V_OH
t_PLH
Q̄ OUTPUT
1.5 V
V_OL

VOLTAGE WAVEFORMS

NOTES:

1 Clock input pulse has the following characteristics: t_{pw} = 20 ns and PRR = 1 MHz. When testing f_{clock}, vary PRR.

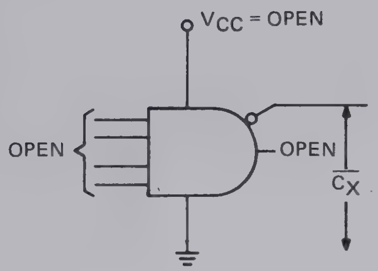
2 D input (pulse A) has the following characteristics: t_{setup} = 15 ns, t_{pw} = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_{pw} = 60 ns, and PRR is 50% of the clock PRR.

3 C_L includes probe and jig capacitance.

Fig. AA SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (LOW-LEVEL DATA)

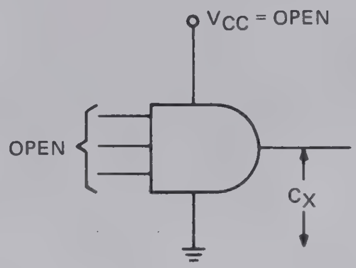
PARAMETER MEASUREMENT INFORMATION

SWITCHING TIME DATA TEST CIRCUITS


VCC = OPEN
OPEN
OPEN
CX

1. Each output is tested separately.

Fig. BB

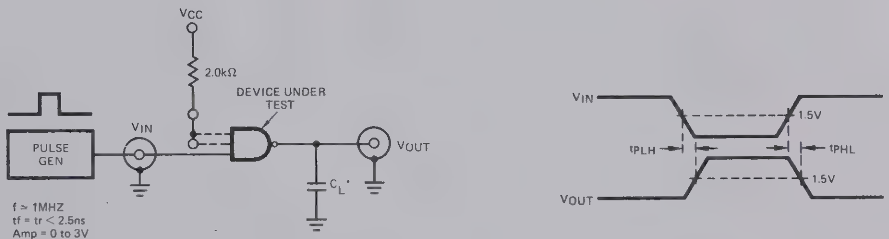

VCC = OPEN
OPEN
CX

1. Each output is tested separately.

Fig. CC

SWITCHING CHARACTERISTICS

TEST CIRCUIT AND WAVEFORM FOR 9S00, 9S04, 9S20, 9S40 AND 9S140

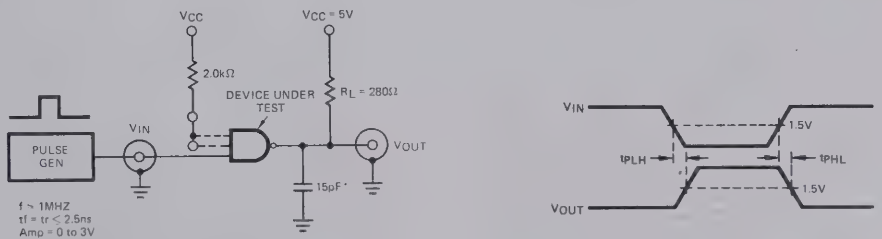

VCC
2.0kΩ
DEVICE UNDER TEST
PULSE GEN
VIN
VOUT
CL*
VIN
1.5V
tPLH
tPHL
1.5V
VOUT

f ≃ 1MHZ
tf = tr < 2.5ns
Amp = 0 to 3V
Duty Cycle = 50%
ZOUT = 50Ω

*Includes all probe and jig capacitance
15pF for 9S00, 9S04, 9S20.
50pF for 9S40, 9S140.

Fig. DD

TEST CIRCUIT AND WAVEFORM FOR 9S03, 9S05 AND 9S22


VCC
VCC = 5V
2.0kΩ
DEVICE UNDER TEST
RL = 280Ω
PULSE GEN
VIN
VOUT
15pF*
VIN
1.5V
tPLH
tPHL
1.5V
VOUT

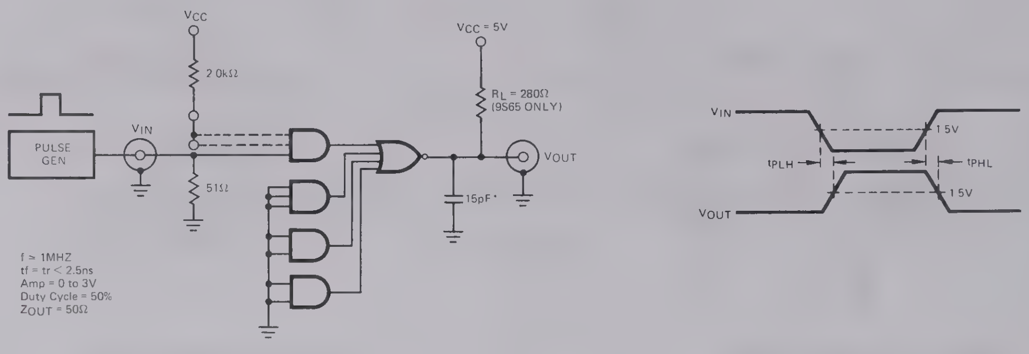
f ≃ 1MHZ
tf = tr < 2.5ns
Amp = 0 to 3V
Duty Cycle = 50%
ZOUT = 50Ω

*Includes all probe and jig capacitance

Fig. EE

SWITCHING CHARACTERISTICS (cont.)

TEST CIRCUIT AND WAVEFORM FOR 9S64, 9S65


VCC
2.0kΩ
PULSE GEN
VIN
51Ω
VCC = 5V
RL = 280Ω
(9S65 ONLY)
15pF*
VOUT
f ≃ 1MHZ
tf = tr < 2.5ns
Amp = 0 to 3V
Duty Cycle = 50%
ZOUT = 50Ω
VIN
1.5V
tPLH
tPHL
1.5V
VOUT

*Includes all probe and jig capacitance

Fig. FF

TYPICAL CHARACTERISTICS

ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE

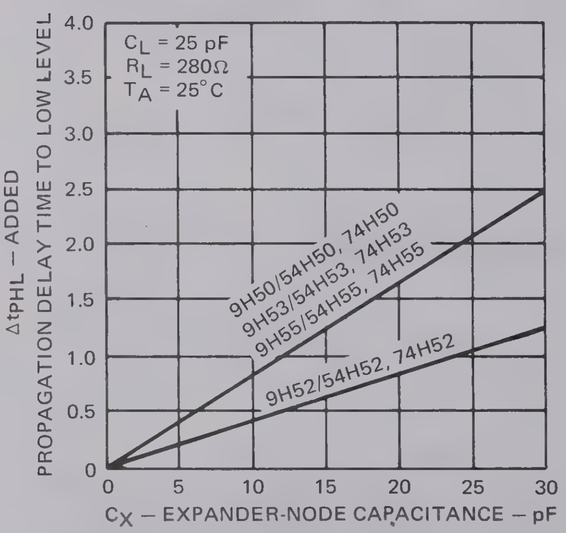


Fig. MM

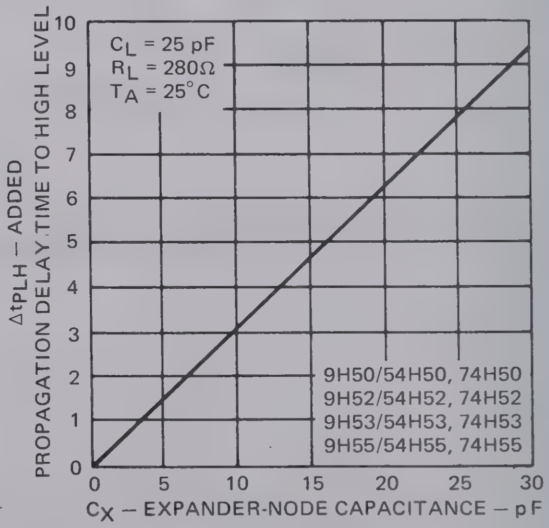
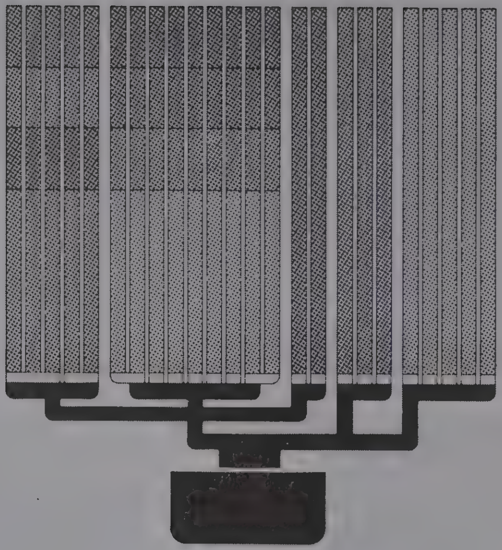


Fig. NN



SSI
Monostable Multivibrator and Interface Circuits 9600 Series Data Sheets

The 9600 TTL elements are Monostable Multivibrator and Interface functions compatible with all SSI and MSI devices.

Full data sheets are provided on the Monostable series. Complete data sheets on the Interface series may be obtained from:

Fairchild Semiconductor
P.O. Box 880 A
Mountain View, California
94040

Attn: Distribution Services

TTL/MONOSTABLE 9600

RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION — The TTL/Monostable 9600 Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9600 has excellent immunity to noise on the V_{CC} and ground lines. The 9600 uses TTL for high speed and high fanout capability and is compatible with all members of the Fairchild TTL family

- **74 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **RESETTABLE**
- **TTL INPUT GATING — LEADING OR TRAILING EDGE TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **IMPROVED PULSE WIDTH TEMPERATURE STABILITY**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

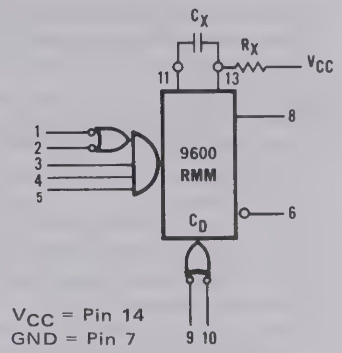
Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	-0.5 V to +8.0 V
Input Voltage (dc) (See Note 2)	-0.5 V to +5.5 V
Input Current (See Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output When Output is HIGH	-0.5 V to $+V_{CC}$ value
Current Into Output When Output is LOW	50 mA

NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a HIGH output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.

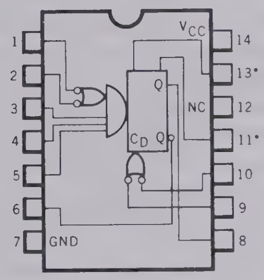
(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than –0.5 V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

LOGIC DIAGRAM

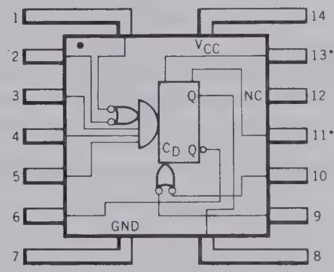


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



*Pins for connecting external timing components.

NC = No Internal Connection

FUNCTIONAL DESCRIPTION — The 9600 monostable multivibrator has five inputs, three active HIGH and two active LOW. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9600 and result in a continuous true output. (See Rule 8.) Retriggering may be inhibited by tying the negation ($\overline{Q}$) output to an active LOW input. The output pulse may be terminated at any time by connecting either or both reset pins to a LOW logic level pin. Active pullups are provided on the outputs for good drive capability into capacitive loads.

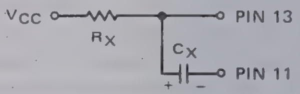
OPERATION RULES

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the logic diagram. The value of R_X may vary from 5.0 to 50 kΩ for 0 to +75°C operation and from 5.0 to 25 kΩ for −55 to +125°C operation. C_X may vary from 0 to any necessary value available.
2. The following are recommended fixed values of R_X: R_X = 30 kΩ for 0 to +75°C operation, R_X = 10 kΩ for −55 to +125°C operation.
3. The output pulse width (t) is defined as follows:

   $t = 0.32\ R_X C_X\ [1 + \frac{0.7}{R_X}]$ Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF, see Fig. 14.

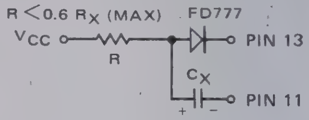
   The value of C_X may vary from 0 to any value necessary and obtainable. If however, C_X has leakage currents approaching 3 μA or if stray capacitance from either pin 11 or pin 13 to ground exceeds 50 pF, the timing equation may not represent the pulse width obtained.

4. If electrolytic type capacitors are to be used, the following three configurations are recommended.



   A. Use with low leakage electrolytic capacitors.

   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volts is less than 5 μA over the operational temperature range and Rule 3 above is satisfied.

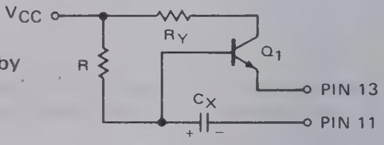


   B. Use with high inverse leakage current electrolytic capacitors.

   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.

   $t \approx 0.3\ RC_X$

   The use of this configuration is not recommended with retriggerable operation.



   C. Use to obtain extended pulse widths.

   This configuration obtains extended pulse widths because of the larger timing resistor allowed by Beta multiplication.

   Electrolytics with high inverse leakage currents can be used.

   $R < R_X\ (0.7)\ (h_{FE}Q_1)$ or < 2.5 MΩ, whichever is less

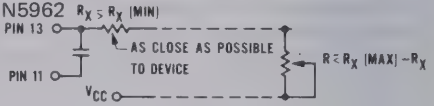
   $R_X(\text{min}) < R_Y < R_X(\text{max})$ R_Y of 5 to 10kΩ is recommended.

   Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

   $t \approx 0.3\ RC_X$

   The use of this configuration is not recommended with retriggerable operation.

5. This circuit is recommended to obtain variable pulse width by remote trimming.

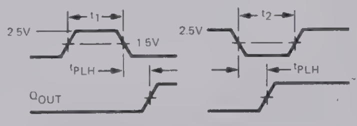


6. Under any operating condition, C_X and R_X(min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules (see Triggering Truth Table, after Fig. 15).

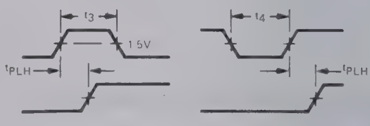
   Input to pin 1 or 2. Pins 2 or 1,3,4,5, 9,10 = HIGH.

   t_1, t_3 = Min. positive input pulse width > 40 ns.

   t_2, t_4 = Min. negative input pulse width > 40 ns.

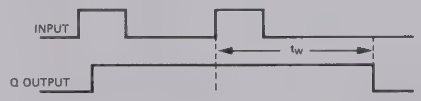


Input to Pin 3, 4 or 5
Other Inputs = HIGH
Pins 1 or 2 = LOW
Pins 9, 10 = HIGH



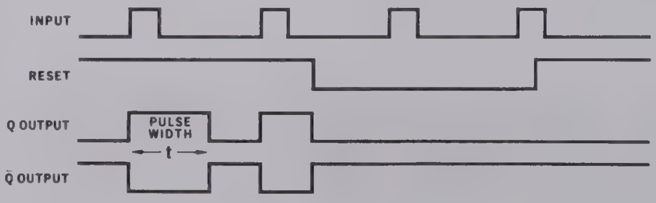
8. The retrigger pulse width is equal to the pulse width t plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t.

   $t_W = t + t_{PLH} = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X}) + t_{PLH}$



NOTE: Retriggering will not occur if the retrigger pulse comes within ≈0.3 C_X ns after the initial trigger pulse (i.e., during the discharge cycle time).

9. Two overriding active LOW resets are provided. A LOW to either or both resets can terminate any timing cycle and/or inhibit any new cycle until both reset inputs are restored to a HIGH. Trigger inputs will not produce spikes in the output when either or both resets are held LOW.



10. Use of a 0.01 to 0.1 μF bypass capacitor located close to the 9600 is recommended.

TABLE I – ELECTRICAL CHARACTERISTICS (T_A = –55°C to 125°C, V_{CC} = 5 V ±10%) (Part No. 9600XM)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS
		–55°C		+25°C			+125°C			
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		(Note 1)
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 9.92 mA (Note 2) V_{CC} = 5.5 V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	2.0		1.7			1.5		Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.90		0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current		–1.6		–1.1	–1.6		–1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
			–1.24		–0.97	–1.24		–1.24	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current				15	60		60	µA	V_{CC} = 5.5 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current					–25			mA	V_{CC} = 5.5 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}	Quiescent Power Supply Drain		24		19	24		24	mA	V_{CC} = 5.0 V, Gnd Pins 1 & 2
t_{PLH}	Negative Trigger Input to True Output				29	45			ns	V_{CC} = 5.0 V R_X = 5.0 Ω C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				29	40			ns	V_{CC} = 5.0 V R_X = 5.0 Ω C_X = 0, C_L = 15 pF
$t_{(min)}$	Minimum True Output Pulse Width				74	100			ns	V_{CC} = 5.0 V R_X = 5.0 Ω C_X = 0, C_L = 15 pF
	Minimum Complement Output Pulse Width					112			ns	
t	Pulse Width			3.20	3.42	3.76			µs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

TABLE II – ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ±5%) (Part No. 9600XC)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS
		0°C		+25°C			75°C			
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		(Note 1)
V_{OH}	Output HIGH Voltage	2.4		2.4	3.4		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 11.3 mA (Note 2) V_{CC} = 5.25 V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	1.9		1.8			1.65		Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current		–1.6		–1.0	–1.6		–1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
			–1.41			–1.41		–1.41	mA	V_{CC} = 4.75 V, V_{IN} = 0.45 V
I_{IH}	Input HIGH Current				15	60		60	µA	V_{CC} = 5.25 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current					–35			mA	V_{CC} = 5.25 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}	Quiescent Power Supply		26		19	26		26	mA	V_{CC} = 5.0 V Ground Pins 1 and 2
t_{PLH}	Negative Trigger Input to True Output				29	56			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				29	47			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t(min)	Minimum True Output Pulse Width				74	120			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
	Minimum Complement Output Pulse Width					130			ns	
t	Pulse Width			3.08	3.42	3.76			µs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:

(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)

(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8.
Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.

TYPICAL ELECTRICAL CHARACTERISTICS

Fig. 1

INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

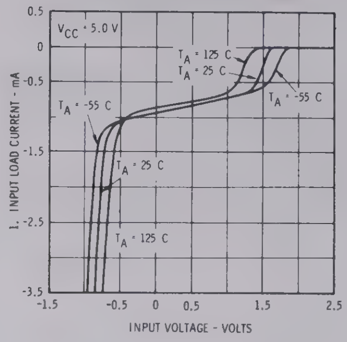


Fig. 2

INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE

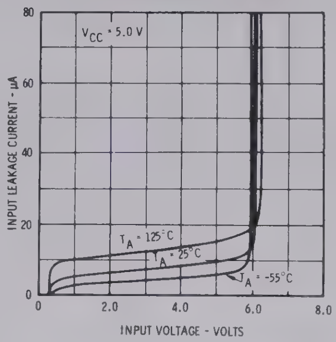


Fig. 3

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

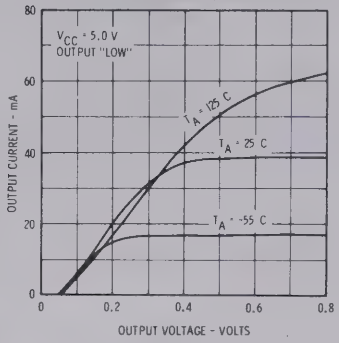


Fig. 4

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)

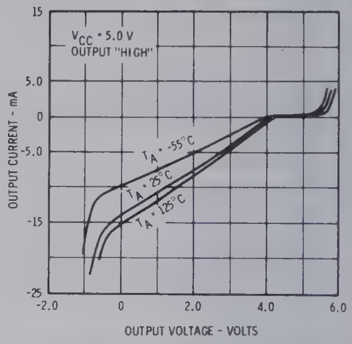


Fig. 5

MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (POSITIVE EDGE TRIGGER INPUT)

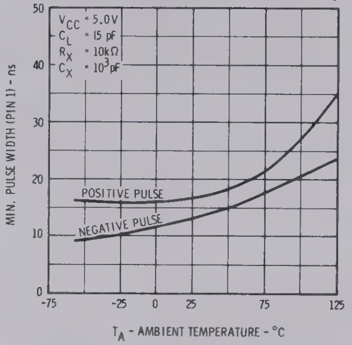


Fig. 6

MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (NEGATIVE EDGE TRIGGER INPUT)

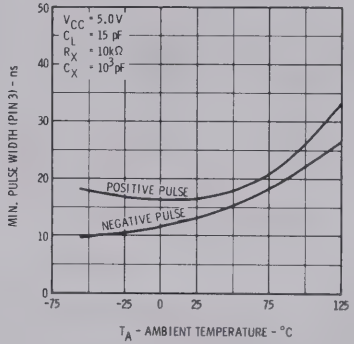


Fig. 7

MINIMUM TIME DELAY, RESET TO OUTPUT VERSUS AMBIENT TEMPERATURE

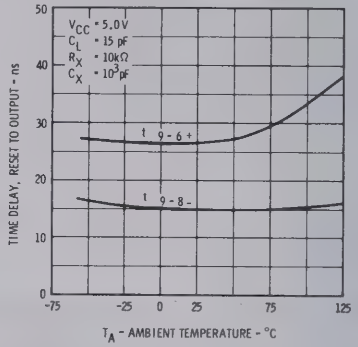


Fig. 8

NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

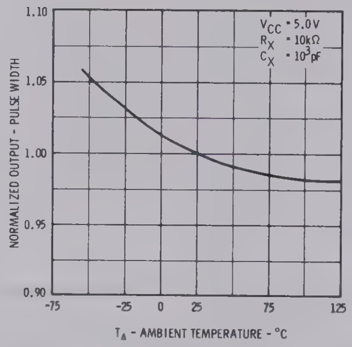


Fig. 9

PULSE WIDTH VERSUS TIMING RESISTOR

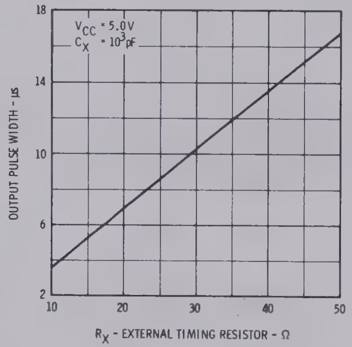


Fig. 10

POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

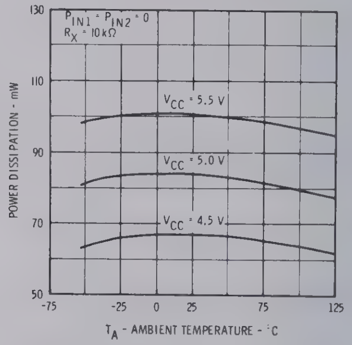


Fig. 11

NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

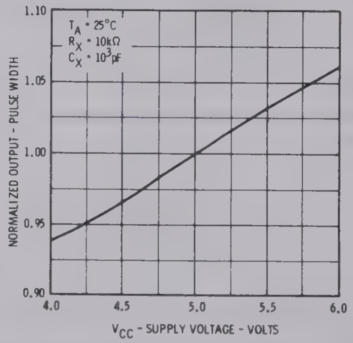


Fig. 12

MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

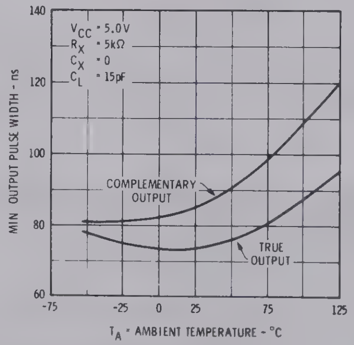
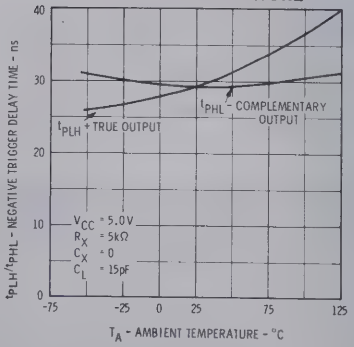


Fig. 13

NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

$[\text{For } C_X \geqslant 10^3 \text{ pF, } t = 0.32\, R_X C_X \, (1 + \frac{0.7}{R_X})]$

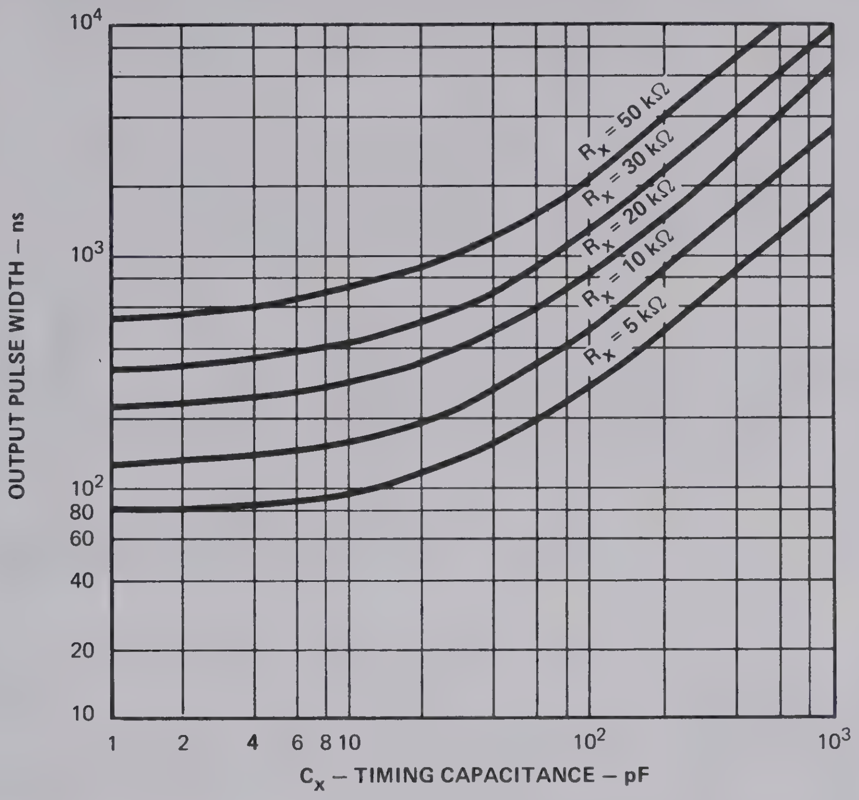
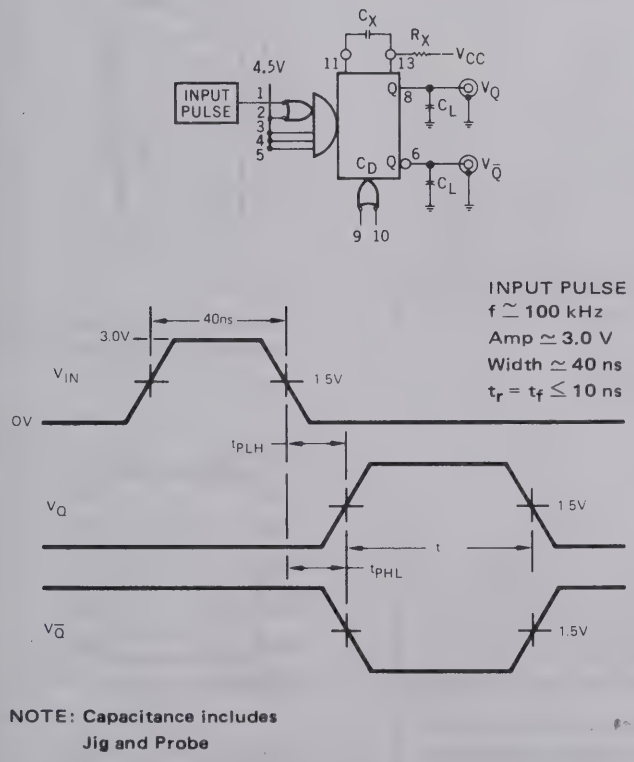


Fig. 14

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS


C_X
R_X
V_{CC}
4.5V
11
13
INPUT PULSE
1
2
3
4
5
Q
8
C_L
V_Q
C_D
$\bar{Q}$
6
C_L
$V_{\bar{Q}}$
9
10
40ns
3.0V
V_{IN}
1.5V
0V
t_{PLH}
V_Q
1.5V
t
t_{PHL}
$V_{\bar{Q}}$
1.5V

INPUT PULSE
f $\simeq$ 100 kHz
Amp $\simeq$ 3.0 V
Width $\simeq$ 40 ns
$t_r = t_f \leq 10$ ns

NOTE: Capacitance includes Jig and Probe

Fig. 15

LOADING RULES

TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD	
	HIGH	LOW
1,2,3,4,5,9,10	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6,8	16 U.L.	8 U.L.

Note: 1 Unit Load (U.L.) = 60 μA HIGH/1.6 mA LOW.

TRIGGERING TRUTH TABLE

(PIN NO'S.) 1	2	3	4	5	9	10	OPERATION
H→L	H	H	H	H	H	H	Trigger
H	H→L	H	H	H	H	H	Trigger
L	X	L→H	H	H	H	H	Trigger
X	L	L→H	H	H	H	H	Trigger
L	X	H	L→H	H	H	H	Trigger
X	L	H	L→H	H	H	H	Trigger
L	X	H	H	L→H	H	H	Trigger
X	L	H	H	L→H	H	H	Trigger
X	X	X	X	X	L	X	Reset
X	X	X	X	X	X	L	Reset

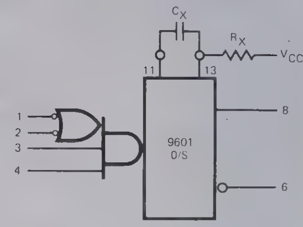
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = Transition from HIGH to LOW Voltage level
L→H = Transition from LOW to HIGH Voltage level

TTL/MONOSTABLE 9601

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The TTL/Monostable 9601 Retriggerable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9601 has excellent immunity to noise on the V_{CC} and ground lines. The 9601 uses TTL for high speed and high fanout capability and is compatible with all members of the Fairchild TTL family.

LOGIC DIAGRAM

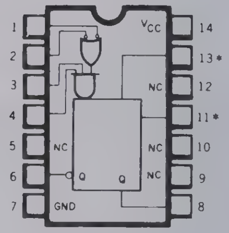


V_{CC} = Pin 14
GND = Pin 7

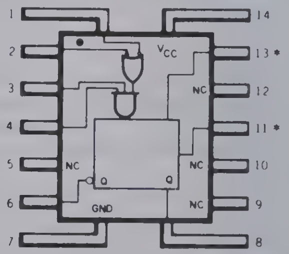
FEATURES:

- 50 ns TO ∞ OUTPUT PULSE WIDTH RANGE
- RETRIGGERABLE 0 TO 100% DUTY CYCLE
- TTL INPUT GATING – LEADING OR TRAILING EDGE TRIGGERING
- COMPLEMENTARY TTL OUTPUTS
- OPTIONAL RETRIGGER LOCK-OUT CAPABILITY
- PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



*Pins for External Timing
NC – No Internal Connection

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (dc) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is HIGH	−0.5 V to +V_{CC} value
Current Into Output When Output is LOW	50 mA

NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a HIGH output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

FUNCTIONAL DESCRIPTION

The 9601 monostable multivibrator has four inputs, two active HIGH and two active LOW. This allows a choice of leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9601 and result in a continuous true output. (See Rule 9.) Retriggering may be inhibited by tying the negation (Q) output to an active LOW input. Active pullups are provided on the outputs for good drive capability into capacitive loads.

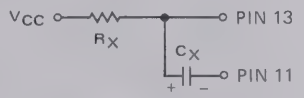
OPERATION RULES

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 to 50 kΩ for 0 to 75°C operation and from 5.0 to 25 kΩ for –55 to +125°C operation.
3. C_X may vary from 0 to any necessary value available. If however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:

$$t = 0.32\, R_X C_X \left[1 + \frac{0.7}{R_X}\right]$$

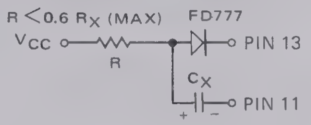
Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF, see Fig. 12.

5. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   A. For use with low leakage electrolytic capacitors.
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range, and Rule 3 above is satisfied.



   B. Use with high inverse leakage current electrolytic capacitors.
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.

$$t \approx 0.3\, RC_X$$



   C. Use to obtain extended pulse widths:
   This configuration obtains extended pulse widths, because of the larger timing resistor allowed by Beta multiplication. Electrolytics with high (>5 μA) inverse leakage currents can be used.

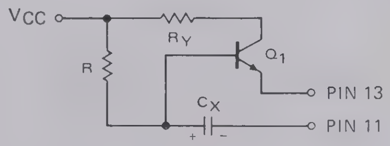
   $R < R_X\ (0.7)\ (h_{FE}\ Q_1)$ or < 2.5 MΩ whichever is lesser

   $R_X\ (\text{min}) < R_Y < R_X\ (\text{max})$ ($5 \leqslant R_Y \leqslant 10$ kΩ is recommended)

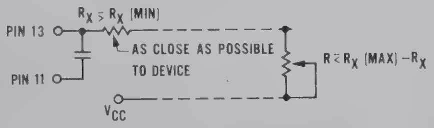
   Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

   $t \approx 0.3\, RC_X$

   Configuration B and C are not recommended with retriggerable operation.

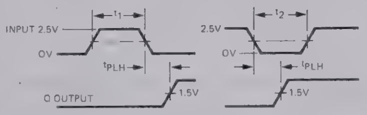


6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

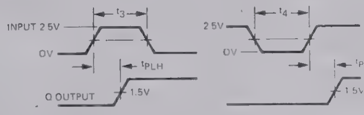


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. (See Triggering Truth Table on page 5.)

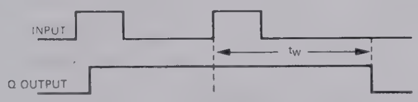
Input to Pin 1 (2)
Pins 2, (1), 3 & 4 = HIGH
t_1, t_4 = Setup time > 40 ns
t_2, t_3 = Release time > 40 ns



Input to Pin 3 (4)
Pin 4 (3) = HIGH
Pins 1 or 2 = LOW



9. The retrigger pulse width is calculated as shown below:



$$t_W = t + t_{PLH} = 0.32\, R_X C_X \left(1 + \frac{0.7}{R_X}\right) + t_{PLH}$$

The retrigger pulse width is equal to the pulse width t plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t.

NOTE: Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle time.)

10. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located close to the 9601 is recommended.

TABLE I — ELECTRICAL CHARACTERISTICS (T_A = −55°C to 125°C, V_{CC} = 5 V ±10%) (Part No. 9601XM)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS (Note 1)
		−55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.72 mA (Note 2)
V_{OL}	Output LOW Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 10 mA (Note 2)
V_{IH}	Input HIGH Voltage (Note 3)	2.0		1.7			1.5		Volts	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage (Note 3)		0.85			0.90		0.85	Volts	Guaranteed Input LOW Threshold
I_{IL}	Input LOW Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V V_{IN} = 0.4 V
I_{IH}	Input HIGH Current				15	60		60	µA	V_{CC} = 5.5 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current			−10		−40			mA	V_{CC} = 5.0 V, V_{OUT} = 0 V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5.5 V, Ground Pins 1 and 2
t_{PLH}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				25	40			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t (min)	Minimum True Output Pulse Width				45	65			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t	Pulse Width			3.08	3.42	3.76			µs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

TABLE II — ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ±5%) (Part No. 9601XC)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS (Note 1)
		0°C		+25°C			+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.4		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 12.8 mA (Note 2)
V_{IH}	Input HIGH Voltage (Note 3)	1.9		1.8			1.6		Volts	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage (Note 3)		.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold
I_{IL}	Input LOW Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V V_{IN} = 0.45 V
I_{IH}	Input HIGH Current				15	60		60	µA	V_{CC} = 5.25 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current			−10		−40			mA	V_{CC} = 5.0 V, V_{OUT} = 0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5.25 V, Ground Pins 1 and 2
t_{PLH}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				25	40			ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0, C_L = 15 pF
t (min)	Minimum True Output Pulse Width				45	65			ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0, C_L = 15 pF
t	Pulse Width			3.08	3.42	3.76			µs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:

(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)

(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8. Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.

(3) Pulse Test to determine V_{IH} and V_{IL} (Min PW 40 ns).

TYPICAL ELECTRICAL CHARACTERISTICS

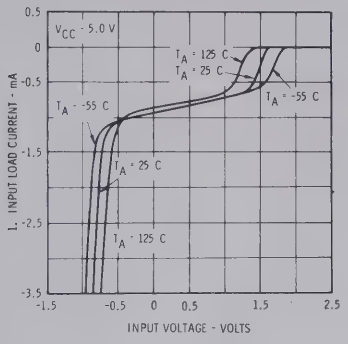


Fig. 1
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

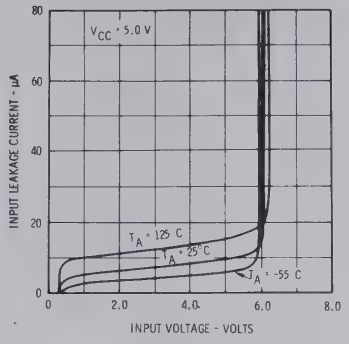


Fig. 2
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE

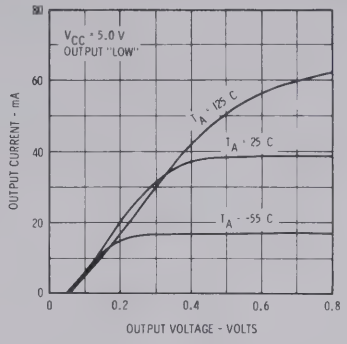


Fig. 3
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

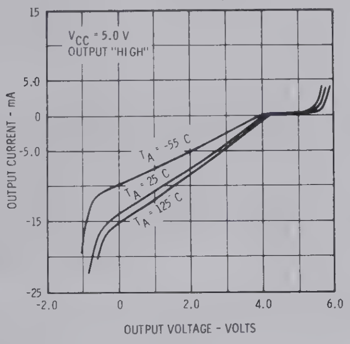


Fig. 4
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)

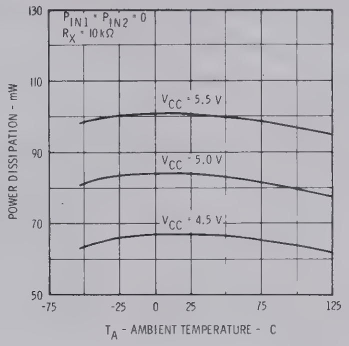


Fig. 5
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

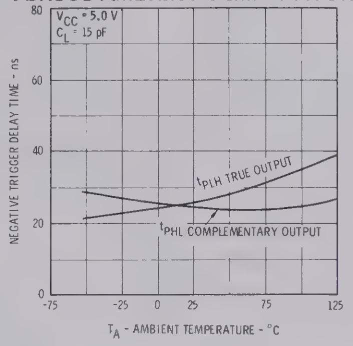


Fig. 6
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE

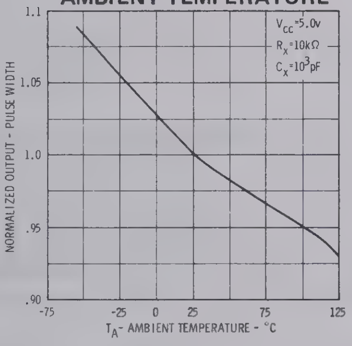


Fig. 7
NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

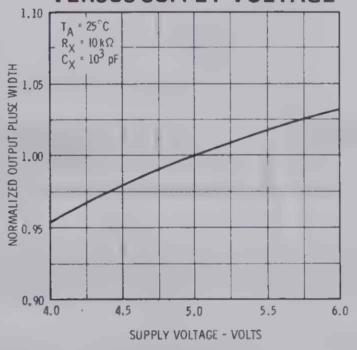


Fig. 8
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

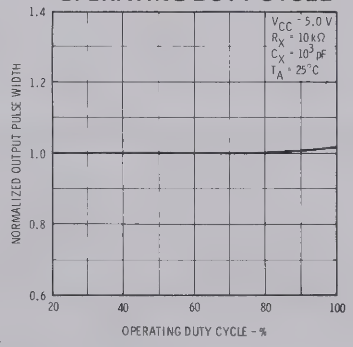


Fig. 9
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE

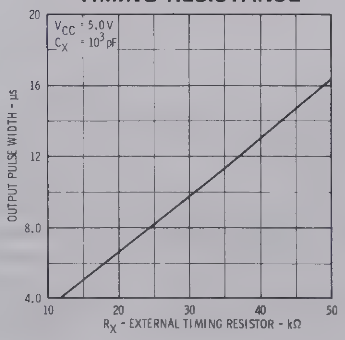


Fig. 10
PULSE WIDTH VERSUS TIMING RESISTANCE

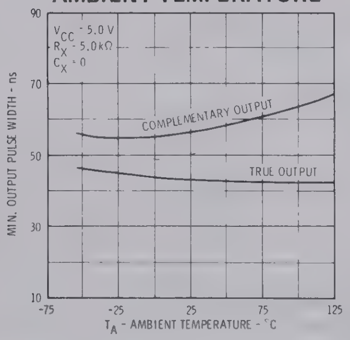


Fig. 11
OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

$$\left[\text{For } C_X \geq 10^3 \text{ pF, } t = 0.32\, R_X C_X \left(1 + \frac{0.7}{R_X}\right)\right]$$

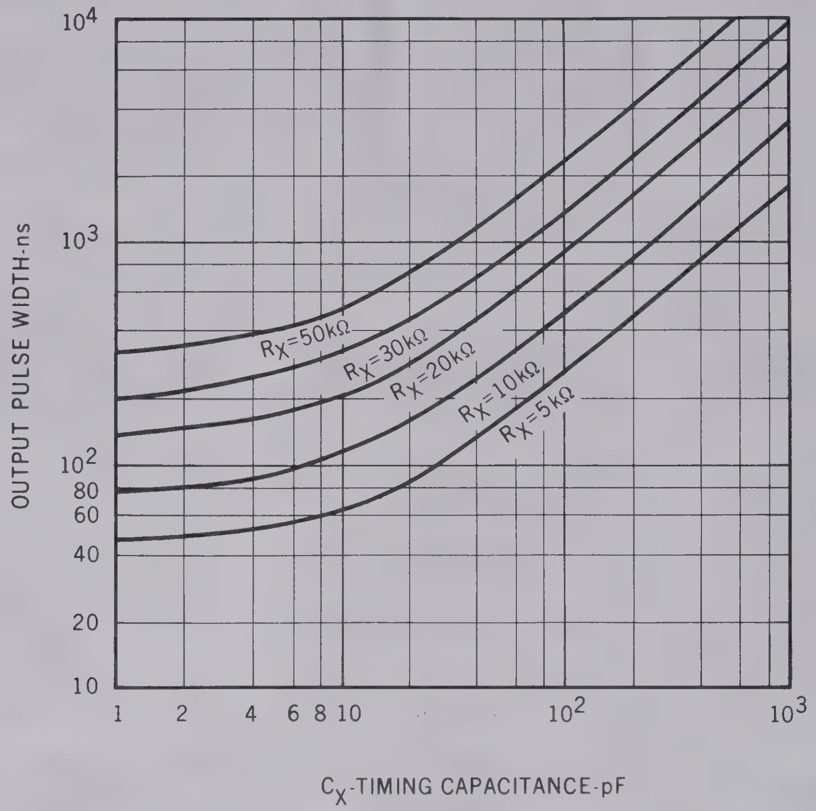
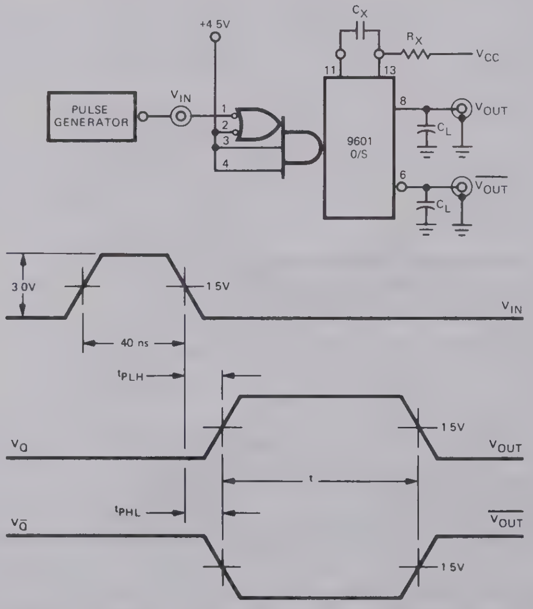


Fig. 12

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



+4.5V
C_X
R_X
V_CC
PULSE GENERATOR
V_IN
1
2
3
4
11
13
8
6
9601 O/S
V_OUT
C_L
V_OUT
C_L
3.0V
1.5V
V_IN
40 ns
t_PLH
V_Q
1.5V
V_OUT
t
t_PHL
V_Q̄
V_OUT
1.5V

NOTE: Capacitance includes Jig and Probe

LOADING RULES

TTL INPUT LOAD AND DRIVE FACTORS

–55°C to +125°C

INPUT LEVEL	LOAD FACTOR
HIGH	1
LOW	1
OUTPUT STATE	**DRIVE FACTOR**
HIGH	12
LOW	6

0°C to 75°C

INPUT LEVEL	LOAD FACTOR
HIGH	1
LOW	1
OUTPUT STATE	**DRIVE FACTOR**
HIGH	16
LOW	8

TRIGGERING TRUTH TABLE

Pin Number				Operation
1	2	3	4	
H→L	H	H	H	Trigger
H	H→L	H	H	Trigger
L	X	L→H	H	Trigger
X	L	L→H	H	Trigger
L	X	H	L→H	Trigger
X	L	H	L→H	Trigger

$T \text{ (trigger)} = (\overline{1} + \overline{2}) \cdot 3 \cdot 4$

Change of T from FALSE to TRUE causes trigger.

H = HIGH voltage level ⩾ V_{IH}
L = LOW voltage ⩽ V_{IL}
L→H = transition from LOW to HIGH voltage level
H→L = transition from HIGH to LOW voltage level
X = Don't care (either HIGH or LOW voltage level)

TTL/MONOSTABLE 9602

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION — The TTL/Monostable 9602 Dual Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9602 has excellent immunity to noise on the V_{CC} and ground lines. The 9602 uses TTL inputs and outputs for high speed and high fanout capability and is compatible with all members of the Fairchild TTL family.

- **72 ns TO ∞ OUTPUT WIDTH RANGE**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **TTL INPUT GATING — LEADING OR TRAILING EDGE TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

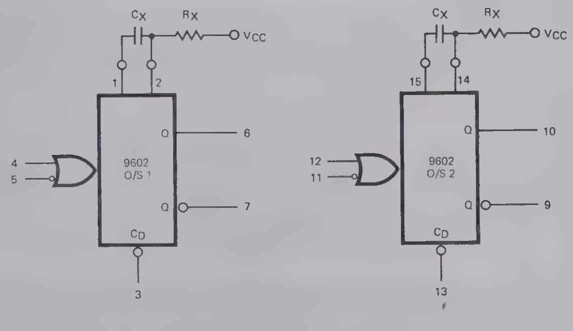
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (dc) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is HIGH	−0.5 V to $+V_{CC}$ value
Current Into Output When Output is LOW	50 mA

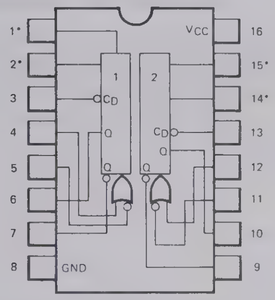
NOTES:

1. The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a HIGH output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.
2. Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

LOGIC DIAGRAM

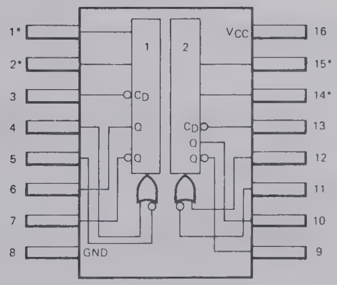


CONNECTION DIAGRAMS
DIP (TOP VIEW)



*Pins for external timing.

FLATPAK (TOP VIEW)



*Pins for external timing.

FUNCTIONAL DESCRIPTION — The 9602 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active LOW and one active HIGH. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9602 and result in a continuous true output. (See Rule 9) The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW. Active pullups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying $\overline{Q}$ output to an active level LOW input or the Q output to the active level HIGH input.

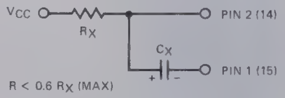
OPERATION RULES

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 kΩ to 50 kΩ for 0 to 75°C operation. The value of R_X may vary from 5.0 kΩ to 25 kΩ for −55 to +125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:

$$t = 0.31\, R_X C_X \left[1 + \frac{1}{R_X}\right]$$

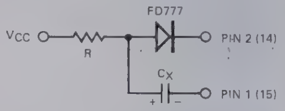
Where R_X is in kΩ, C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see Fig. 14

5. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3μA, and the inverse capacitor leakage at 1.0 volt is less than 5μA over the operational temperature range and Rule 3 above is satisfied.



   B. Use with high inverse leakage current electrolytic capacitors:
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

$$t \approx 0.3\ RC_X$$

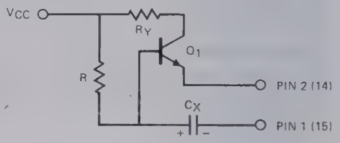


   C. Use to obtain extended pulse widths:
   This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

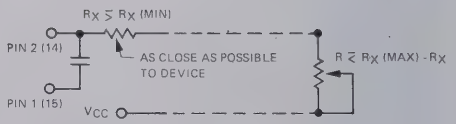
$R < R_X\,(0.7)\,(h_{FE}\,Q_1)$ or < 2.5 MΩ whichever is the lesser
$R_X\,(\text{min}) < R_Y < R_X\,(\text{max})$ ($5 \leq R_Y \leq 10$ kΩ is recommended)
Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$$t \approx 0.3\ RC_X$$

This configuration is not recommended with retriggerable operation.

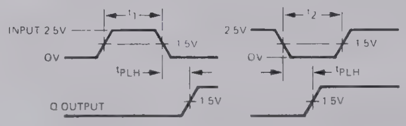


6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

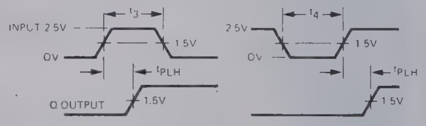


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. See Triggering Truth Table, following pages.

Input to Pin 5 (11)
Pin 4 (12) = LOW
Pin 3 (13) = HIGH
t_1, t_3 = Min. Positive Input Pulse Width > 40 ns
t_2, t_4 = Min. Negative Input Pulse Width > 40 ns

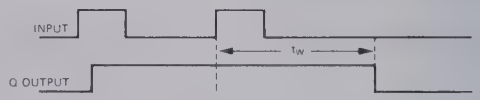


Input to Pin 4 (12)
Pin 5 (11) = HIGH
Pin 3 (13) = HIGH



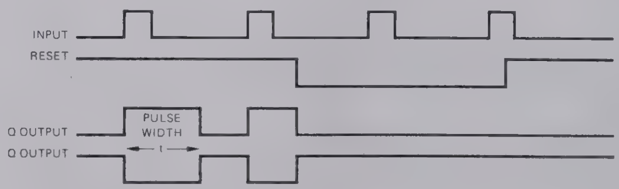
9. The retriggerable pulse width is calculated as shown below:

$$t_W = t + t_{PLH} = 0.31\ R_X\,C_X\,(1 + \frac{1}{R_X}) + t_{PLH}$$



The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as t.
Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle)

10. Reset Operation — An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one-shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the 9602 is recommended.

TABLE I – ELECTRICAL CHARACTERISTICS (T_A = –55°C to 125°C, V_{CC} = 5 V ± 10%) (Part No. 9602XM)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS (Note 1)
		–55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 9.92 mA (Note 2) V_{CC} = 5.5 V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	2.0		1.7			1.5		Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.90		0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current		–1.6		–1.1	–1.6		–1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
			–1.24		–0.97	–1.24		–1.24	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current				10	60		60	µA	V_{CC} = 5.5 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current					–25			mA	V_{CC} = 5.5 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}	Quiescent Power Supply Drain		45		39	45		45	mA	V_{CC} = 5.0 V
t_{PLH}	Negative Trigger Input to True Output				25	35			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				29	43			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
$t_{(min)}$	Minimum True Output Pulse Width				72	90			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
	Minimum Complement Output Pulse Width				78	100			ns	C_X = 0, C_L = 15 pF
t	Pulse Width			3.08	3.42	3.76			µs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pins 2 and 14)		50			50		50	pF	Pins 2 and 14 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

TABLE II – ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ±5%) (Part No. 9602XC)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS (Note 1)
		0°C		+25°C			+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.4		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 11.3 mA (Note 2) V_{CC} = 5.25 V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	1.9		1.8			1.65		Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current		–1.6		–1.0	–1.6		–1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
			–1.41			–1.41		–1.41	mA	V_{CC} = 4.75 V, V_{IN} = 0.45 V
I_{IH}	Input HIGH Current				10	60		60	µA	V_{CC} = 5.25 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current					–35			mA	V_{CC} = 5.25 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}	Quiescent Power Supply Drain		52		39	50		52	mA	V_{CC} = 5.0 V, Ground Pins 1 and 2
t_{PLH}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				29	48			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
$t_{(min)}$	Minimum True Output Pulse Width				72	100			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
	Minimum Complement Output Pulse Width				78	110			ns	C_X = 0, C_L = 15 pF
t	Pulse Width			3.08	3.42	3.76			µs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pins 2 and 14)		50			50		50	pF	Pins 2 and 14 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
1. Unless otherwise noted, 10 kΩ resistor placed between Pin 2 (14) and V_{CC}, for all tests. (R_X)
2. Ground Pin 1 (15) for V_{OL} on Pin 7 (9), or for V_{OH} on Pin 6 (10), or for I_{SC} on Pin 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for V_{OL} on Pin 6 (10), or for V_{OH} on Pin 7 (9), or for I_{SC} on Pin 7 (9).

TYPICAL ELECTRICAL CHARACTERISTICS

Fig. 1

INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

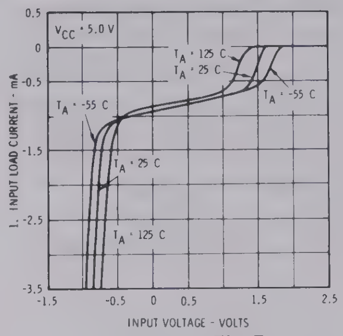


Fig. 2

INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE

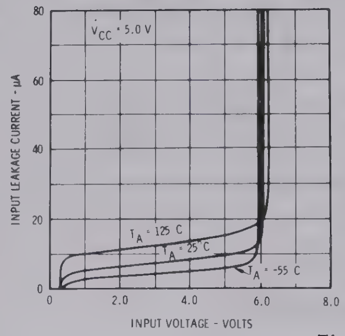


Fig. 3

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

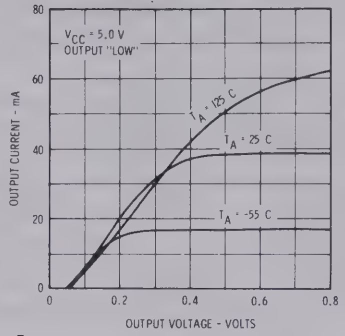


Fig. 4

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)

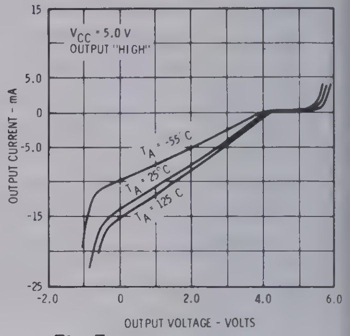


Fig. 5

MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (POSITIVE EDGE TRIGGER INPUT)

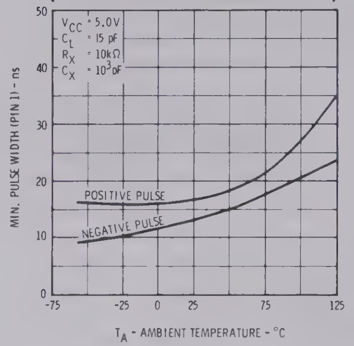


Fig. 6

MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (NEGATIVE EDGE TRIGGER INPUT)

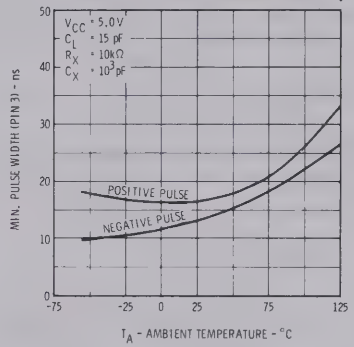


Fig. 7

MINIMUM TIME DELAY, RESET TO OUTPUT VERSUS AMBIENT TEMPERATURE

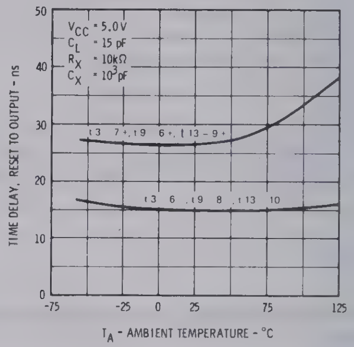


Fig. 8

NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

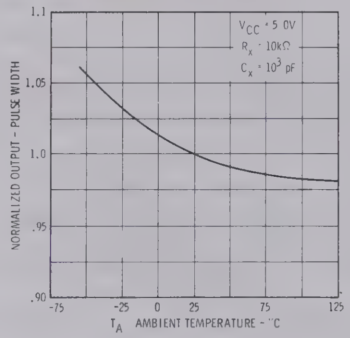


Fig. 9

PULSE WIDTH VERSUS TIMING RESISTOR

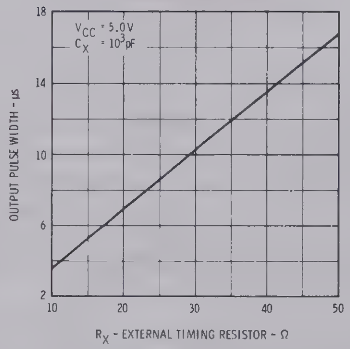


Fig. 10

POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

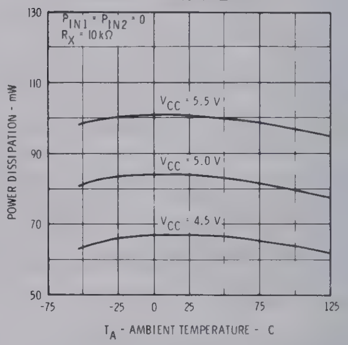


Fig. 11

NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

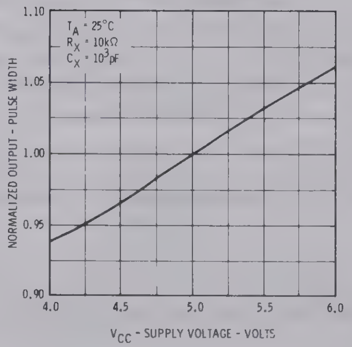


Fig. 12

MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

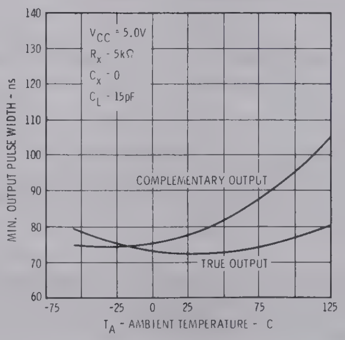
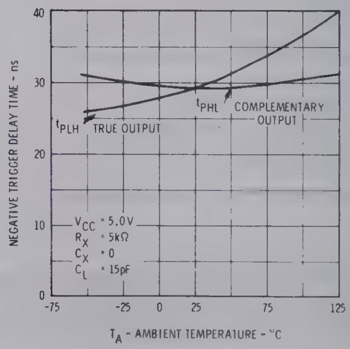


Fig. 13

NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_x < 10^3$ pF

For $C_x \geq 10^3$ pF, $t = 0.31\, R_x C_x \left(1 + \frac{1}{R_x}\right)$

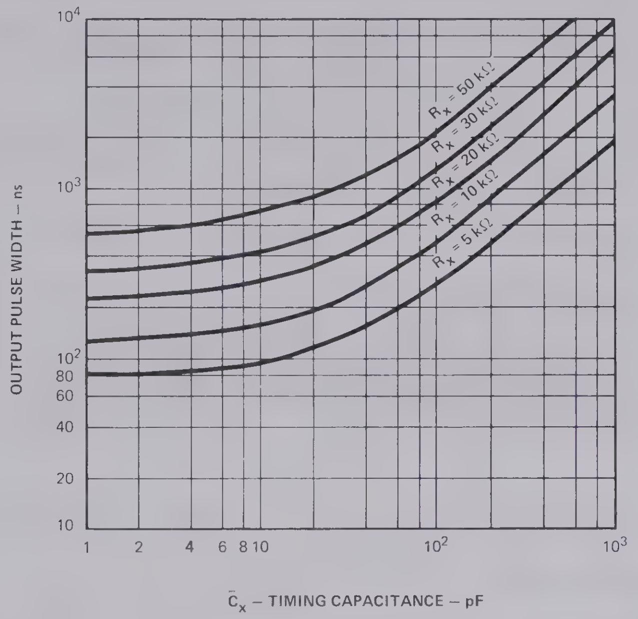


Fig. 14

LOADING RULES

TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD	
	HIGH	LOW
3, 4, 5, 11, 12, 13	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6, 7, 9, 10	16 U.L.	8 U.L.

1 Unit Load (U.L.) = 60μA HIGH/1.6mA LOW

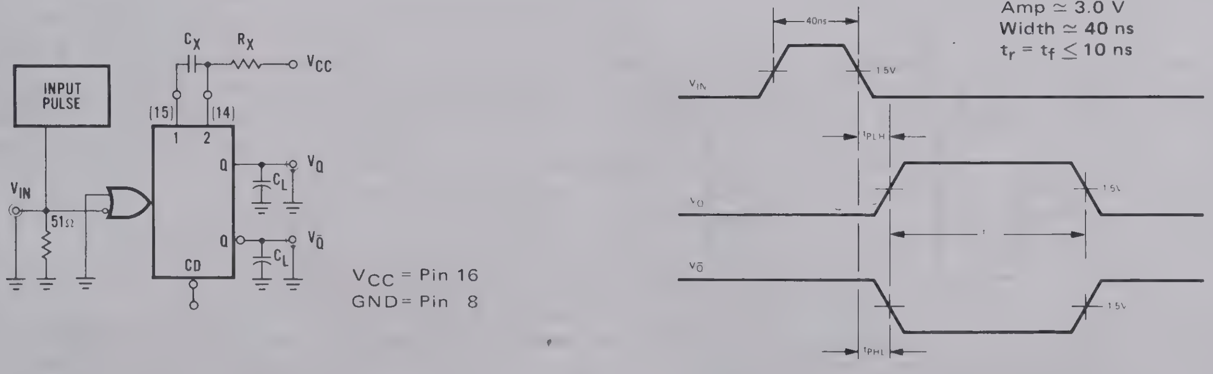
TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ⩾ V_{IH}
L = LOW Voltage Level ⩽ V_{IL}
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

SWITCHING CIRCUITS AND WAVEFORMS

INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 40 ns
$t_r = t_f \leq 10$ ns


INPUT PULSE
V_{IN}
51Ω
C_X
R_X
V_{CC}
(15)
(14)
1
2
Q
$\bar{Q}$
CD
V_Q
$V_{\bar{Q}}$
C_L
C_L
40ns
1.5V
V_{IN}
t_{PLH}
V_Q
1.5V
t
$V_{\bar{Q}}$
1.5V
t_{PHL}

V_{CC} = Pin 16
GND = Pin 8

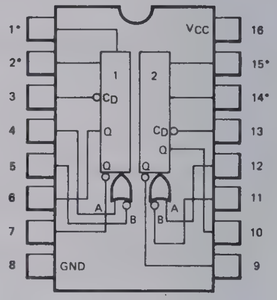
Fig. 18

LPTTL/MONOSTABLE 96L02
LOW POWER DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The TTL/Monostable 96L02 is a low power Dual Retriggerable, Resettable Monostable Multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components. The 96L02 has excellent immunity to noise on the V_{CC} and ground lines. The 96L02 uses TTL inputs and outputs for high speed and high fan out capability and is compatible with all members of the Fairchild TTL family.

- **TYPICAL POWER DISSIPATION OF 25 mW/ONE SHOT**
- **50 ns TYPICAL PROPAGATION DELAY**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **TTL INPUT GATING – LEADING OR TRAILING EDGE TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1*
2*
3
4
5
6
7
8
VCC
GND
1
2
CD
Q
Q
CD
Q
Q
A
B
B
A
16
15*
14*
13
12
11
10
9

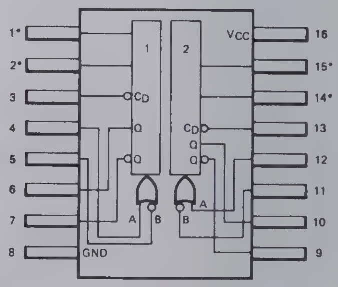
*Pins for external timing.

PIN NAMES

		LOADING	
		HIGH	LOW
$\overline{B}$	Trigger (Active LOW) Input	0.5	0.25
A	Trigger (Active HIGH) Input	0.5	0.25
$\overline{C}_D$	Clear (Active LOW) Input	0.5	0.25
Q	Output (Active HIGH)	9.0	3.0
$\overline{Q}$	Output (Active LOW)	9.0	3.0

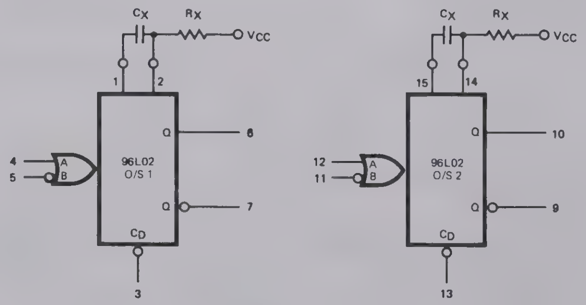
1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW

FLATPAK (TOP VIEW)


1*
2*
3
4
5
6
7
8
VCC
GND
1
2
CD
Q
Q
CD
Q
Q
A
B
B
A
16
15*
14*
13
12
11
10
9

*Pins for external timing.

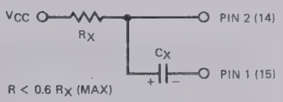
LOGIC DIAGRAM


CX
RX
VCC
1
2
4
5
A
B
96L02
O/S 1
Q
Q
CD
6
7
3
CX
RX
VCC
15
14
12
11
A
B
96L02
O/S 2
Q
Q
CD
10
9
13

FUNCTIONAL DESCRIPTION – The 96L02 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active LOW and one active HIGH. This allows leading edge of trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 96L02 and result in a continuous true output. (See Rule 9) The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW. Active pullups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying the $\overline{Q}$ output to the active level LOW input or the Q output to the active level HIGH input.

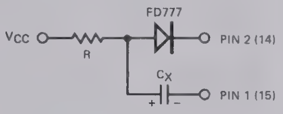
OPERATION RULES

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 16 kΩ to 220 kΩ for 0 to 75°C operation. The value of R_X may vary from 20 kΩ to 100 kΩ for –55 to +125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 1.0 µA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows: $t = 0.33\, R_X C_X \left[1 + \frac{3.0}{R_X}\right]$ (for $C_X > 10^3$ pF) Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF, see Fig. 1
5. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 1.0 µA, and the inverse capacitor leakage at 1.0 V is less than 1.6 µA over the operational temperature range and Rule 3 above is satisfied.



   B. Use with high inverse leakage current electrolytic capacitors:
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

$$t \approx 0.3\, RC_X$$



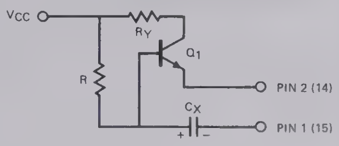
   C. Use to obtain extended pulse widths:
   This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

   $R < R_X\,(0.7)\,(h_{FE}\ Q_1)$ or < 2.5 MΩ whichever is the lesser
   $R_X\,(\text{min}) < R_Y < R_X\,(\text{max})$

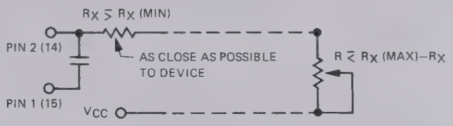
   Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$$t \approx 0.3\, RC_X$$

   This configuration is not recommended with retriggerable operation.

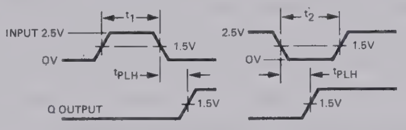


6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

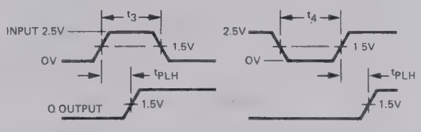


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. See Triggering Truth Table, following pages.

   Input to Pin 5 (11)
   Pin 4 (12) = LOW
   Pin 3 (13) = HIGH
   t_1, t_3 = Min. Positive Input Pulse Width > 60 ns
   t_2, t_4 = Min. Negative Input Pulse Width > 60 ns

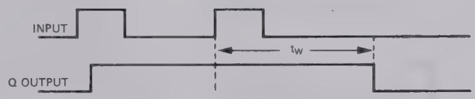


   Input to Pin 4 (12)
   Pin 5 (11) = HIGH
   Pin 3 (13) = HIGH

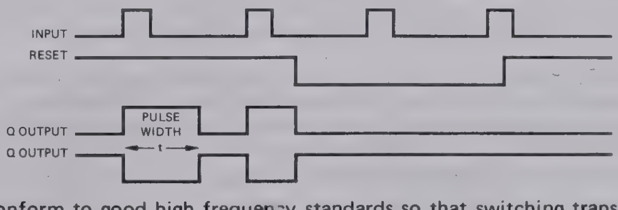


9. The retriggerable pulse width is calculated as shown below:

$$t_W = t + t_{PLH} = 0.33\ R_X\, C_X\, \left(1 + \frac{3.0}{R_X}\right) + t_{PLH}$$



   The retrigger pulse width is equal to the pulse width (t) plus a delay time.
   For pulse widths greater than 500 ns, tw can be approximated as t.
   Retriggering will not occur if the retrigger pulse comes within ≈ 0.9 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle)
10. Reset Operation -- An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one-shots. Use of a 0.01 to 0.1 µF bypass capacitor between V_{CC} and Ground located near the 96L02 is recommended.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
96L02XM	4.5 V	5.0 V	5.5 V	–55°C to 125°C
96L02XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage For all Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage For all Inputs
V_{OH}	Output HIGH Voltage	2.4	3.4		Volts	V_{CC} = MIN., I_{OH} = –0.36 mA
V_{OL}	Output LOW Voltage		0.14	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.80 mA
I_{IH}	Input HIGH Current			20	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		–0.25	–0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	–2.0		–13	mA	V_{CC} = MAX., V_{OUT} = 1.0 V
I_{CC}	Power Supply Current		10	16	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltages extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
96L02XM						
t_{PLH}	Negative Trigger Input to True Output		55	75	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t_{PHL}	Negative Trigger Input to Complement Output		45	62	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t(min)	Minimum True Output Pulse Width		110		ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t	Pulse Width	12.4	13.8	15.2	µs	$V_{CC} = 5.0$ V, $R_X = 39$ kΩ, $C_X = 1000$ pF
R_X	Timing Resistor Range	20		100	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		1.3		%	$R_X = 39$ kΩ, $C_X = 1000$ pF
96L02XC						
t_{PLH}	Negative Trigger Input to True Output		55	80	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t_{PHL}	Negative Trigger Input to Complement Output		45	65	ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t(min)	Minimum True Output Pulse Width		110		ns	$V_{CC} = 5.0$ V, $R_X = 20$ kΩ $C_X = 0$, $C_L = 15$ pF
t	Pulse Width	12.4	13.8	15.2	µs	$V_{CC} = 5.0$ V, $R_X = 39$ kΩ, $C_X = 1000$ pF
R_X	Timing Resistor Range	16		220	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		0.3	1.6	%	$R_X = 39$ kΩ, $C_X = 1000$ pF

OUTPUT PULSE WIDTH (t) USING LOW VALUES OF C_X ($C_X \leqslant 1000$ pF)
(FOR $C_X > 1000$ pF SEE OPERATION RULES 4 AND 5.)

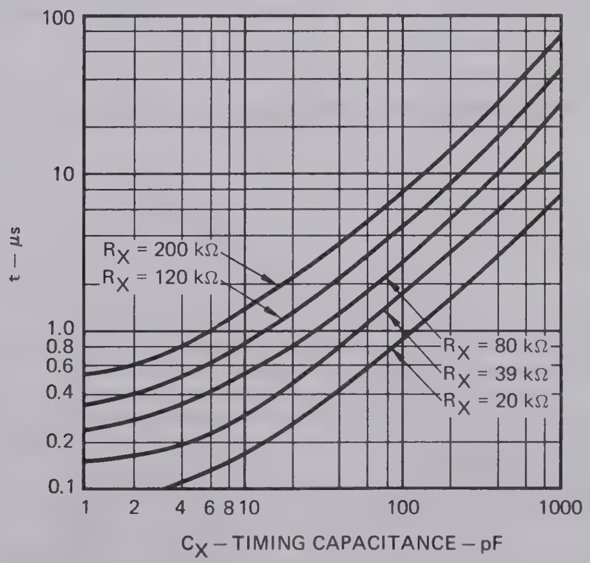
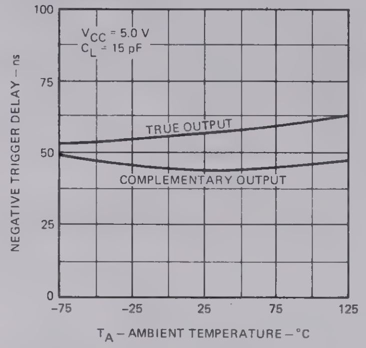


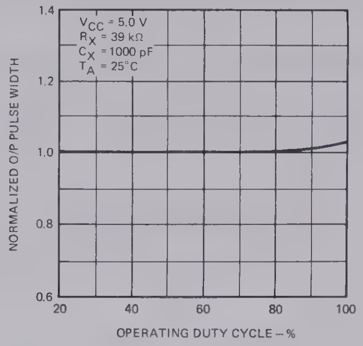
Fig. 1

TYPICAL PULSE CHARACTERISTICS

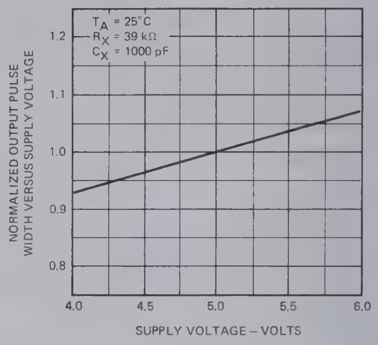
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



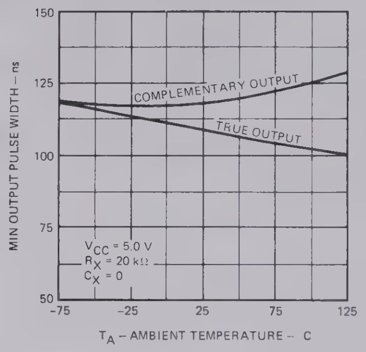
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE



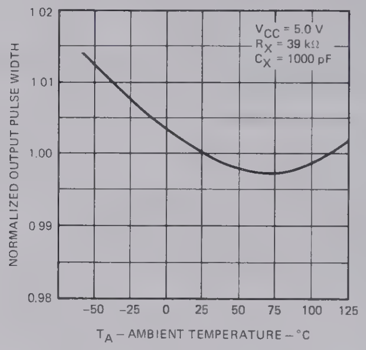
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



MIN. OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

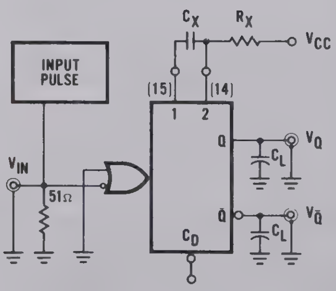


TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

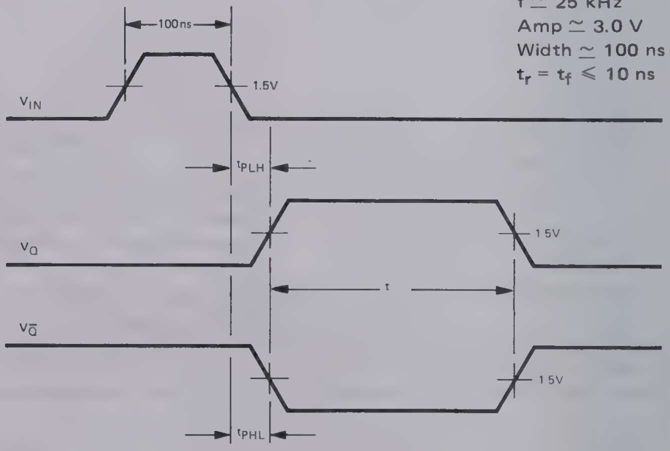
H = HIGH Voltage Level ⩾ V_{IH}
L = LOW Voltage Level ⩽ V_{IL}
X = Don't Care (either H or L)
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

SWITCHING CIRCUITS AND WAVEFORMS



INPUT PULSE
C_X
R_X
V_{CC}
(15)
(14)
1
2
Q
$\bar{Q}$
C_L
C_L
V_Q
$V_{\bar{Q}}$
V_{IN}
51Ω
C_D

V_{CC} = Pin 16
GND = Pin 8



100ns
1.5V
V_{IN}
t_{PLH}
V_Q
1.5V
t
$V_{\bar{Q}}$
1.5V
t_{PHL}

INPUT PULSE
f ≃ 25 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leqslant 10$ ns

TTL/MONOSTABLE 9603/54121, 74121
MONOSTABLE MULTIVIBRATOR

DESCRIPTION — The 9603/54121, 74121 is a TTL Monostable Multivibrator with dc triggering from positive or gated negative going inputs and with inhibit facility. Both positive and negative going output pulses are provided with full fan out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1.0 V/S, providing the circuit with an excellent noise immunity of typically 1.2 V. A high immunity to V_{CC} noise of typically 1.5 V is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 ns to 40 s by choosing appropriate timing components. With no external timing components (i.e., pin 9 connected to pin 14, pins 10, 11 open) an output pulse of typically 30 ns is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

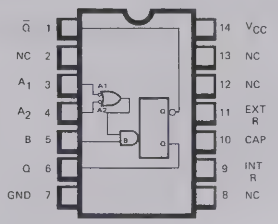
Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T, R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 mW at 5.0 V (50% duty cycle) and a quiescent dissipation of typically 65 mW.

Duty cycles as high as 90% are achieved when using R_T = 40 kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

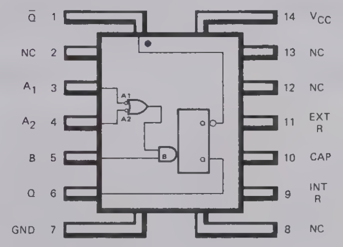
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



Note: 9—11 Timing Pins

FLATPAK (TOP VIEW)



Note: 9—11 Timing Pins

(See Notes 6 thru 9)

TRUTH TABLE (See Notes 1 thru 3)

t_n INPUT			t_{n+1} INPUT			OUTPUT
A_1	A_2	B	A_1	A_2	B	
H	H	L	H	H	H	Inhibit
L	X	H	L	X	L	Inhibit
X	L	H	X	L	L	Inhibit
L	X	L	L	X	H	One Shot
X	L	L	X	L	H	One Shot
H	H	H	X	L	H	One Shot
H	H	H	L	X	H	One Shot
X	L	L	X	H	L	Inhibit
L	X	L	H	X	L	Inhibit
X	L	H	H	H	H	Inhibit
L	X	H	H	H	H	Inhibit
H	H	L	X	L	L	Inhibit
H	H	L	L	X	L	Inhibit

Positive logic: See truth table and notes 5 and 6

$H = V_{IH} \geq 2$ V
$L = V_{IL} \leq 0.8$ V

NOTES:

1. t_n = time before input transition.
2. t_{n+1} = time after input transition.
3. X indicates that either a HIGH or LOW, may be present.
4. NC = No Internal Connection.
5. A_1 and A_2 are negative edge triggered-logic inputs, and will trigger the one shot when either or both go to LOW level with B at HIGH level.
6. B is a positive Schmitt-trigger input for slow edges or level detection and will trigger the one shot when B goes to HIGH level with either A_1 or A_2 at LOW level. (See Truth Table.)
7. External timing capacitor may be connected between pin 10 (positive) and pin 11. With no external capacitance, an output pulse width of typically 30 ns is obtained.
8. To use the internal timing resistor (2 kΩ nominal), connect pin 9 to pin 14.
9. To obtain variable pulse width connect external variable resistance between pin 9 and pin 14. No external current limiting is needed.
10. For accurate repeatable pulse widths connect an external resistor between pin 11 and pin 14 with pin 9 open-circuit.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9603XM/54121XM			9603XC/74121XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N				10			10	U.L.
Input Pulse Rise/Fall Time:	Schmitt Input (B)			1.0			1.0	V/s
	Logic Inputs (A_1, A_2)			1.0			1.0	V/μs
Input Pulse Width		50			50			ns
External Timing Resistance Between Pins 11 and 14 (Pin 9 open)		1.4			1.4			kΩ
External Timing Resistance				30			40	kΩ
Timing Capacitance		0		1000	0		1000	μF
Output Pulse Width				40			40	s
Duty Cycle:	R_T = 2 kΩ			67%			67%	
	R_T = 30 kΩ			90%				
	R_T = 40 kΩ						90%	

X= package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST* FIGURE
			MIN.	TYP. (Note 2)	MAX.			
V_{T+}	Positive-Going Threshold Voltage at A Input			1.4	2.0	Volts	V_{CC} = MIN.	57
V_{T-}	Negative-Going Threshold Voltage at A Input		0.8	1.4		Volts	V_{CC} = MIN.	57
V_{T+}	Positive-Going Threshold Voltage at B Input			1.55	2.0	Volts	V_{CC} = MIN.	57
V_{T-}	Negative-Going Threshold Voltage at B Input		0.8	1.35		Volts	V_{CC} = MIN.	57
V_{OH}	Output HIGH Voltage		2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA	57
V_{OL}	Output LOW Voltage			0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	57
I_{IH}	Input HIGH Current	at A_1 or A_2		2.0	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	60
				0.05	1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
		at B		4.0	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V	61
				0.05	1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current	at A_1 or A_2		−1.0	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	58
		at B		−2.0	−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	59
I_{OS}	Output Short Circuit Current at Q or Q (Note 3)		−20	−25	−55	mA	9603/54121 V_{CC} = MAX.	62 & 63
			−18	−25	−55	mA	9603/74121	
I_{CC}	Supply Current	in Quiescent (Unfired) State		13	25	mA	V_{CC} = MAX.	64
		in Fired State		23	40	mA	V_{CC} = MAX.	64

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

*See parameter measurement information in series 9N/54, 74TTL section.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST * FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay B Input to Q Output	15	35	55	ns	V_{CC} = 5.0 V C_L = 15 pF C_T = 80 pF		H
t_{PLH}	Turn Off Delay A_1/A_2 Inputs to Q Output	25	45	70				
t_{PHL}	Turn On Delay B Input to $\overline{Q}$ Output	20	40	65				
t_{PHL}	Turn On Delay A_1/A_2 Inputs to $\overline{Q}$ Output	30	50	80				
$t_{pw(out)}$	Pulse Width Obtained Using Internal Timing Resistor	70	110	150	ns	C_T = 80 pF	V_{CC} = 5.0 V C_L = 15 pF R_T = Open Pin 9 to V_{CC}	I
$t_{pw(out)}$	Pulse Width Obtained with Zero Timing Capacitance	20	30	50	ns	C_T = 0 pF		
$t_{pw(out)}$	Pulse Width Obtained Using External Timing Resistor	600	700	800	ns	C_T = 100 pF	V_{CC} = 5.0 V C_L = 15 pF R_T = 10 kΩ Pin 9 to Open	
		6.0	7.0	8.0	ms	C_T = 1.0 μF		
t_{hold}	Minimum Duration of Trigger Pulse		30	50	ns	C_T = 80 pF	V_{CC} = 5.0 V C_L = 15 pF R_T = Open Pin 9 to V_{CC}	

*See parameter measurement information in series 9N/54, 74 section.

TYPICAL CHARACTERISTICS

Fig. 1
VARIATION IN INTERNAL TIMING RESISTOR VALUE VERSUS AMBIENT TEMPERATURE

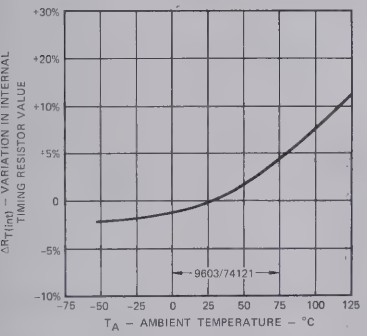


Fig. 2
VARIATION IN OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

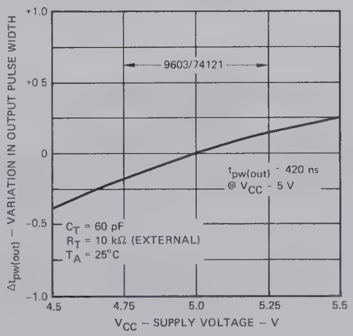


Fig. 3
VARIATION IN OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

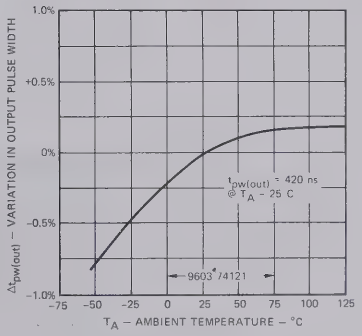


Fig. 4
SCHMITT TRIGGER THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE

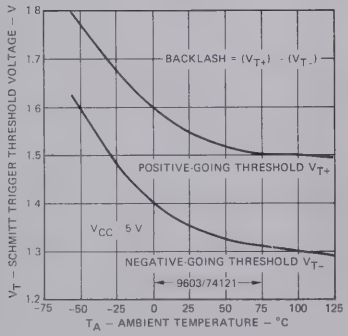


Fig. 5
TURN OFF DELAY TIME B INPUT TO Q OUTPUT VERSUS AMBIENT TEMPERATURE

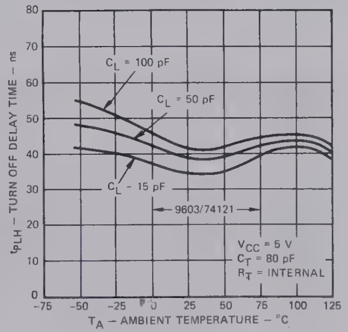
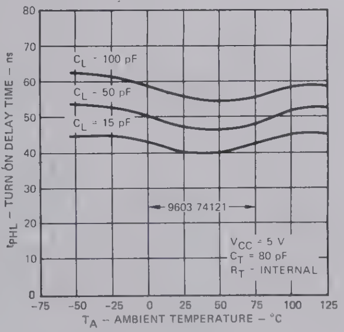


Fig. 6
TURN ON DELAY TIME B INPUT TO $\overline{Q}$ OUTPUT VERSUS AMBIENT TEMPERATURE



TYPICAL CHARACTERISTICS (Cont'd)

Fig. 7
OUTPUT PULSE WIDTH VERSUS TIMING RESISTOR VALUE

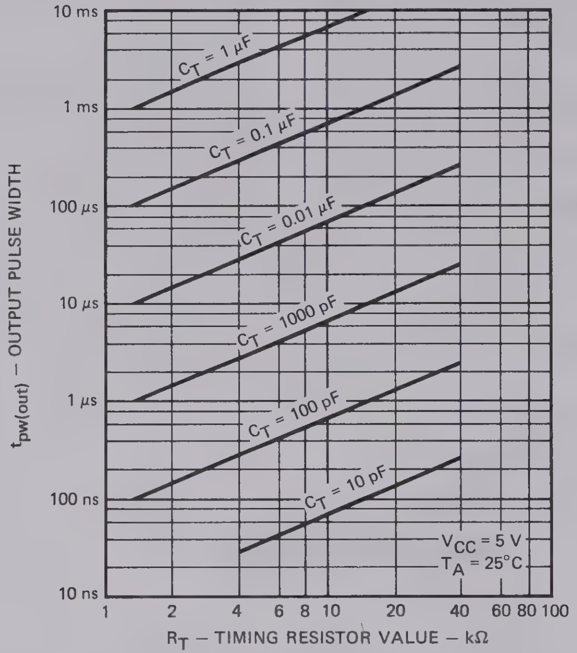
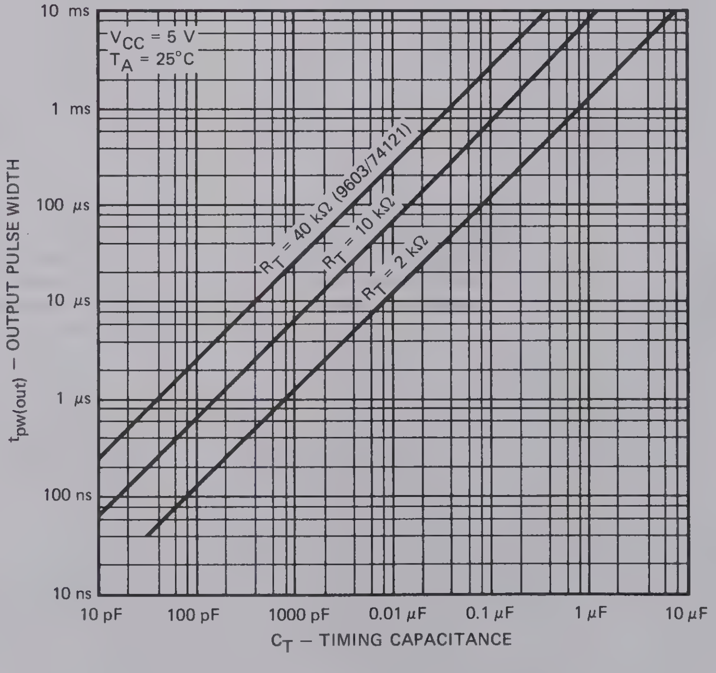


Fig. 8
OUTPUT PULSE WIDTH VERSUS EXTERNAL CAPACITANCE



μA9614

DUAL DIFFERENTIAL LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA9614 is a TTL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTL, with the active pull-up and the pull-down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other (See Fig. 5). The active pull-up is short circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary providing "NAND" and "AND" functions of the inputs, adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both input and output to handle line transients.

- **SINGLE 5 VOLT SUPPLY**
- **TTL COMPATIBLE INPUTS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS**
- **COMPLIMENTARY OUTPUTS FOR 'NAND', 'AND' OPERATION**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR APPLICATION**
- **MILITARY TEMPERATURE RANGE**

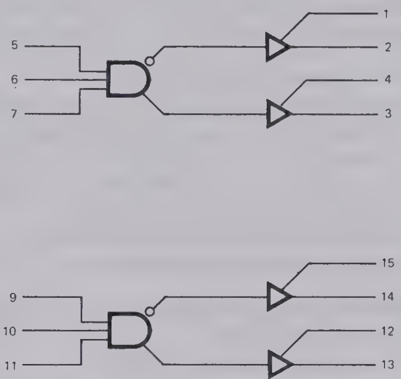
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.7 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collector)	−0.5 V to +12 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	
Ceramic DIP	730 mW
Flatpak	570 mW

NOTE

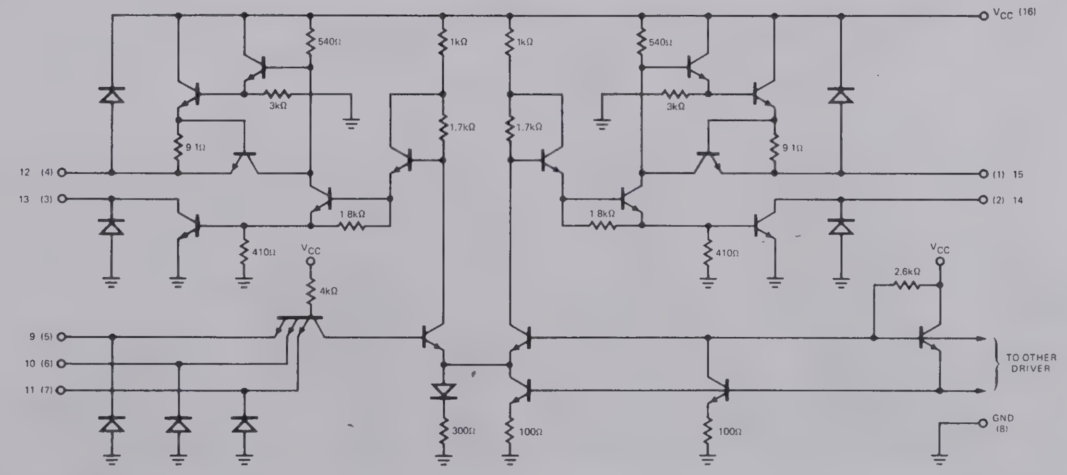
1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

EQUIVALENT CIRCUIT (1/2 9614)



µA9615

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The µA9615 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 V supply. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe and a 130 Ω terminating resistor are provided at the inputs. The output has an uncommitted collector with an active pull-up available on an adjacent pin to allow either "wire-or" or active pull up TTL output configuration.

- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **CHOICE OF AN UNCOMMITTED COLLECTOR OR ACTIVE PULL-UP**
- **STROBE**
- **FULL MILITARY TEMPERATURE RANGE**
- **SINGLE 5 V SUPPLY VOLTAGES**
- **FREQUENCY RESPONSE CONTROL**
- **130 Ω TERMINATING RESISTOR**

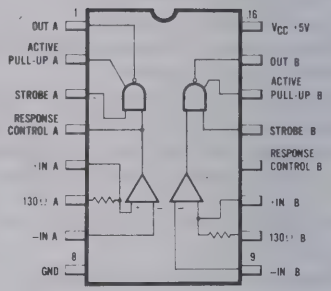
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	–0.5 V to +7.0 V
Input Voltage Referred to Ground (Pins 5, 6, 7, 9, 10, 11)	±20 V
Voltage Applied to Outputs for HIGH Output State without Active Pull Up	–0.5 V to +13.2 V
Voltage Applied to Strobe	–0.5 V to +5.5 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	
Ceramic DIP	730 mW
Flatpak	570 mW

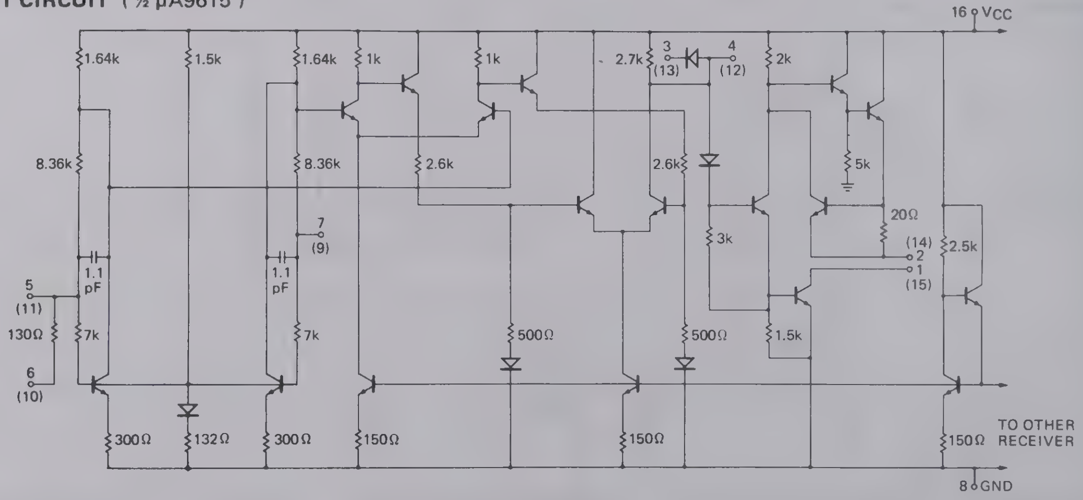
NOTE

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak Package.

LOGIC DIAGRAM


OUT A
ACTIVE PULL-UP A
STROBE A
RESPONSE CONTROL A
+IN A
130Ω A
–IN A
GND
1
8
16
9
V_{CC} +5V
OUT B
ACTIVE PULL-UP B
STROBE B
RESPONSE CONTROL B
+IN B
130Ω B
–IN B

EQUIVALENT CIRCUIT (½ µA9615)


16 V_{CC}
1.64k
1.5k
1.64k
1k
1k
2.7k
3 (13)
4 (12)
2k
8.36k
8.36k
2.6k
2.6k
5k
7 (9)
20Ω
3k
(14) 2
1 (15)
2.5k
5 (11)
1.1 pF
1.1 pF
130Ω
7k
7k
500Ω
500Ω
1.5k
6 (10)
300Ω
132Ω
300Ω
150Ω
150Ω
150Ω
TO OTHER RECEIVER
8 GND

μA9616

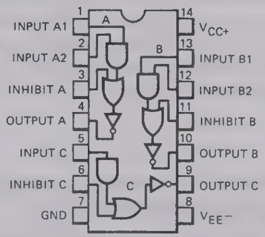
TRIPLE EIA RS-232-C LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9616 is a Triple Line Driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24. Each driver in the μA9616 converts TTL/DTL logic level to EIA/CCITT levels for transmission between data terminal equipment and data communication equipment. The μA9617 performs the complementary functions. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH level on the inhibit terminal interrupts signal transfer and forces the output to a $-V_{OUT}$ or MARK state. The μA9616 is constructed on a single silicon chip using the Fairchild Planar* process.

- INTERNAL SLEW RATE LIMITING
- NO EXTERNAL CAPACITORS REQUIRED
- THREE CHANNELS PER PACKAGE
- MEETS EIA RS-232-C AND CCITT V.24 SPECIFICATIONS
- LOGICAL TRUE INHIBIT FUNCTION
- SUPPLY INDEPENDENT OUTPUT SWING
- OUTPUT CURRENT LIMITING

CONNECTION DIAGRAM
(TOP VIEW)


INPUT A1
INPUT A2
INHIBIT A
OUTPUT A
INPUT C
INHIBIT C
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
A
B
C
VCC+
INPUT B1
INPUT B2
INHIBIT B
OUTPUT B
OUTPUT C
VEE−

TRUTH TABLE

INPUT 1	INPUT 2	INHIBIT	OUTPUT
All Sections:			
L	L	L	H
H	H	L	L
L	L	H	L
H	H	H	L
For Channels A & B add:			
L	H	L	H
H	L	L	H
L	H	H	L
H	L	H	L

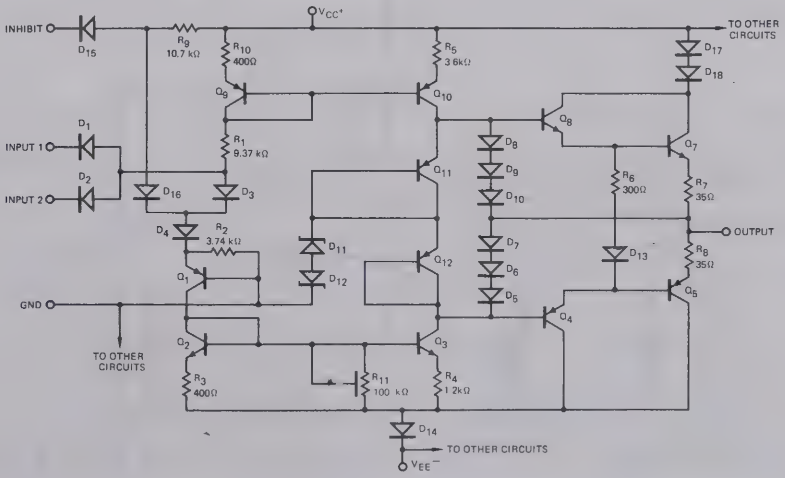
(For Channel C, omit INPUT 2 Column)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±15 V
Input or Inhibit Voltage	−1.5 to +6 V
Output Signal Voltage	±15 V
Maximum Power Dissipation (Note 1)	630 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature	0°C to +75°C
Lead Temperature (Soldering, 60 seconds)	300°C

Note 1: Perate 8.3mW/°C above 70°C

EQUIVALENT CIRCUIT (One of three channels)


INHIBIT
D15
R9 10.7 kΩ
R10 400Ω
VCC+
R5 3.6kΩ
TO OTHER CIRCUITS
D17
D18
Q9
Q10
Q8
Q7
D1
INPUT 1
R1 9.37 kΩ
D8
D9
D10
R6 300Ω
R7 35Ω
Q11
D2
INPUT 2
D16
D3
D4
R2 3.74 kΩ
D11
D12
D7
D6
D5
D13
OUTPUT
R8 35Ω
Q12
Q1
GND
Q5
Q4
Q2
Q3
TO OTHER CIRCUITS
R3 400Ω
R11 100 kΩ
R4 1.2kΩ
D14
TO OTHER CIRCUITS
VEE−

*Planar is a patented Fairchild process.

μA9617

TRIPLE EIA RS-232-C LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA9617 is a Triple Line Receiver designed to meet the terminator electrical requirements of EIA RS-232-C AND CCITT V.24. It receives line signals produced by the μA9616, an EIA/CCITT driver, and converts them to TTL compatible logic levels. The inputs have a resistance between 3 kΩ and 7 kΩ and can withstand ±25 V. Each receiver can operate in either hysteresis or non-hysteresis (slicing) modes, and each receiver provides fail-safe operation as defined by Section 2.5 of RS-232-C. Noise immunity may be increased by connecting a capacitor between the response control pin and ground. The μA9617 is constructed on a single silicon chip using the Fairchild Planar* process.

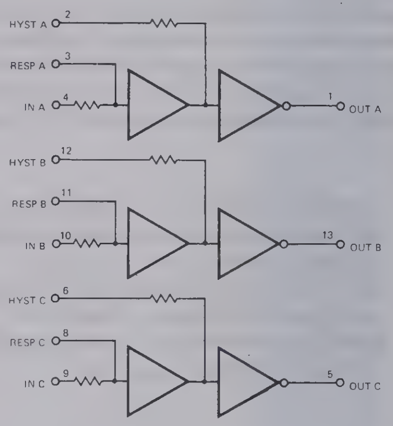
- **MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS**
- **FAIL-SAFE OPERATION**
- **HYSTERESIS OR NON-HYSTERESIS MODE**
- **INDIVIDUAL RESPONSE CONTROLS**
- **TTL COMPATIBLE OUTPUT**
- **SINGLE +5 V SUPPLY**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 V
Input Voltage	±25V
Output Current	25 mA
Maximum Power Dissipation (Note 1)	630mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +75°C
Lead Temperature (Soldering, 60 seconds)	300°C

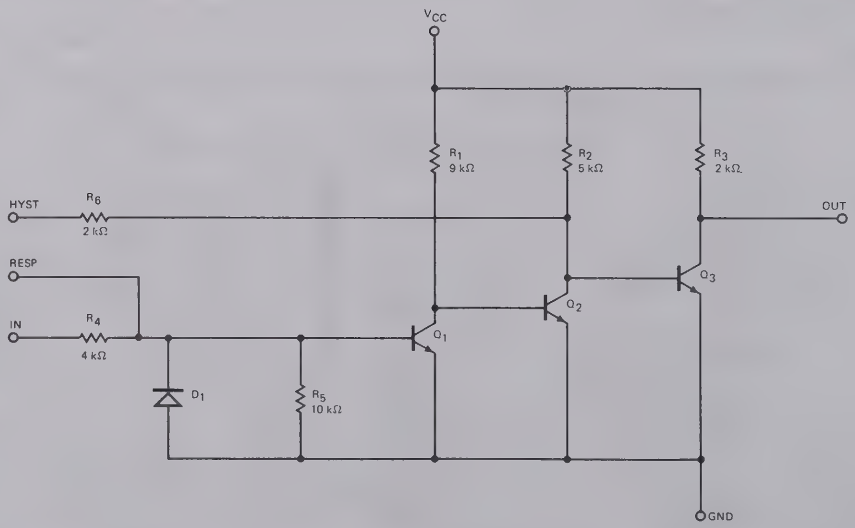
Note 1. Derate 8.3 mW/°C above 70°C

LOGIC DIAGRAM


HYST A
2
RESP A
3
IN A
4
1
OUT A
HYST B
12
RESP B
11
IN B
10
13
OUT B
HYST C
6
RESP C
8
IN C
9
5
OUT C

V_{CC} = Pin 14
GND = Pin 7

EQUIVALENT CIRCUIT (One of three identical circuits)


V_{CC}
R_1
9 kΩ
R_2
5 kΩ
R_3
2 kΩ
HYST
R_6
2 kΩ
OUT
RESP
Q_3
Q_2
IN
R_4
4 kΩ
Q_1
D_1
R_5
10 kΩ
GND

*Planar is a patented Fairchild process.

μA9620

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA9620 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges. It can receive ±500 mV of differential data in the presence of HIGH level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output. In addition to line reception the μA9620 can perform many functions, a few of which are presented in the applications section. It can interface with nearly all input logic levels including CML, CTL, HLLDTL, RTL and TTL. HLLDTL logic can be provided by tieing the output to V_{CC2} (+12 V) through a resistor. The outputs can also be wired-OR. The μA9620 offers the advantages of logic compatible voltages (+5 V, +12 V), TTL output characteristics, and a flexible input array with a high common mode range. The direct inputs are provided in addition to the attenuated inputs (normally used) to allow the input attenuation and response time to be changed by use of external components.

- TTL COMPATIBLE OUTPUT
- HIGH COMMON MODE VOLTAGE RANGE
- WIRED-OR CAPABILITY
- DIRECT INPUTS (A_D, B_D)
- FULL MILITARY TEMPERATURE RANGE
- LOGIC COMPATIBLE SUPPLY VOLTAGES

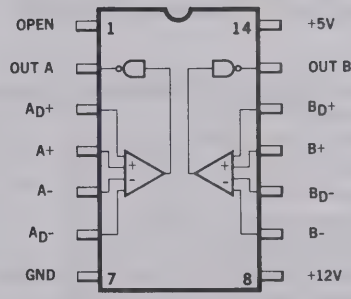
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V
Voltage Applied to Outputs for HIGH Output State	−0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	
Ceramic DIP	670 mW
Flatpak	570 mW

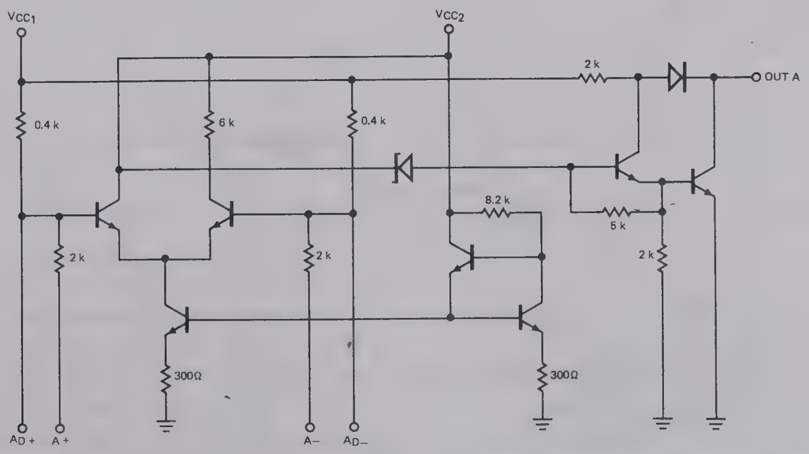
NOTE

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak Package.

LOGIC DIAGRAM



EQUIVALENT CIRCUIT



μA9621

DUAL LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130 Ω twisted pair are provided. The output has the capability of driving high capacitance loads. It can typically switch >200 mA during transients.

- **TTL COMPATIBILITY**
- **TRANSMISSION LINE BACK-MATCHING**
- **OUTPUT CLAMP DIODES**
- **HIGH CAPACITANCE DRIVE**
- **HIGH OUTPUT VOLTAGE**
- **MILITARY TEMPERATURE RANGE**

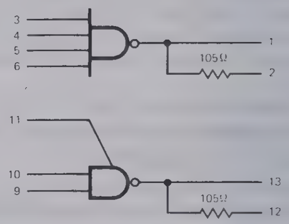
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	+3.8 V to +8 V
Input Voltage	–0.5 V to +15 V
Voltage Applied to Outputs	–2 V to $+V_{CC1}$ +1 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note)	
Ceramic DIP	670 mW
Flatpak	570 mW

NOTE

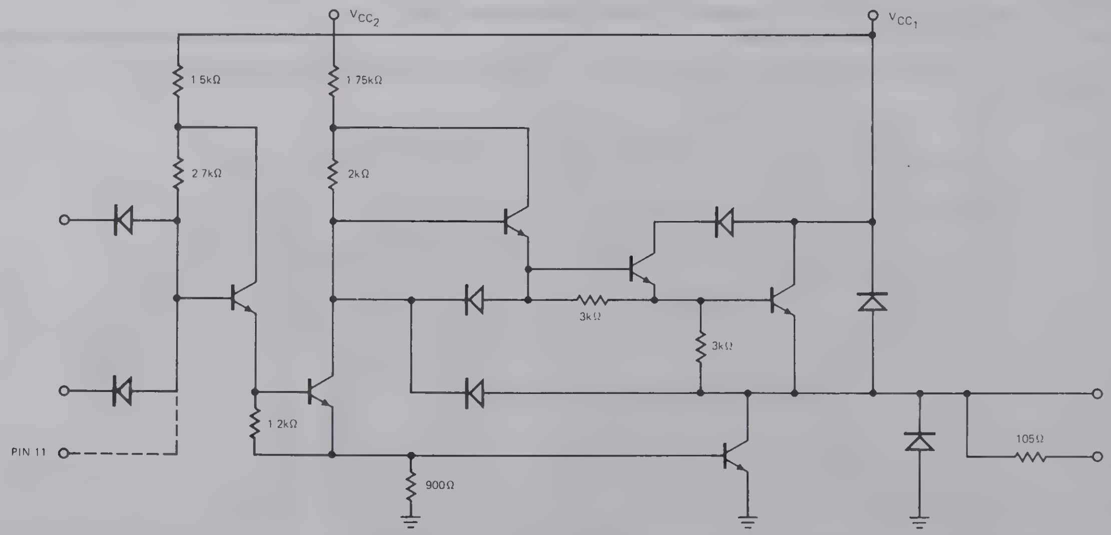
Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak Package.

LOGIC DIAGRAM



V_{CC_1} = 14, V_{CC_2} = 8, GND = 7

SCHEMATIC DIAGRAM (ONE SIDE ONLY)



µA9622
DUAL LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

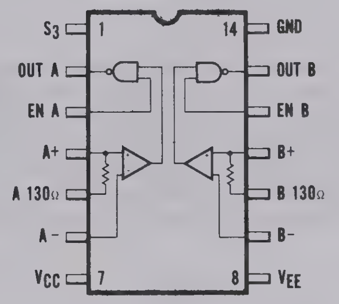
GENERAL DESCRIPTION — The µA9622 is a Dual Line Receiver designed to discriminate a worst case logic swing of 2.0 V from a ±10 V common mode noise signal or ground shift. A 1.5 V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only ±5% (75 mV) over the military and industrial temperature ranges.

The µA9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S_3*. A 130 Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output HIGH level can be increased to +12 V by tieing it to a positive supply through a resistor. The output circuits allow wired-OR operation.

*S_3 connected to V_{CC}—open inputs causes output to be V_{OH}.
S_3 connected to Ground—open inputs causes output to be V_{OL}.

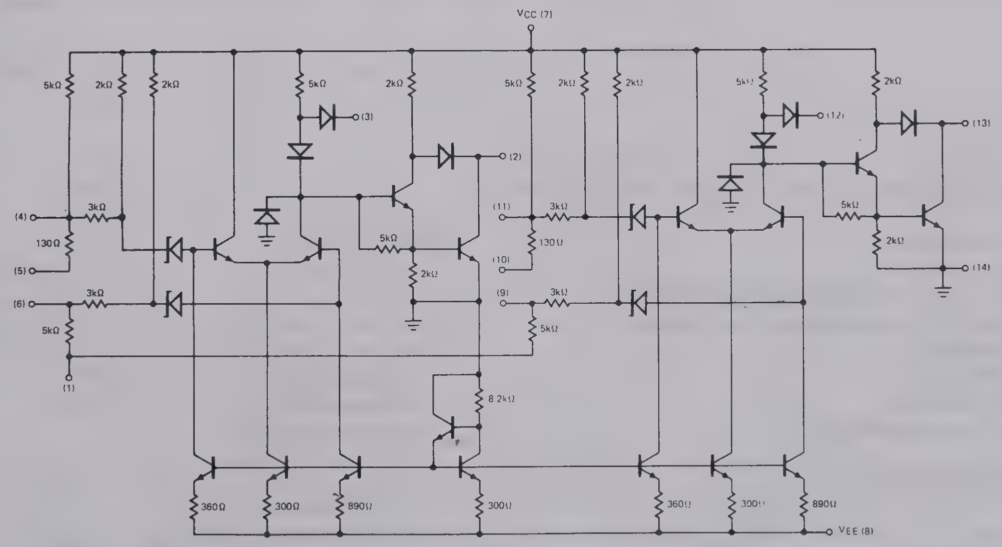
- TTL COMPATIBLE THRESHOLD VOLTAGE
- INPUT TERMINATING RESISTORS
- CHOICE OF OUTPUT STATE WITH INPUTS OPEN
- TTL COMPATIBLE OUTPUT
- HIGH COMMON MODE
- WIRE-OR CAPABILITY
- ENABLE INPUTS
- FULL MILITARY TEMPERATURE RANGE
- LOGIC COMPATIBLE SUPPLY VOLTAGES

LOGIC DIAGRAM



S3
1
14
GND
OUT A
OUT B
EN A
EN B
A+
B+
A 130Ω
B 130Ω
A −
B−
VCC
7
8
VEE

EQUIVALENT CIRCUIT



VCC (7)
5kΩ
2kΩ
2kΩ
5kΩ
2kΩ
5kΩ
2kΩ
2kΩ
5kΩ
2kΩ
(3)
(2)
(12)
(13)
(4)
3kΩ
130Ω
(5)
(6)
3kΩ
5kΩ
(1)
5kΩ
2kΩ
(11)
3kΩ
130Ω
(10)
(9)
3kΩ
5kΩ
5kΩ
2kΩ
(14)
8.2kΩ
360Ω
300Ω
890Ω
300Ω
360Ω
300Ω
890Ω
VEE (8)

μA9624 • μA9625
DUAL TTL, MOS INTERFACE ELEMENTS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9624 is a Dual 2-Input TTL Compatible Interface gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

The μA9625 is a dual MOS to TTL level converter. It is designed to convert standard negative MOS logic levels to TTL levels. The μA9625 features a high input impedance which allows preservation of the driving MOS logic level.

Both the μA9624 and μA9625 are available in the 14-lead Ceramic Dual In-Line Package and the 1/4 x 1/4 Flatpak.

NOTE: The TTL and MOS devices manufactured by Fairchild Semiconductor are considered as positive TRUE logic (the more positive voltage level is assigned the binary state of "1" or TRUE). Following MIL-STD-806B logic symbol specifications, the μA9624 is represented as a NAND gate and the μA9625 as a non-inverting buffer. This convention (of assuming MOS as a positive TRUE logic) has not been uniformly accepted by the industry; therefore, it is necessary to note that with negative TRUE MOS logic (the more negative voltage level is assigned the binary state "1" or TRUE), the μA9624 acts as an AND gate and the μA9625 as an inverter.

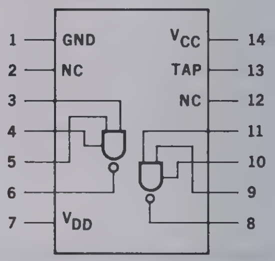
- **TTL COMPATIBLE INPUTS/OUTPUT**
- **MOS COMPATIBLE OUTPUT/INPUTS**
- **LOW POWER**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

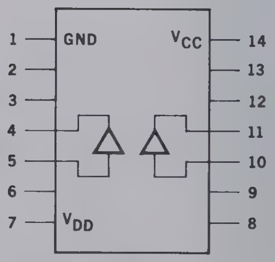
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	V_{DD} to +10 V
Voltage Applied to Outputs for HIGH Output State (μA9624)	V_{DD} to $+V_{CC}$ value
Voltage Applied to Outputs for HIGH Output State (μA9625)	−0.5 V to V_{CC} value
Input Voltage (dc) (μA9624)	−0.5 V to +5.5 V
Input Voltage (dc) (μA9625)	V_{CC} to V_{DD}
V_{DD} Pin Potential to Ground Pin	−30 V to +0.5 V
V_{DD} Pin Potential to Tap Pin (μA9624)	−30 V to +0.5 V
V_{TAP}	V_{CC} +0.5 V
Internal Power Dissipation (Note 3)	
Ceramic DIP	670 mW
Flatpak	570 mW
Lead Temperature (Soldering, 60 seconds)	300°C

LOGIC DIAGRAMS

μA9624



μA9625



μA9644

DUAL HIGH VOLTAGE, HIGH CURRENT DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9644 is a Dual 4-Input NAND Gate whose output can sink 500 mA in the LOW state, and maintain 30 V in the HIGH state. The outputs are uncommitted collectors in a Darlington configuration which have typical saturation voltages of 0.8 V at low currents and 1.2 V at 500 mA. The inputs are TTL Compatible and feature input clamp diodes. The input fan in requirement is typically 1/2 a normal DTL Unit Load. An input strobe common to both gates in provided, and an expander input node on each gate is available for input diode expansion. Separate ground pins are provided for each gate to minimize ground pin offset voltages at high current levels.

- **500 mA CURRENT SINKING CAPABILITY**
- **OUTPUT VOLTAGES UP TO 30 V**
- **LOW AVERAGE POWER, TYPICALLY 30 mW PER GATE**
- **HIGH SPEED, TYPICALLY 50 ns DELAY TIMES**
- **TTL COMPATIBLE INPUTS**
- **INPUT CLAMP DIODES**
- **LOW FAN IN LOADING REQUIREMENTS**
- **COMMON STROBE INPUT**
- **EXPANDER NODE FOR INPUT DIODE EXPANSION**

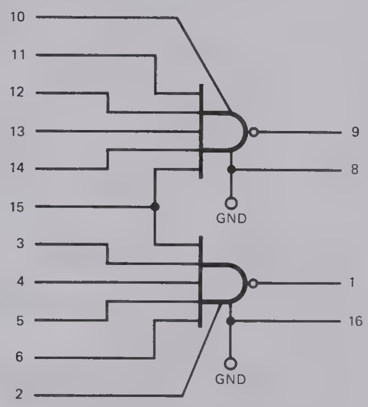
ABSOLUTE MAXIMUM RATING

Storage Temperature		–65°C to +175°C
Temperature (Ambient) Under Bias		–55°C to +125°C
V_{CC} Pin Potential to Ground Pin		–0.5 V to +8.0 V
Input Voltages (dc)		–0.5 V to +5.5 V
Voltage Applied to Outputs (Output HIGH)	See Safe Area Curves on following pages	–0.5 V to +30 V
Output Current (dc) (Output LOW)		640 mA
Internal Power Dissipation (Note)		730 mW
Lead Temperature (Soldering, 60 seconds)		300°C

NOTE

Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP .

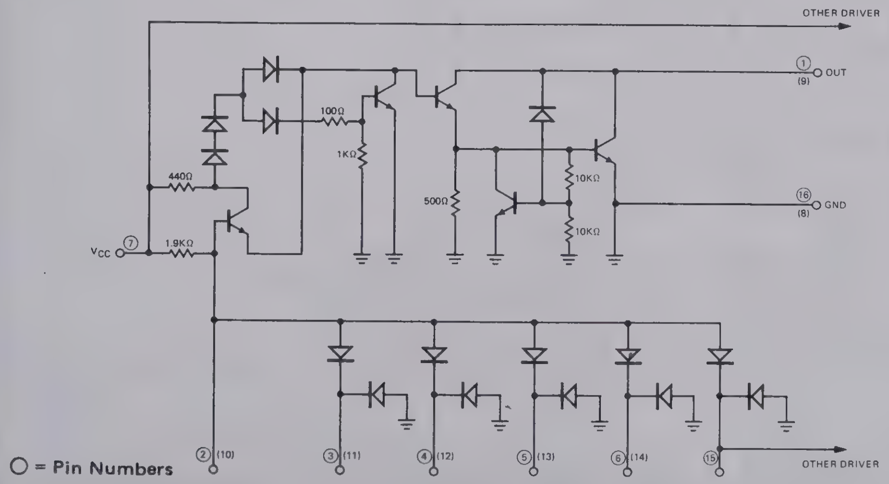
LOGIC DIAGRAM


10
11
12
13
14
15
3
4
5
6
2
9
8
GND
1
16
GND

V_{CC} = Pin 7

Fig. 1

EQUIVALENT CIRCUIT (One of two identical channels)


OTHER DRIVER
① OUT
(9)
100Ω
1KΩ
440Ω
500Ω
10KΩ
10KΩ
⑯ GND
(8)
VCC ⑦
1.9KΩ
○ = Pin Numbers
② (10)
③ (11)
④ (12)
⑤ (13)
⑥ (14)
⑮
OTHER DRIVER

CONNECTION DIAGRAM

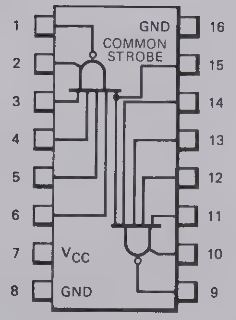

1
2
3
4
5
6
7
8
GND
COMMON STROBE
VCC
GND
16
15
14
13
12
11
10
9

Fig. 2

SN55107 • SN75107 • SN55108 • SN75108

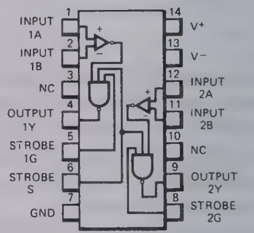
DUAL LINE RECEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

DESCRIPTION—The SN55107/75107 and SN55108/75108 are high speed, Two-Channel Line Receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3V but can be increased to ±15V by the use of input attenuators. Separate or common strobes are available. The SN55107/75107 circuit features an active pull-up (totem pole output). The SN55108/75108 circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the SN55109/75109 and SN55110/75110 line drivers. The SN55107/75107 and SN55108/75108 line receivers are useful in high speed balanced, unbalanced and party line transmission systems and as data comparators.

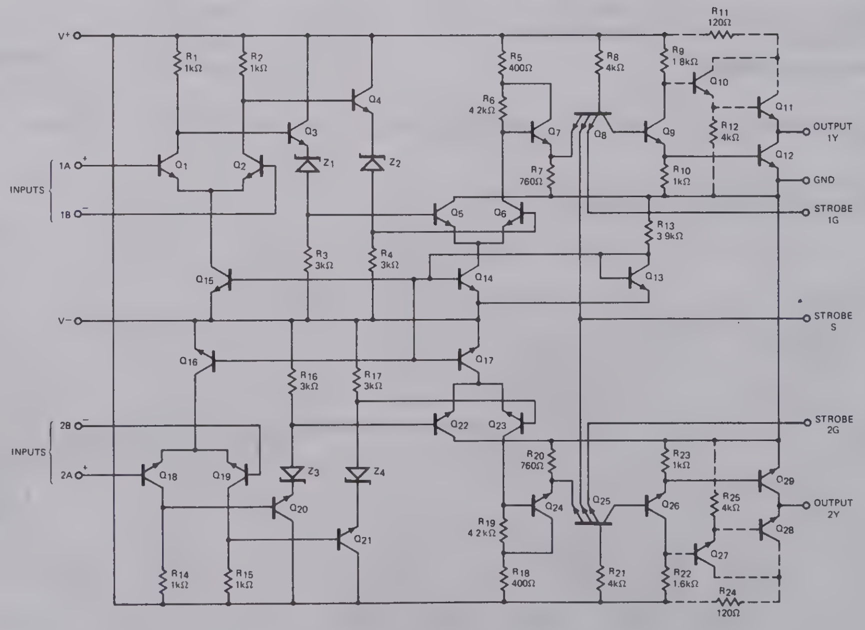
- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **HIGH COMMON-MODE REJECTION RATIO**
- **HIGH INPUT IMPEDANCE**
- **HIGH INPUT SENSITIVITY**
- **INPUT COMMON-MODE VOLTAGE RANGE OF ±3V**
- **SEPARATE OR COMMON STROBES**
- **TTL OR DTL DRIVE CAPABILITY**
- **WIRED-OR OUTPUT CAPABILITY (SN55108/75108 ONLY)**
- **HIGH DC NOISE MARGINS**

CONNECTION DIAGRAM
(TOP VIEW)



INPUT 1A
INPUT 1B
NC
OUTPUT 1Y
STROBE 1G
STROBE S
GND
V+
V−
INPUT 2A
INPUT 2B
NC
OUTPUT 2Y
STROBE 2G
1
2
3
4
5
6
7
8
9
10
11
12
13
14

EQUIVALENT CIRCUIT



V+
V−
INPUTS
1A +
1B −
2B −
2A +
R1 1kΩ
R2 1kΩ
R3 3kΩ
R4 3kΩ
R5 400Ω
R6 4.2kΩ
R7 760Ω
R8 4kΩ
R9 1.8kΩ
R10 1kΩ
R11 120Ω
R12 4kΩ
R13 3.9kΩ
R14 1kΩ
R15 1kΩ
R16 3kΩ
R17 3kΩ
R18 400Ω
R19 4.2kΩ
R20 760Ω
R21 4kΩ
R22 1.6kΩ
R23 1kΩ
R24 120Ω
R25 4kΩ
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Z1
Z2
Z3
Z4
OUTPUT 1Y
GND
STROBE 1G
STROBE S
STROBE 2G
OUTPUT 2Y

NOTE: Components shown with dashed lines are applicable to the SN55107 and SN75107 only.

SN55109 • SN75109 • SN55110 • SN75110

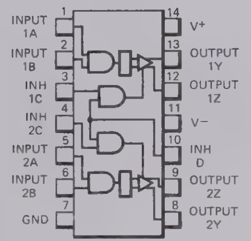
DUAL LINE DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

DESCRIPTION – The SN55109/75109 and SN55110 are Dual Line Drivers featuring independent channels with common supply voltage and ground terminals. The major difference between the SN55109/75109 and the SN55110/75110 drivers is the output-current specification. The output current is nominally 6 mA for the SN55109/75109 and 12 mA for the SN55110/75110. The driver circuits have a constant output that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off by appropriate logic levels at the inhibit inputs. The circuit also features an inhibit input that is common to both drivers, providing more circuit versatility. The common-mode voltage range of the driver outputs is –3 V to +10 V, which allows a common-mode voltage on the line without affecting the driver performance. For application information see SN55107 • SN75107 • SN55108 • SN75108 Data Sheet.

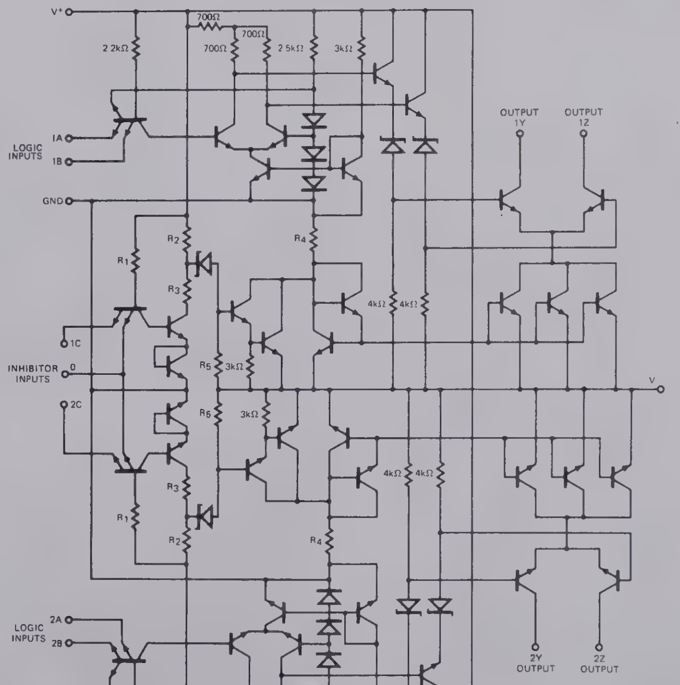
- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **TTL INPUT COMPATIBILITY**
- **CURRENT-MODE OUTPUT (6mA or 12mA TYPICAL)**
- **HIGH OUTPUT IMPEDANCE**
- **HIGH COMMON-MODE OUTPUT VOLTAGE RANGE (–3V to 10V)**
- **INHIBITOR AVAILABLE FOR DRIVER SELECTION**

CONNECTION DIAGRAM
(TOP VIEW)



INPUT 1A
INPUT 1B
INH 1C
INH 2C
INPUT 2A
INPUT 2B
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V+
OUTPUT 1Y
OUTPUT 1Z
V−
INH D
OUTPUT 2Z
OUTPUT 2Y

EQUIVALENT CIRCUIT



V+
700Ω
700Ω
700Ω
2.2kΩ
2.5kΩ
3kΩ
LOGIC INPUTS
1A
1B
GND
OUTPUT 1Y
OUTPUT 1Z
R2
R1
R3
R4
4kΩ
4kΩ
1C
INHIBITOR INPUTS
D
2C
R5
3kΩ
R5
3kΩ
V−
4kΩ
4kΩ
R3
R1
R2
R4
LOGIC INPUTS
2A
2B
2Y OUTPUT
2Z OUTPUT
2.2kΩ
700Ω
700Ω
2.5kΩ
3kΩ

	SN55109 SN75109	SN55110 SN75110
R_1	4 kΩ	2.2 kΩ
R_2	1.5 kΩ	820 Ω
R_3	440 Ω	240 Ω
R_4	1.75 kΩ	875 Ω
R_5	2.74 kΩ	1.5 kΩ

NOTES:
1. Component values shown are nominal.
2. Resistance values are in ohms.

SN75450

DUAL PERIPHERAL DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The SN75450 is a versatile general purpose dual interface driver circuit that employs TTL or DTL logic. The SN75450 features two standard series 74 TTL gates and two uncommitted, high current, high voltage transistors offering the system designer the flexibility to tailor the circuit to his application. The SN75450 is useful in high speed logic buffers, power drivers, lamp drivers, relay drivers, line drivers, MOS drivers, clock drivers and memory drivers.

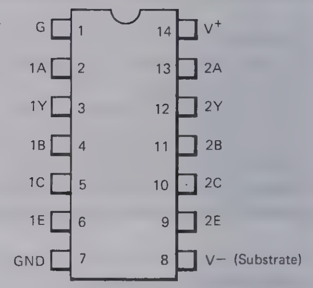
- **HIGH SPEED**
- **300 mA CURRENT CAPABILITY**
- **HIGH VOLTAGE CAPABILITY**
- **UNCOMMITTED OUTPUT DEVICES**
- **TTL OR DTL INPUT COMPATIBILITY**

ABSOLUTE MAXIMUM RATINGS

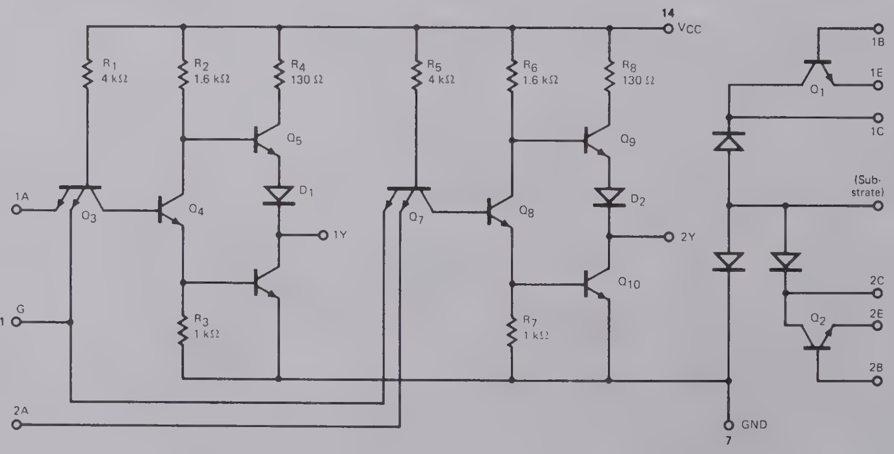
Supply Voltage (Note 1)	+7 V
Internal Power Dissipation (Note 2)	800 mW
Input Voltage (Note 3)	5.5 V
V_{CC} to Substrate or Collector to Substrate Voltage	35 V
Collector to Base Voltage	35 V
Emitter To Base Voltage	5 V
Collector to Base Voltage (Note 4)	30 V
Continuous Collector Current	300 mA
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 seconds)	300°C

CONNECTION DIAGRAM
(TOP VIEW)

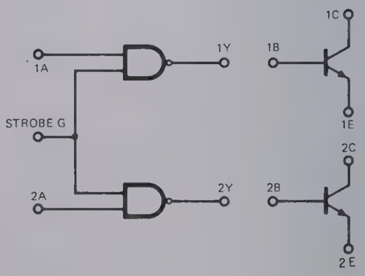
14 LEAD DIP

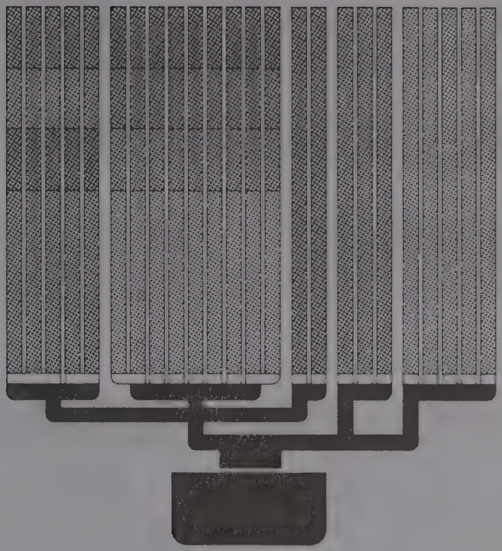

G 1
1A 2
1Y 3
1B 4
1C 5
1E 6
GND 7
14 V+
13 2A
12 2Y
11 2B
10 2C
9 2E
8 V− (Substrate)

EQUIVALENT CIRCUIT


14
VCC
R1 4 kΩ
R2 1.6 kΩ
R4 130 Ω
R5 4 kΩ
R6 1.6 kΩ
R8 130 Ω
Q5
Q9
Q1
1B
1E
1C
1A
Q3
Q4
D1
Q7
Q8
D2
(Substrate)
1Y
2Y
Q10
2C
2E
Q2
2B
G
1
R3 1 kΩ
R7 1 kΩ
2A
GND
7

BLOCK DIAGRAM


1A
STROBE G
2A
1Y
2Y
1B
1C
1E
2B
2C
2E



MSI
9300, 93L, 93S and 54/74 Series Data Sheets

TTL/MSI 9300
4-BIT UNIVERSAL SHIFT REGISTER

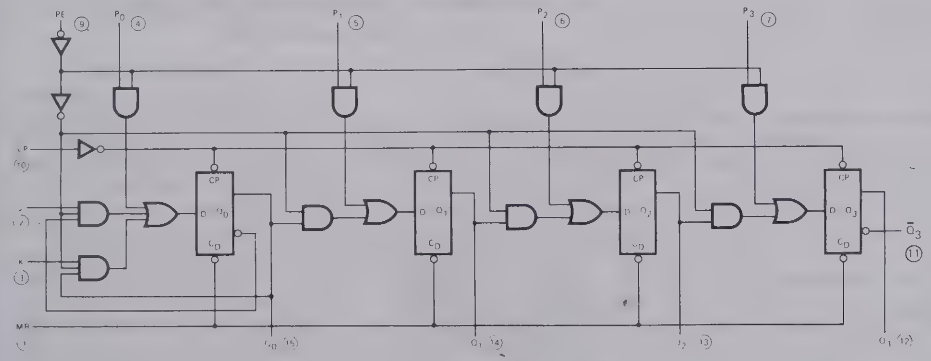
DESCRIPTION — The 9300 is a TTL/MSI 4-Bit Universal Shift Register. As a high speed multi-functional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. This new 9300 replaces the earlier 9300 device in all applications. All requirements of the original 9300 specification are satisified with the minimum shift rate of 15 MHz being improved to 30 MHz.

- 38 MHz TYPICAL SHIFT FREQUENCY
- ASYNCHRONOUS COMMON RESET
- J, $\overline{K}$ INPUTS TO FIRST STAGE
- SYNCHRONOUS PARALLEL ENTRY
- TYPICAL POWER DISSIPATION OF 300 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- TTL COMPATIBLE

PIN NAMES		**LOADING** (Note a)
$\overline{PE}$	Parallel Enable (Active LOW) Input	2.3 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	1 U.L.
J	First Stage J (Active HIGH) Input	1 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	1 U.L.
CP	Clock (Active HIGH) Going Edge Input	2 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs (Note b)	6 U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note c)	8 U.L.

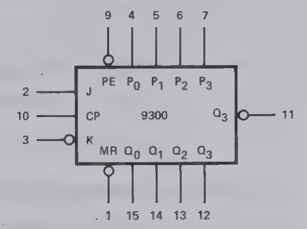
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 6 U.L. is the output LOW drive factor and 12 U.L. is the output HIGH drive factor.
c. 8 U.L. is the output LOW drive factor and 16 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM


PE ⑨
P0 ④
P1 ⑤
P2 ⑥
P3 ⑦
CP ⑩
J ②
K ③
MR ①
CP
D
Q0
CD
Q1
Q2
Q3
Q̄3 ⑪
Q0 ⑮
Q1 ⑭
Q2 ⑬
Q3 ⑫

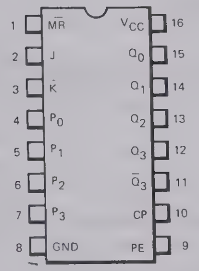
○ = Pin Numbers

LOGIC SYMBOL

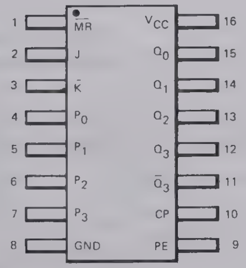

9
4
5
6
7
2
10
3
J
CP
K
PE
P0
P1
P2
P3
9300
Q̄3
11
MR
Q0
Q1
Q2
Q3
1
15
14
13
12

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 MR
2 J
3 K̄
4 P0
5 P1
6 P2
7 P3
8 GND
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 Q̄3
10 CP
9 PE

FLATPAK (TOP VIEW)


1 MR
2 J
3 K̄
4 P0
5 P1
6 P2
7 P3
8 GND
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 Q̄3
10 CP
9 PE

FUNCTIONAL DESCRIPTION — The logic diagram indicates the functional characteristics of the 9300 4-bit shift register. Several special logic features of the 9300 design which increase the range of useful application are:

1. A J$\overline{K}$ input is provided to the first flip-flop in the register. This type of input is the same as the more common JK input except that the LOW voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for most general applications. At the same time the simple D type input most appropriate for a shift register can be easily obtained by tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logic operation—except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the parallel enable input is LOW. With the parallel enable input LOW, the element appears as four common clocked D flip-flops. When the parallel enable is HIGH, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active HIGH output is provided for all four stages and an active LOW output is provided for the last stage.
6. A master asynchronous reset input allows the setting to zero of all stages independent of any other input condition.

TRUTH TABLES

TABLE I—SERIAL ENTRY

($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE III—PARALLEL ENTRY

($\overline{PE}$ = LOW, $\overline{MR}$ = HIGH)

D-Input (P_0, P_1, P_2 or P_3)	Output Q at t_{n+1} (Q_0, Q_1, Q_2 or Q_3)
L	L
H	H

TABLE II—SERIAL ENTRY

($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J&$\overline{K}$ Connected	Q_0 at t_{n+1}
L	L
H	H

TABLE IV—MODE SELECTION

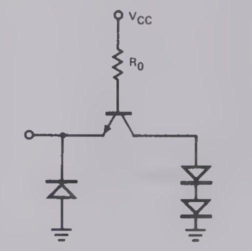
	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
Serial Entry	H	X	X	X	X	Refer to Table I & II		H
Parallel Entry	L	Refer to Table III				X	X	H

(n+1) = Indicates state after next clock

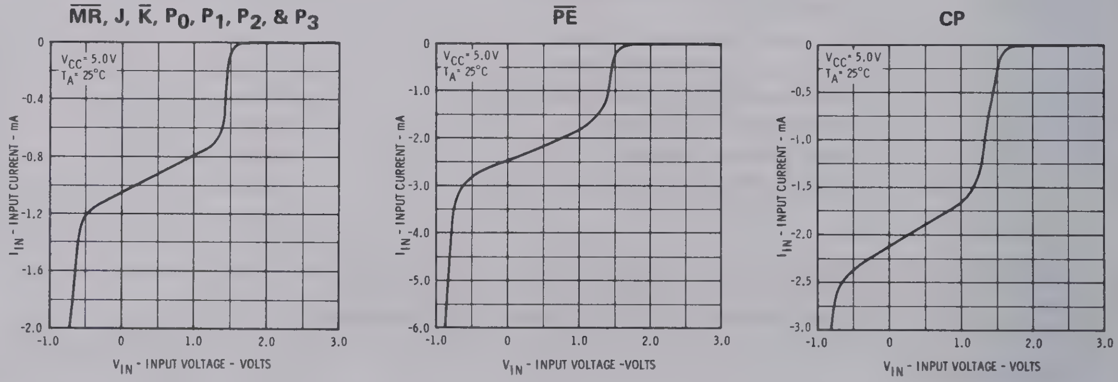
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE



$\overline{MR}$, J, $\overline{K}$, P_0, P_1, P_2, & P_3

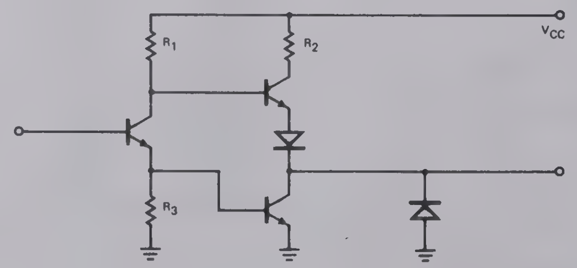
$\overline{PE}$

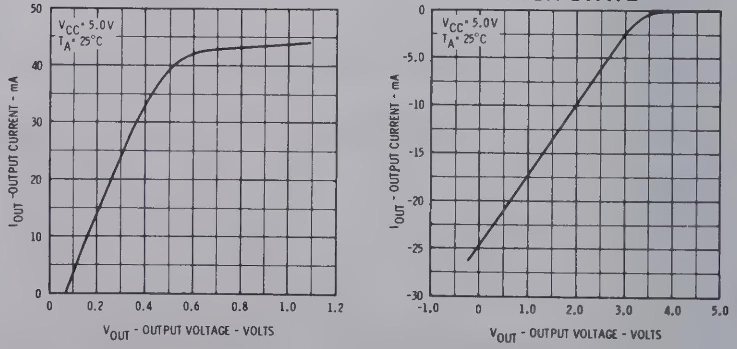
CP

OUTPUTS

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (Q_0, Q_1, Q_2, Q_3 AND $\overline{Q}_3$)

EQUIVALENT CIRCUIT





LOW STATE

HIGH STATE

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN.	TYP.	MAX.	
9300XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9300XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETERS	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP. (Note 4)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage for All Inputs	
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C	
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −640 µA for $\overline{Q}_3$, and −480 µA for Q_0–Q_3 V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 12.8 mA for $\overline{Q}_3$ and 9.6 mA for Q_0–Q_3 V_{IN} = V_{IH} or V_{IL} per Truth Table	
I_{IH}	Input HIGH Current						
	J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3		10	40			
	CP		20	80	µA	V_{CC} = MAX., V_{IN} = 2.4 V	
	$\overline{PE}$		23	92			
	Input HIGH Current, all inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current						
	J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3		−0.96	−1.6			
	CP		−1.92	−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
	$\overline{PE}$		−2.21	−3.7			
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−40	−80	mA	V_{CC} = MAX., V_{OUT} = 0 V	
I_{CC}	Power Supply Current		60	86	mA	9300XM	V_{CC} = MAX.
			60	92	mA	9300XC	Inputs HIGH

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
f_{sr}	Shift Right Frequency	30	38		MHz	See Fig. 1.	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH}	Turn Off Delay from Clock to Output		12	22	ns		
t_{PHL}	Turn On Delay from Clock to Output		19	26	ns		
t_{PHL} ($\overline{MR}$)	Turn On Delay from $\overline{MR}$ to OUTPUT (Except $\overline{Q}_3$)		26	37	ns	See Fig. 2.	

SWITCHING SET-UP REQUIREMENTS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{pw} (CP)	Clock Pulse Width	17	11		ns	See Fig. 1	$V_{CC} = 5.0$ V
t_s (Data)	Set-up Time Data to Clock	20	13		ns	See Fig. 3.	
t_h (Data)	Hold Time Data to Clock	0	−11		ns		
t_s ($\overline{PE}$)	Set-up Time $\overline{PE}$ to Clock	39	24		ns	See Fig. 4	
t_h ($\overline{PE}$)	Hold Time $\overline{PE}$ to Clock	−10	−20		ns		
t_{pw} ($\overline{MR}$)	Master Reset Pulse Width	25	13		ns	See Fig. 2.	
t_{rec} ($\overline{MR}$)	Recovery Time Master Reset to Clock	25	12		ns		

DEFINITION OF TERMS

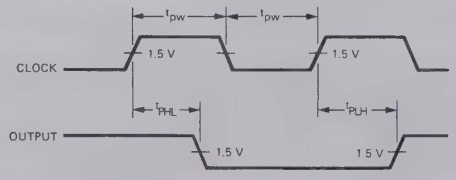
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the Reset pulse and the clock transistion from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SWITCHING TIME WAVEFORMS

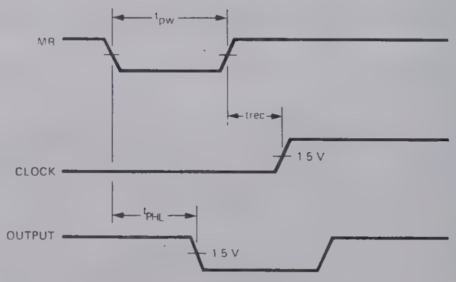
Clock to Output Delays and Clock Pulse Width.



OTHER CONDITIONS: J = $\overline{PE}$ = $\overline{MR}$ = H
$\overline{K}$ = L

Fig. 1.

Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time.

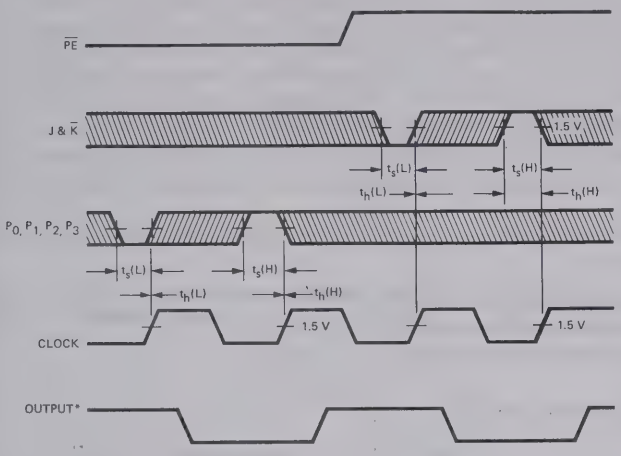


OTHER CONDITIONS: $\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3 = H$

Fig. 2.

SWITCHING TIME WAVEFORMS
(Cont't)

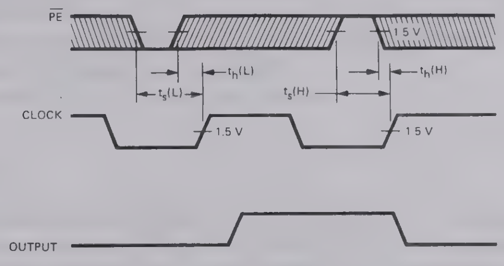
Set-up (t_s) and Hold (t_h) Time for Serial Data (J and $\overline{K}$) and Parallel Data (P_0, P_1, P_2 and P_3)


PE
J & K̄
1.5 V
t_s(L)
t_s(H)
t_h(L)
t_h(H)
P0, P1, P2, P3
t_s(L)
t_s(H)
t_h(L)
t_h(H)
1.5 V
1.5 V
CLOCK
OUTPUT*

OTHER CONDITIONS: $\overline{MR}$ = H
*J & $\overline{K}$ SET-UP TIME AFFECTS Q_0 ONLY

Fig. 3.

Set-up (t_s) and Hold (t_h) Time for $\overline{PE}$ Input.


PE
1.5 V
t_h(L)
t_h(H)
t_s(L)
t_s(H)
CLOCK
1.5 V
1.5 V
OUTPUT

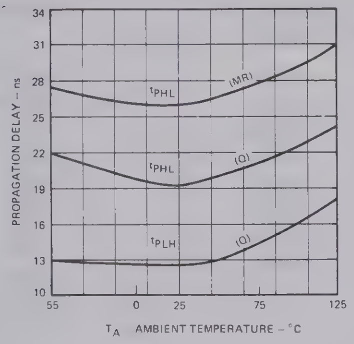
OTHER CONDITIONS: $\overline{MR}$ = H, J = $\overline{K}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 4.

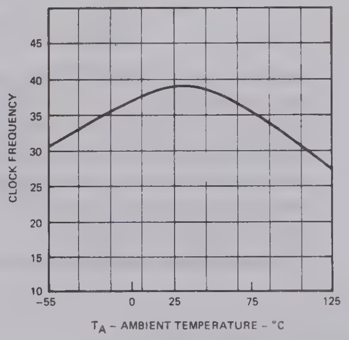
Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL SWITCHING CHARACTERISTICS

SWITCHING PERFORMANCE
CLOCK TO OUTPUT (Q_3) DELAY
AND MASTER RESET TO OUTPUT DELAY
VERSUS TEMPERATURE



CLOCK FREQUENCY
VERSUS
AMBIENT TEMPERATURE



TTL/MSI 93H00

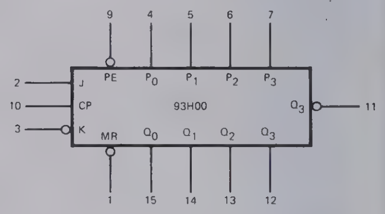
HIGH SPEED UNIVERSAL 4-BIT SHIFT REGISTER

DESCRIPTION — The 93H00 is a TTL/MSI 4-Bit Universal Shift Register offering a typical shift frequency to 55 MHz and guaranteed minimum value of 45 MHz. These features make the 93H00 useful in a wide range of high speed register and counter applications. These include serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data registers.

The 93H00 is pin compatible with the 9300 and 93L00 shift registers. Major electrical differences are the speed of operation and resulting power dissipation.

- **55 MHz TYPICAL SHIFT FREQUENCY**
- **ASYNCHRONOUS COMMON RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**
- **SYNCHRONOUS PARALLEL ENTRY**
- **TYPICAL POWER DISSIPATION OF 350 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **PIN FOR PIN COMPATIBLE WITH 9300A AND 93L00 DEVICES**

LOGIC SYMBOL


9
4
5
6
7
PE
P0
P1
P2
P3
2
J
10
CP
93H00
Q̄3
11
3
K
MR
Q0
Q1
Q2
Q3
1
15
14
13
12

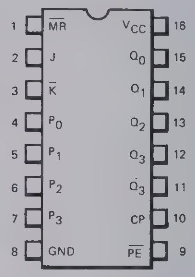
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES		**LOADING** (Note a)
$\overline{PE}$	Parallel Enable (Active LOW) Input	1 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	1 U.L.
J	First Stage J (Active HIGH) Input	1 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	1 U.L.
CP	Clock (Active HIGH) Going Edge Input	2 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs (Note b)	8 U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note b)	10 U.L.

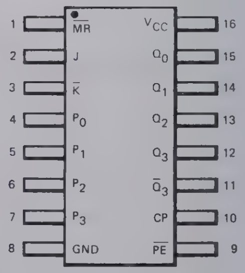
NOTES
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor

CONNECTION DIAGRAMS

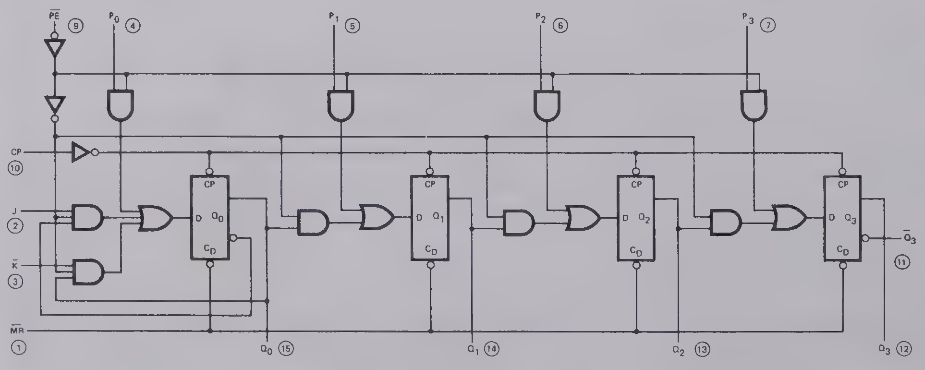
DIP (TOP VIEW)


1
MR
VCC
16
2
J
Q0
15
3
K
Q1
14
4
P0
Q2
13
5
P1
Q3
12
6
P2
Q̄3
11
7
P3
CP
10
8
GND
PE
9

FLATPAK (TOP VIEW)


1
MR
VCC
16
2
J
Q0
15
3
K
Q1
14
4
P0
Q2
13
5
P1
Q3
12
6
P2
Q̄3
11
7
P3
CP
10
8
GND
PE
9

LOGIC DIAGRAM


PE 9
P0 4
P1 5
P2 6
P3 7
CP 10
J 2
K 3
MR 1
CP
D
Q0
CD
Q1
Q2
Q3
Q̄3 11
Q0 15
Q1 14
Q2 13
Q3 12

○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The logic diagram indicates the functional characteristics of the 93H00 4-bit shift register. Special logic features of the 93H00 design which increase the range of application are described below:

1. A J$\overline{K}$ input is provided to the first flip-flop in the register. This type of input is the same as the more common JK input except that the LOW voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for most general applications. At the same time the simple D type input most appropriate for a shift register can be easily obtained by tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logic operation—except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is LOW. With the Parallel Enable input LOW, the element appears as four common clocked D flip-flops. When the Parallel Enable is HIGH, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active HIGH output is provided for all four stages and an active LOW output is provided for the last stage.
6. A master asynchronous reset input allows the setting to zero of all stages independent of any other input condition.

TRUTH TABLES

TABLE I — SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II — SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J&$\overline{K}$ Connected	Q_0 at t_{n+1}
L	L
H	H

TABLE III — PARALLEL ENTRY
($\overline{PE}$ = LOW, $\overline{MR}$ = HIGH)

D-Input (P_0, P_1, P_2 or P_3)	Output Q at t_{n+1} (Q_0, Q_1, Q_2 or Q_3)
L	L
H	H

(n+1) = Indicates state after next clock

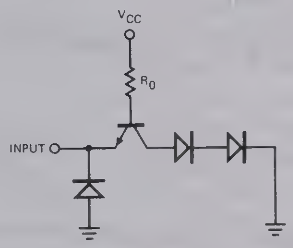
TABLE IV — MODE SELECTION

	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
Serial Entry	H	X	X	X	X	Refer to Table I & II		H
Parallel Entry	L	Refer to Table III				X	X	H

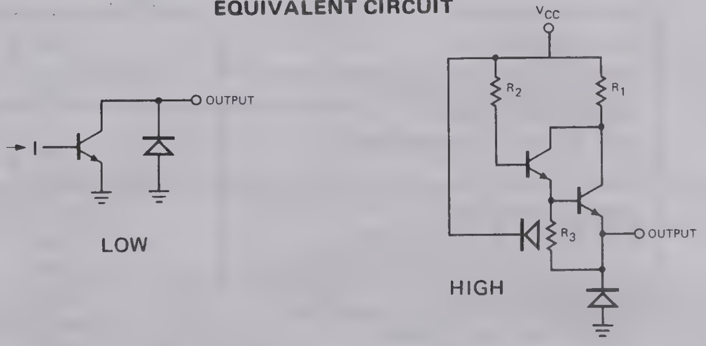
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT



OUTPUTS
EQUIVALENT CIRCUIT



LOW

HIGH

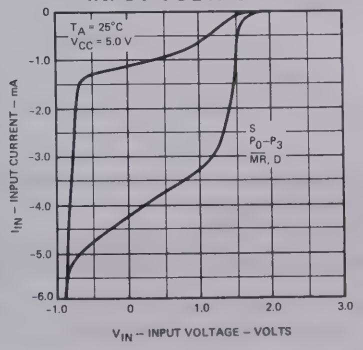


Fig. 1
INPUT CURRENT VERSUS INPUT VOLTAGE

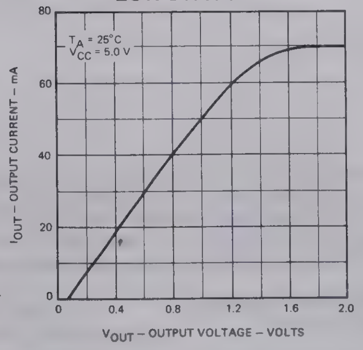


Fig. 2
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

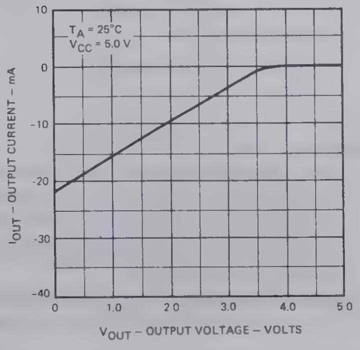


Fig. 3
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN.	TYP.	MAX.	
93H00XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93H00XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.64 mA (−0.8 mA, Pin 11) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 12.8 mA (16 mA, Pin 11) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.4 V
	J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3,$\overline{PE}$		−0.96	−1.6		
	CP		−1.92	−3.2		
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V
	J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3, $\overline{PE}$			40		
	CP			80		
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 5)	−30	−75	−100	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current 93H00XM		65	102	mA	V_{CC} = MAX.
	Power Supply Current 93H00XC		65	112		

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
f_{sr}	Shift Right Frequency	45	55		MHz	Fig. 4	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH}	Turn Off Delay from Clock to Output		10	16	ns		
t_{PHL}	Turn on Delay from Clock to Output		14.5	21	ns		
t_{PHL} ($\overline{MR}$)	Turn on Delay from $\overline{MR}$ to Output (Except $\overline{Q}_3$)		21	28	ns	Fig. 5	

SWITCHING SET-UP REQUIREMENTS ($T_A = 25°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
t_{pw} (CP)	Clock Pulse Width	12	9.0		ns	Fig. 4	$V_{CC} = 5.0$ V
t_s (Data)	Set-Up Time Data to Clock	12	6.0		ns	Fig. 6	
t_h (Data)	Hold Time Data to Clock	0	−5.0		ns		
t_s ($\overline{PE}$)	Set-Up Time $\overline{PE}$ to Clock	15	8.0		ns	Fig. 7	
t_h ($\overline{PE}$)	Hold Time $\overline{PE}$ to Clock	0	−7.0		ns		
t_{pw} ($\overline{MR}$)	Master Reset Pulse Width	19	11		ns	Fig. 5	
t_{rec} ($\overline{MR}$)	Recovery Time Master Reset to Clock	7.0	3.0		ns		

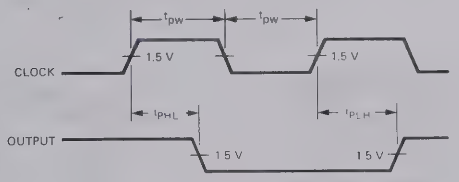
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

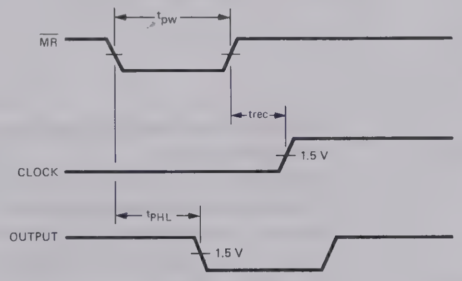
SWITCHING TIME WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



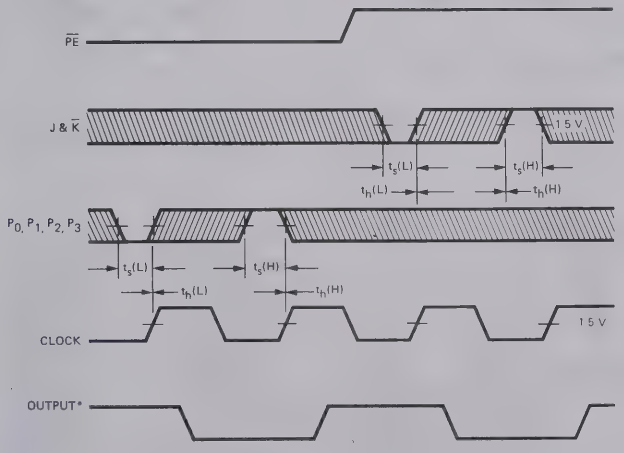
Other Conditions: $J = \overline{PE} = \overline{MR} = H$
$\overline{K} = L$

Fig. 4 – CLOCK TO OUTPUT DELAYS & CLOCK PULSE WIDTH



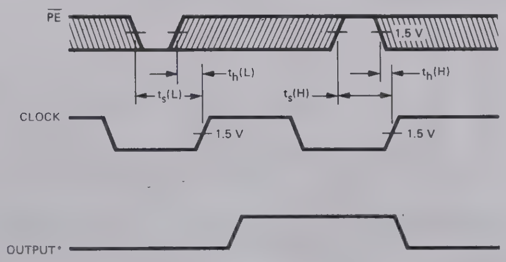
Other Conditions: $\overline{PE} = L$
$P_0 = P_1 = P_2 = P_3 = H$

Fig. 5 – MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Other Conditions: $\overline{MR} = H$
*J&$\overline{K}$ Set-Up Time Affects Q_0 Only

Fig. 6 – SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J&$\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



Other Conditions: $\overline{MR} = H$, $J = \overline{K} = L$
$P_0 = P_1 = P_2 = P_3 = H$
*t_s(H) and t_h(H) Affects Q_0 Only

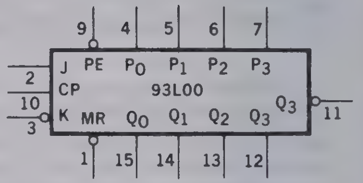
Fig. 7 – SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT

LPTTL/MSI 93L00
LOW POWER 4-BIT SHIFT REGISTER

DESCRIPTION — The LPTTL/MSI 93L00 4-Bit Shift Register is a medium speed multi-functional sequential logic block, useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTL technology for high speed and high fanout capability, and is compatible with the Fairchild TTL family.

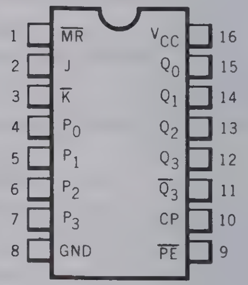
- 15 MHz TYPICAL SHIFT FREQUENCY
- ASYNCHRONOUS COMMON RESET
- J, $\overline{K}$ INPUTS TO FIRST STAGE
- SYNCHRONOUS PARALLEL ENTRY
- TYPICAL POWER DISSIPATION OF 75 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

LOGIC SYMBOL


9
4
5
6
7
J
PE
P0
P1
P2
P3
2
CP
93L00
10
3
K
MR
Q0
Q1
Q2
Q3
Q3
11
1
15
14
13
12

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)

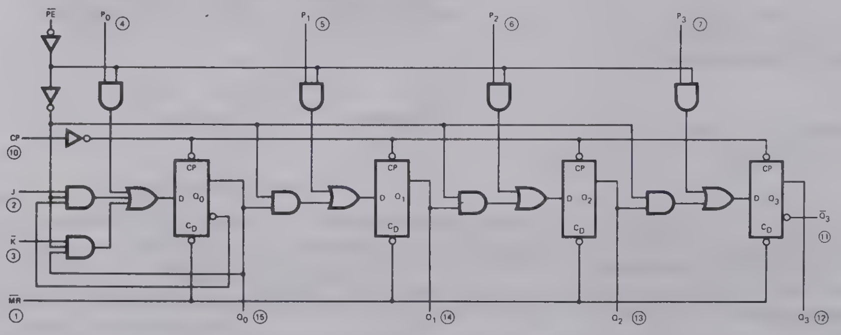

1 MR
2 J
3 K
4 P0
5 P1
6 P2
7 P3
8 GND
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 Q3
10 CP
9 PE

PIN NAMES

		LOADING	
		HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	1.15 U.L.	0.575 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	1.0 U.L.	0.5 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	8.0 U.L.	2.0 U.L.
$\overline{Q}_3$	Complementary Last Stage Output	8.0 U.L.	2.0 U.L.

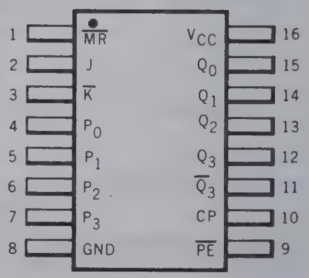
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM


PE
P0 4
P1 5
P2 6
P3 7
CP 10
J 2
K 3
MR 1
CP
D Q0
CD
CP
D Q1
CD
CP
D Q2
CD
CP
D Q3
CD
Q3 11
Q0 15
Q1 14
Q2 13
Q3 12

○ = PIN NUMBERS

FLATPAK (TOP VIEW)


1 MR
2 J
3 K
4 P0
5 P1
6 P2
7 P3
8 GND
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 Q3
10 CP
9 PE

FUNCTIONAL DESCRIPTION — The logic diagram indicates the functional characteristics of the 93L00 4-bit shift register. Special logic features of the 93L00 design increase the versatility of this shift register.

1. A $J\overline{K}$ input is provided to the first flip-flop in the register. This type of input is the same as the more common JK input except that the LOW voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for most general applications. At the same time the simple D type input most appropriate for a shift register can be easily obtained by tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logic operation—except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the parallel enable input is LOW. With the parallel enable input LOW, the element appears as four common clocked D flip-flops. When the parallel enable is HIGH, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active HIGH output is provided for all four stages and an active LOW output is provided for the last stage.
6. An asynchronous master reset input allows the setting to zero of all stages independent of any other input condition.

TRUTH TABLES

TABLE I — SERIAL ENTRY

($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE III — PARALLEL ENTRY

($\overline{PE}$ = LOW, $\overline{MR}$ = HIGH)

D-Input (P_0, P_1, P_2 or P_3)	Output Q at t_{n+1} (Q_0, Q_1, Q_2 or $\overline{Q}_3$)
L	L
H	H

(n+1 = Indicates state after next clock)

TABLE II — SERIAL ENTRY

($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J & $\overline{K}$ Connected	Q_0 at t_{n+1}
L	L
H	H

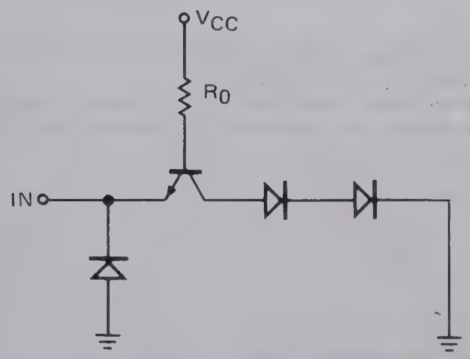
TABLE IV — MODE SELECTION

	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
Serial Entry	H	X	X	X	X	Refer to Table I & II		H
Parallel Entry	L	Refer to Table III				X	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TYPICAL INPUT AND OUTPUT CIRCUITS

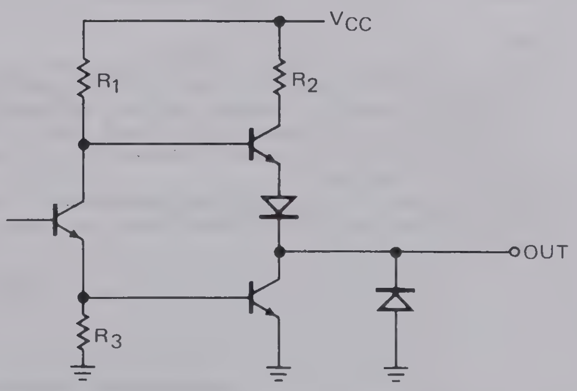
INPUTS EQUIVALENT CIRCUIT



TYPICAL RESISTORS

R_0 = 16 kΩ
R_1 = 6 kΩ
R_2 = 240 Ω
R_3 = 5 kΩ

OUTPUTS EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L00XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L00XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.3 V
	J, $\overline{K}$, $\overline{MR}$, P_0,P_1,P_2 & P_3		−0.25	−0.40		
	CP		−0.50	−0.80		
	$\overline{PE}$		−0.58	−0.92		
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V
	J, $\overline{K}$, $\overline{MR}$, P_0,P_1,P_2 & P_3		2.0	20		
	CP		4.0	40		
	$\overline{PE}$		5.0	46		
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		15	23	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
f_{sr}	Shift Right Frequency	10	17		MHz	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 1c)
t_{PLH}	Turn Off Delay		23	35	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 1a)
t_{PHL}	Turn On Delay		34	51	ns	
t_{PHL} ($\overline{MR}$)	Reset Time for $\overline{MR}$		55	83	ns	

SWITCHING SET-UP REQUIREMENTS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN	TYP	MAX			
t_{pw}CP	Clock Pulse Width	38	25		ns	Fig. 1c	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_s	Set-up Time	60	35		ns	Fig. 1a	
t_h	Hold Time	0	-22		ns		
t_s ($\overline{PE}$)	Set-up Time for $\overline{PE}$	68	45		ns	Fig. 1b	
t_h ($\overline{PE}$)	Hold Time for $\overline{PE}$	-20	-39		ns		
t_{rec} ($\overline{MR}$)	Recovery Time for $\overline{MR}$	70	45		ns	Fig. 1a	
$t_{pw}\overline{MR}$	Min Reset Pulse Width	53	35		ns		

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the flip-flop(s) to respond.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME FOR MR: $t_{rec}(\overline{MR})$ is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order for the flip-flop(s) to respond to the clock.

Fig. 1a

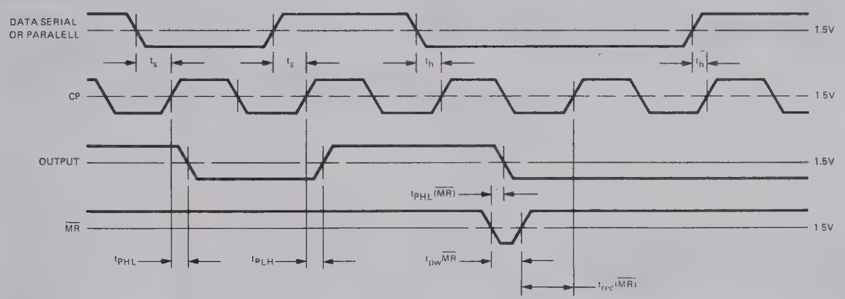

DATA SERIAL OR PARALELL
1.5V
ts
ts
th
th
CP
1.5V
OUTPUT
1.5V
tPHL(MR)
MR
1.5V
tPHL
tPLH
tpwMR
trec(MR)

Fig. 1b

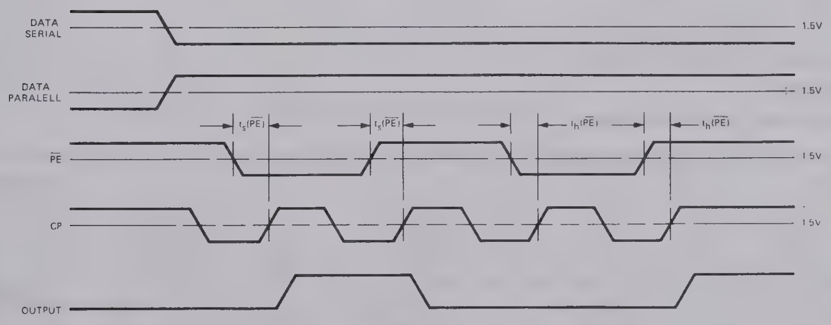
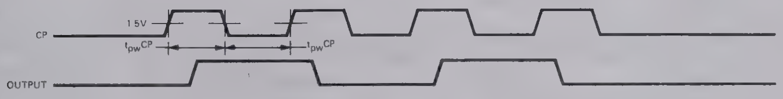

DATA SERIAL
1.5V
DATA PARALELL
1.5V
ts(PE)
ts(PE)
th(PE)
th(PE)
PE
1.5V
CP
1.5V
OUTPUT

Fig. 1c


1.5V
CP
tpwCP
tpwCP
OUTPUT

V_{OUT} Frequency = 1/2 X V_{IN} Frequency

J = HIGH, $\overline{K}$ = LOW, $\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH

Fig. 1 SWITCHING TIME & SHIFT RIGHT FREQUENCY WAVEFORM

TTL/MSI 93S00

4-BIT UNIVERSAL SHIFT REGISTER

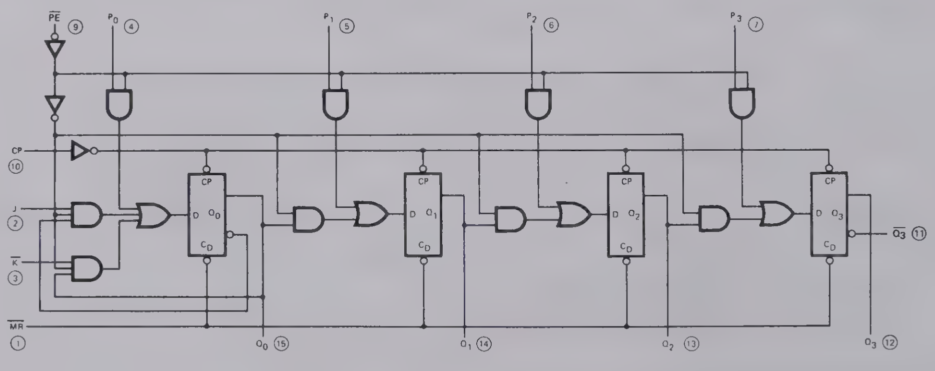
TO BE ANNOUNCED

DESCRIPTION — The 93S00 is a TTL/MSI super high speed 4-Bit Universal Shift Register. It utilizes Schottky clamped diode technology to achieve its super high speeds. As a high speed multi-functional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

- TYPICAL SHIFT RIGHT FREQUENCY OF 100 MHz
- ASYNCHRONOUS COMMON RESET
- J, $\overline{K}$ INPUTS TO FIRST STAGE
- SYNCHRONOUS PARALLEL ENTRY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

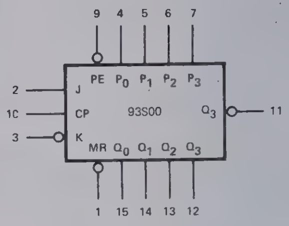
PIN NAMES	
$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0, P_1, P_2, P_3	Parallel Inputs
J	First Stage J (Active HIGH) Input
$\overline{K}$	First Stage K (Active LOW) Input
CP	Clock (Active HIGH) Going Edge Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOGIC DIAGRAM



PE 9
P0 4
P1 5
P2 6
P3 7
CP 10
J 2
K 3
MR 1
CP D Q0 CD
CP D Q1 CD
CP D Q2 CD
CP D Q3 CD
Q̄3 11
Q0 15
Q1 14
Q2 13
Q3 12
○ = Pin Numbers

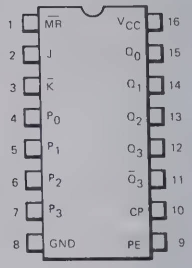
LOGIC SYMBOL



9 4 5 6 7
PE P0 P1 P2 P3
2 J
10 CP
3 K
93S00
Q̄3 11
MR Q0 Q1 Q2 Q3
1 15 14 13 12

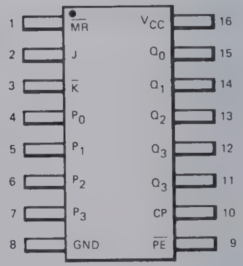
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 MR
2 J
3 K
4 P0
5 P1
6 P2
7 P3
8 GND
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 Q̄3
10 CP
9 PE

FLATPAK (TOP VIEW)



1 MR
2 J
3 K
4 P0
5 P1
6 P2
7 P3
8 GND
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 Q̄3
10 CP
9 PE

TTL/MSI 9301
ONE-OF-TEN DECODER

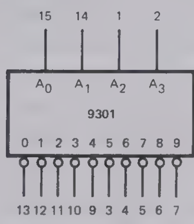
DESCRIPTION — The 9301 is a Multipurpose Decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTL for high speed and high fan out capability, and is compatible with all members of the Fairchild TTL family.

- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **GUARANTEED FANOUT OF 10 TTL LOADS OVER THE FULL TEMPERATURE RANGE AND SUPPLY VOLTAGE RANGES**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 145 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL AND TTL FAMILIES**
- **ALL CERAMIC "HERMETIC" 16 LEAD DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)
A_0, A_1, A_2, A_3	Address Inputs	1 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.

NOTES:
a. Unit Load (U.L.) = 40μA HIGH/1.6mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

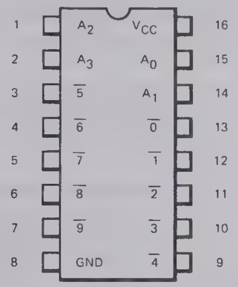
LOGIC SYMBOL



15
14
1
2
A0
A1
A2
A3
9301
0 1 2 3 4 5 6 7 8 9
13 12 11 10 9 3 4 5 6 7

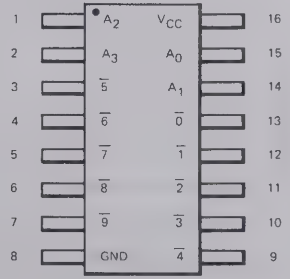
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



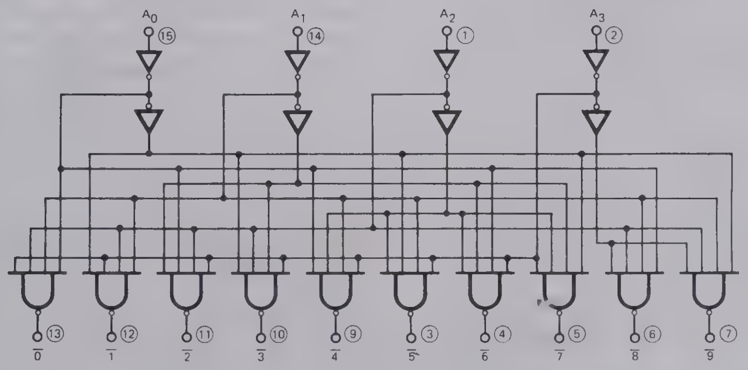
1 A2
2 A3
3 5̄
4 6̄
5 7̄
6 8̄
7 9̄
8 GND
16 VCC
15 A0
14 A1
13 0̄
12 1̄
11 2̄
10 3̄
9 4̄

FLATPAK (TOP VIEW)



1 A2
2 A3
3 5̄
4 6̄
5 7̄
6 8̄
7 9̄
8 GND
16 VCC
15 A0
14 A1
13 0̄
12 1̄
11 2̄
10 3̄
9 4̄

LOGIC DIAGRAM



A0 15
A1 14
A2 1
A3 2
13 0̄
12 1̄
11 2̄
10 3̄
9 4̄
3 5̄
4 6̄
5 7̄
6 8̄
7 9̄

○ = PIN NUMBER

FUNCTIONAL DESCRIPTION — The 9301 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by the logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW enables.

The logic design of the 9301 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the 9301 is used as a 1 of 8 decoder.

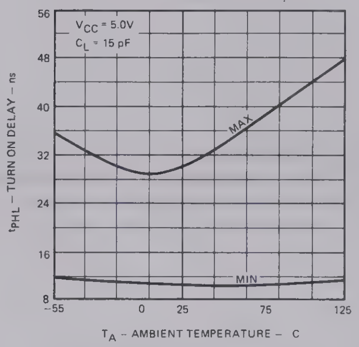
TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

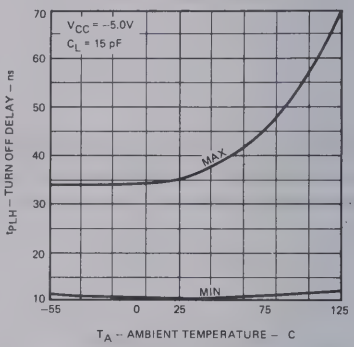
H = HIGH Voltage Level
L = LOW Voltage Level

SWITCHING PERFORMANCE

TYPICAL TURN ON DELAY VERSUS TEMPERATURE



TYPICAL TURN OFF DELAY VERSUS TEMPERATURE



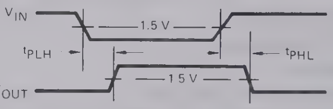
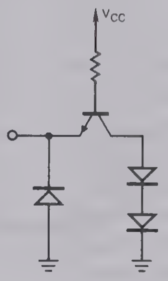


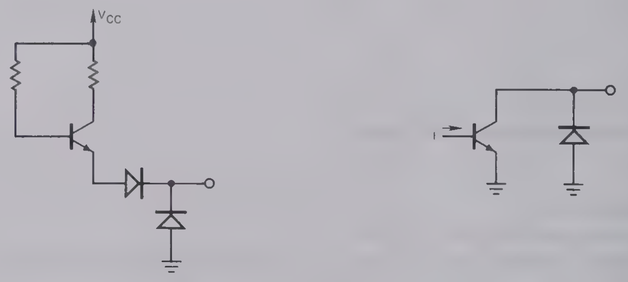
Fig. 1

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



OUTPUT HIGH

OUTPUT LOW

INPUT CURRENT VERSUS INPUT VOLTAGE

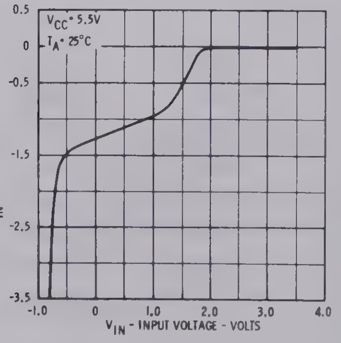


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH

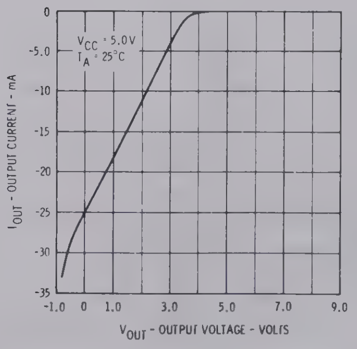


Fig. 3

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

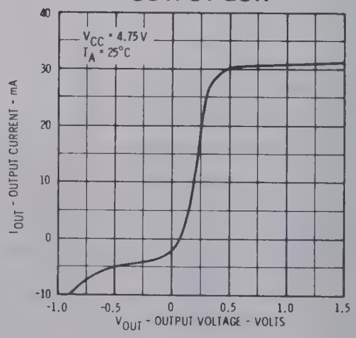


Fig. 4

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
*Input Voltage (dc)	−0.5V to +5.5V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
930IXM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
930IXC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC}= MIN, I_{IN} = −12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-20	-40	-70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		29	44	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0V, 25°C, and maximum loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		23	35	ns	V_{CC} = 5.0V
t_{PHL}	Turn On Delay Input to Output		20	30	ns	C_L = 15pF (See Fig. 1)

LPTTL/MSI 93L01

LOW POWER ONE-OF-TEN DECODER

DESCRIPTION – The LPTTL/MSI 93L01 is a Multipurpose Decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTL technology and is compatible with the Fairchild TTL family.

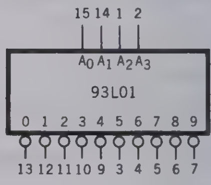
- MULTI-FUNCTION CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- DEMULTIPLEXING CAPABILITY
- TYPICAL PROPAGATION DELAY OF 63 ns
- TYPICAL POWER DISSIPATION OF 45 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

PIN NAMES

		LOADING	
		HIGH	LOW
A_0, A_1, A_2, A_3	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{9}$	Outputs (Active LOW)	10 U.L.	2.5 U.L.

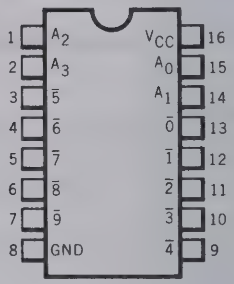
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC SYMBOL

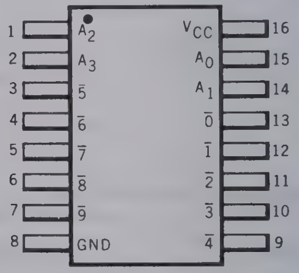

15 14 1 2
A_0 A_1 A_2 A_3
93L01
0 1 2 3 4 5 6 7 8 9
13 12 11 10 9 3 4 5 6 7

V_{CC} = PIN 16
GND = PIN 8

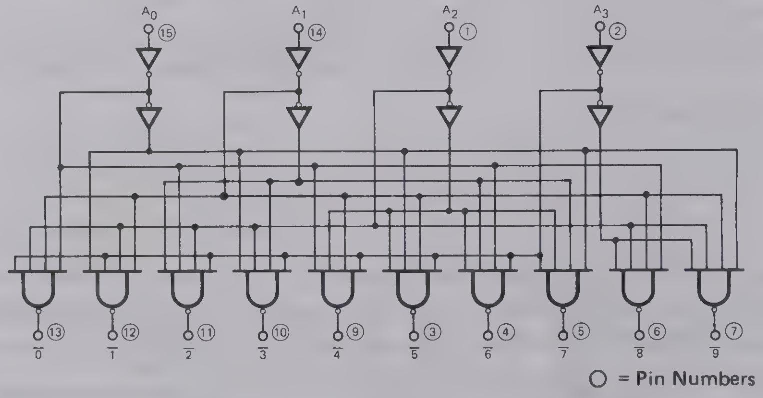
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 A_2
2 A_3
3 $\overline{5}$
4 $\overline{6}$
5 $\overline{7}$
6 $\overline{8}$
7 $\overline{9}$
8 GND
16 V_{CC}
15 A_0
14 A_1
13 $\overline{0}$
12 $\overline{1}$
11 $\overline{2}$
10 $\overline{3}$
9 $\overline{4}$

FLATPAK (TOP VIEW)


1 A_2
2 A_3
3 $\overline{5}$
4 $\overline{6}$
5 $\overline{7}$
6 $\overline{8}$
7 $\overline{9}$
8 GND
16 V_{CC}
15 A_0
14 A_1
13 $\overline{0}$
12 $\overline{1}$
11 $\overline{2}$
10 $\overline{3}$
9 $\overline{4}$

LOGIC DIAGRAM


A_0 ⑮
A_1 ⑭
A_2 ①
A_3 ②
⑬ $\overline{0}$
⑫ $\overline{1}$
⑪ $\overline{2}$
⑩ $\overline{3}$
⑨ $\overline{4}$
③ $\overline{5}$
④ $\overline{6}$
⑤ $\overline{7}$
⑥ $\overline{8}$
⑦ $\overline{9}$
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 93L01 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the 93L01 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the 93L01 is used as a 1-of-8 decoder.

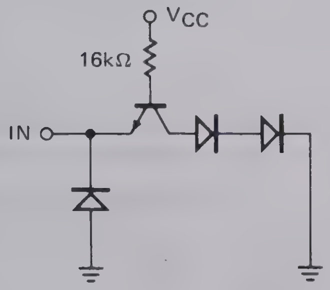
TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

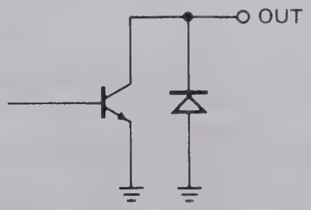
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

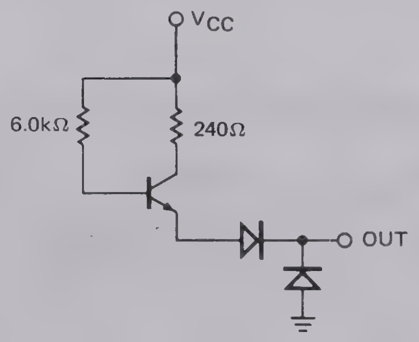


OUTPUTS
EQUIVALENT CIRCUITS

OUTPUT LOW



OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L01XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L01XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V (Note 5)
I_{CC}	Power Supply Current		9.0	13	mA	V_{CC} = MAX., Inputs at GND

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		32	50	ns	V_{CC} = 5.0 V See Fig. 1
t_{PHL}	Turn On Delay Input to Output		36	55	ns	C_L = 15 pF

SWITCHING TIME WAVEFORMS

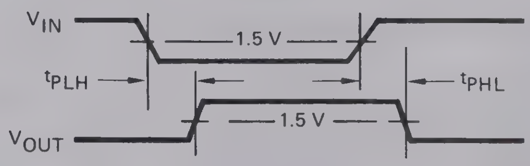


Fig. 1

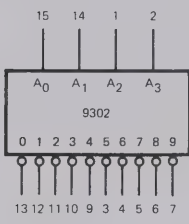
TTL/MSI 9302

ONE-OF-TEN DECODER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION – The 9302 is a multipurpose Decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The open collector outputs provide wired-OR capability which can be used for numerous summing, decoding and demultiplexing operations. The circuit uses TTL for high speed and high fan out capability, and is compatible with all members of the Fairchild TTL family.

- **OUTPUTS HAVE WIRED-OR CAPABILITY**
- **PROVIDES CAPABILITY TO GENERATE AND SUM MINTERMS OF 3 OR 4 VARIABLES**
- **ACTIVE LOW OUTPUTS ARE USEFUL FOR DRIVING LOW VOLTAGE LAMPS AND RELAYS**
- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 145 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**

LOGIC SYMBOL


15 14 1 2
A_0 A_1 A_2 A_3
9302
0 1 2 3 4 5 6 7 8 9
13 12 11 10 9 3 4 5 6 7

V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

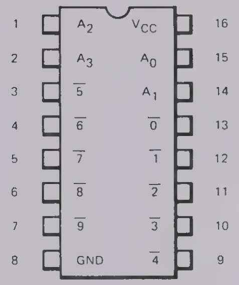
PIN NAMES		LOADING (Note a)
A_0, A_1, A_2, A_3	Address Inputs	1 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.

NOTES:

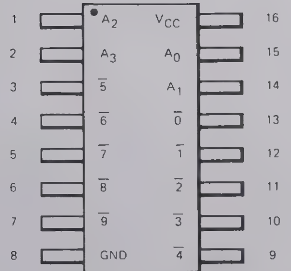
a. Unit Load (U.L.) = 40µA HIGH/1.6mA LOW

b. An external pull-up resistor is needed to provide HIGH level drive capability. The outputs will sink a maximum of 16mA at V_{OUT} = 0.4 V.

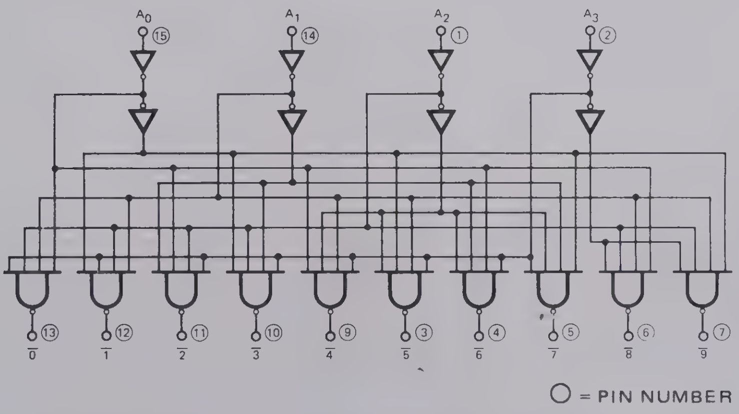
CONNECTION DIAGRAMS DIP (TOP VIEW)


1 A_2 V_{CC} 16
2 A_3 A_0 15
3 $\overline{5}$ A_1 14
4 $\overline{6}$ $\overline{0}$ 13
5 $\overline{7}$ $\overline{1}$ 12
6 $\overline{8}$ $\overline{2}$ 11
7 $\overline{9}$ $\overline{3}$ 10
8 GND $\overline{4}$ 9

FLATPAK (TOP VIEW)


1 A_2 V_{CC} 16
2 A_3 A_0 15
3 $\overline{5}$ A_1 14
4 $\overline{6}$ $\overline{0}$ 13
5 $\overline{7}$ $\overline{1}$ 12
6 $\overline{8}$ $\overline{2}$ 11
7 $\overline{9}$ $\overline{3}$ 10
8 GND $\overline{4}$ 9

LOGIC DIAGRAM


A_0 ⑮
A_1 ⑭
A_2 ①
A_3 ②
⑬ $\overline{0}$
⑫ $\overline{1}$
⑪ $\overline{2}$
⑩ $\overline{3}$
⑨ $\overline{4}$
③ $\overline{5}$
④ $\overline{6}$
⑤ $\overline{7}$
⑥ $\overline{8}$
⑦ $\overline{9}$
○ = PIN NUMBER

FUNCTIONAL DESCRIPTION — The 9302 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by the logic symbol. The open collector outputs provide easy summing of input terms. The 9302 provides the capability in one package to generate and sum any or all of the minterms of three variables, or the first 10-of-16 minterms of four variables.

The logic design of the 9302 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input (A_3) produces a useful inhibit function when the 9302 is used as a 1-of-8 decoder.

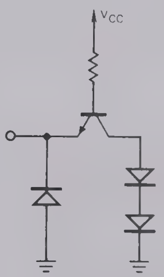
TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

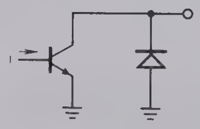
H = HIGH Voltage Level
L = LOW Voltage Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

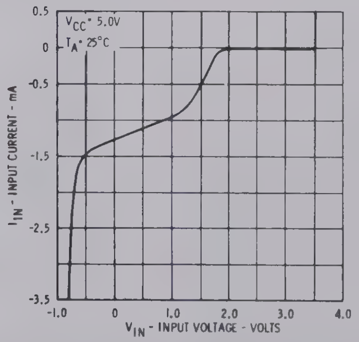
INPUT EQUIVALENT CIRCUIT



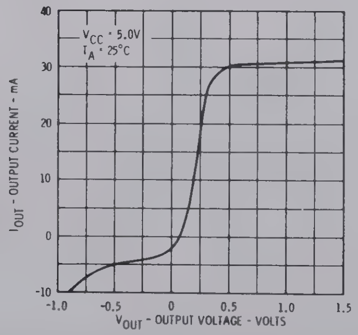
OUTPUT EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)	
Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
*Input Voltage (dc)	-0.5V to +5.5V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9302XM	4.5 V	5.0 V	5.5 V	-55°C to 125°C
9302XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC}= MIN, I_{IN} = -12mA, T_A = 25°C
I_{CEX}	Output HIGH Leakage Current			250	μA	V_{CC} = MIN., V_{CEX} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		-0.96	-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{CC}	Power Supply Current		29		mA	V_{CC} = MAX.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0V, 25°C, and maximum loading.

TTL/MSI 9304

DUAL FULL ADDER

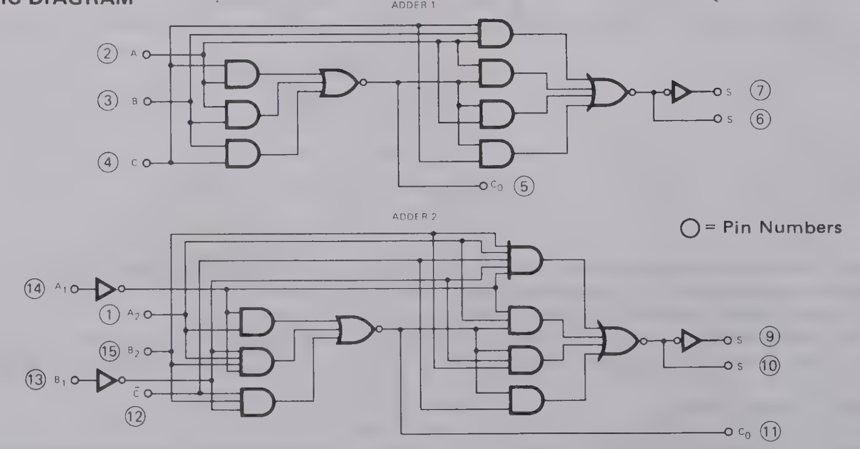
DESCRIPTION — The 9304 consists of two independent, high speed, binary Full Adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion and majority gating. The circuit uses TTL for high speed, high fanout operation and is compatible with all members of the Fairchild TTL family.

- MULTI-FUNCTION CAPABILITY
- 8ns CARRY PROPAGATION DELAY
- COMPLEMENTARY INPUTS AND OUTPUTS AVAILABLE
- TYPICAL POWER DISSIPATION OF 150 mW
- THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL AND TTL FAMILIES
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES		LOADING (Note a)
FULL ADDER 1		
A, B	Operand Inputs	4 U.L.
C	Carry Input	4 U.L.
S	Sum Output (Note c)	10 U.L.
$\overline{S}$	Complementary Sum Output (Note c)	10 U.L.
$\overline{C}_0$	Carry (Active LOW) Output (Note b)	7 U.L.
FULL ADDER 2		
A_1, B_1	OR Operand (Active HIGH) Input	1 U.L.
$\overline{A}_2$, $\overline{B}_2$	OR Operand (Active LOW) Input	4 U.L.
$\overline{C}$	Carry (Active LOW) Input	4 U.L.
S	Sum Output (Note c)	10 U.L.
$\overline{S}$	Complementary Sum Output (Note c)	10 U.L.
C_0	Carry (Active HIGH) Output (Note b)	7 U.L.

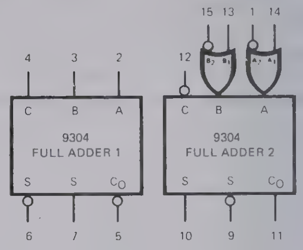
NOTES:
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.
b. 7 U.L. is the output LOW drive factor and 14 U.L. is the output HIGH drive factor.
c. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM


ADDER 1
② A
③ B
④ C
S ⑦
S ⑥
C0 ⑤
ADDER 2
⑭ A1
① A2
⑮ B2
⑬ B1
C ⑫
S ⑨
S ⑩
C0 ⑪

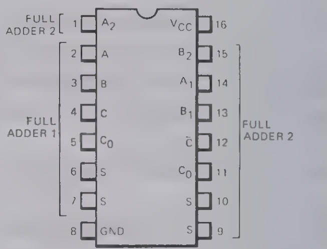
○ = Pin Numbers

LOGIC SYMBOL

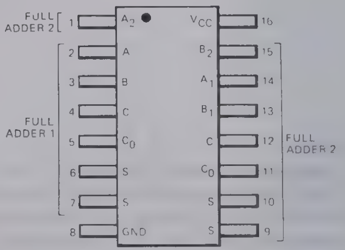

4 3 2
C B A
9304
FULL ADDER 1
S S C0
6 7 5
15 13 1 14
12
B2 B1 A2 A1
C B A
9304
FULL ADDER 2
S S C0
10 9 11

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)


FULL ADDER 2
FULL ADDER 1
FULL ADDER 2
1 A2
2 A
3 B
4 C
5 C0
6 S
7 S
8 GND
16 VCC
15 B2
14 A1
13 B1
12 C
11 C0
10 S
9 S

FLATPAK (TOP VIEW)


FULL ADDER 2
FULL ADDER 1
FULL ADDER 2
1 A2
2 A
3 B
4 C
5 C0
6 S
7 S
8 GND
16 VCC
15 B2
14 A1
13 B1
12 C
11 C0
10 S
9 S

FUNCTIONAL DESCRIPTION – The Fairchild 9304 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active HIGH or active LOW inputs at the A and B terminals. The adders produce a LOW carry and both LOW and HIGH sum with active HIGH inputs, a HIGH carry and both HIGH and LOW sum when active LOW inputs are used. This principle of duality is shown below, where the adders are drawn as functional blocks.

TRUTH TABLES

ADDER 1

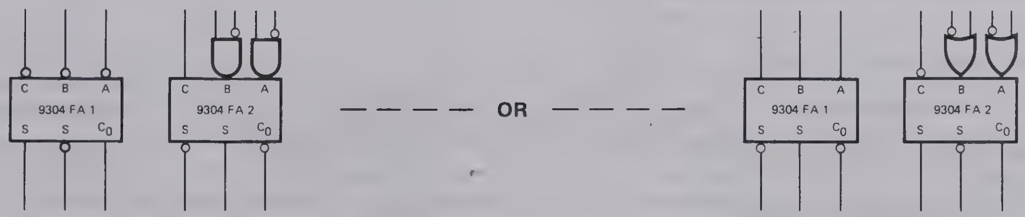
INPUTS			OUTPUTS		
C	B	A	$\overline{C}_0$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

ADDER 2

INPUTS					OUTPUTS		
$\overline{C}$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_0	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

FUNCTIONAL BLOCK REPRESENTATION



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
*Input Voltage (dc)	–0.5V to +5.5V
*Input Current (dc)	–30mA to +5.0mA
Voltage Applied to Outputs (Output HIGH)	–0.5V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN.	TYP.	MAX.	
9304XM	4.5 V	5.0 V	5.5 V	-55°C to 125°C
9304XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage For All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage For All Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_{IN} = –12 mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	I_{OH} = –560μA (Pins 5 & 11) V_{CC} = MIN., I_{OH} = –800μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	I_{OL} = 11.2mA (Pins 5 & 11) V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current A_1 & B_1 (Pins 14 & 13) Other Inputs		 10 40	 40 160	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current A_1 & B_1 (Pins 14 & 13) Other Inputs		 -0.96 -3.84	 -1.6 -6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-30	-60	-100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current			55	mA	V_{CC} = MAX., Pins 13 & 14 = 0.0 V

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0V, 25°C, and maximum loading.

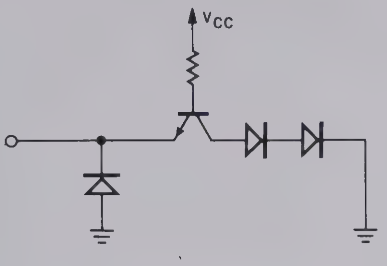
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETERS	9304XM			9304XC			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output A_1 to $\overline{S}$		28	40		28	45	ns	V_{CC} = 5.0 V C_L = 15pF See Fig. B
t_{PHL}	Turn On Delay Input to Output A_1 to $\overline{S}$		25	35		25	40	ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

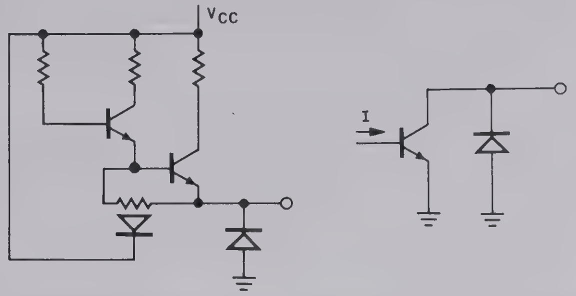
INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUIT

OUTPUT HIGH

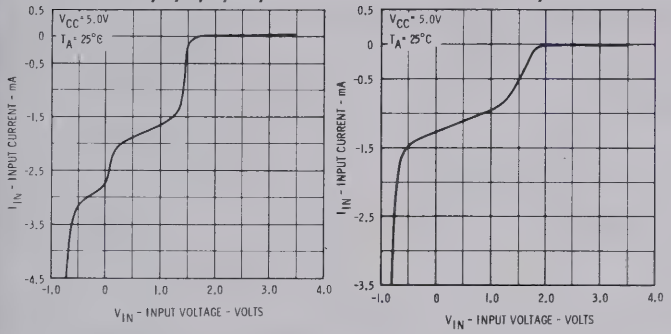
OUTPUT LOW



INPUT CURRENT VERSUS INPUT VOLTAGE

PINS 1, 2, 3, 4, 12, 15

PINS 13, 14



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

HIGH STATE

LOW STATE

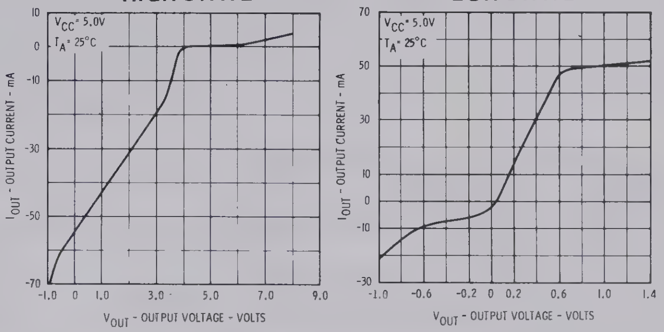
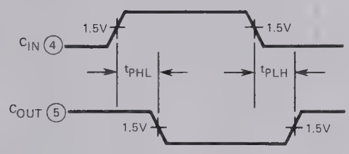
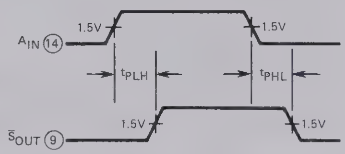


Fig. A

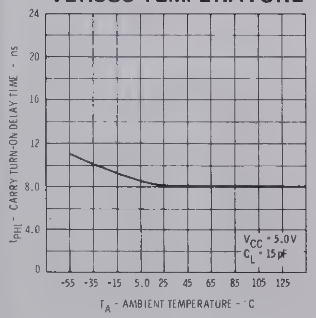
SWITCHING CHARACTERISTICS


CIN ④
COUT ⑤
1.5V
1.5V
tPHL
tPLH
1.5V
1.5V

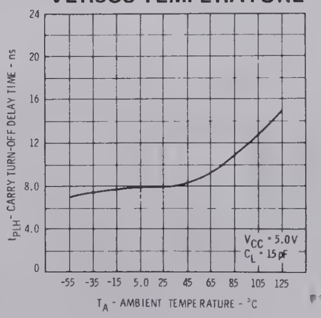
Note: ○ = PIN NUMBER


AIN ⑭
S̄OUT ⑨
1.5V
1.5V
tPLH
tPHL
1.5V
1.5V

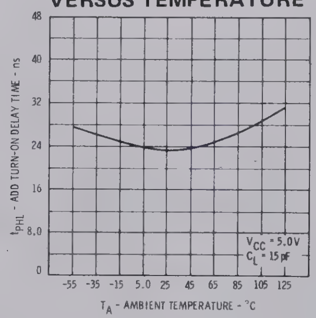
TYPICAL CARRY TURN ON DELAY TIME VERSUS TEMPERATURE



TYPICAL CARRY TURN OFF DELAY TIME VERSUS TEMPERATURE



TYPICAL ADD TURN ON DELAY TIME VERSUS TEMPERATURE



TYPICAL ADD TURN OFF DELAY TIME VERSUS TEMPERATURE

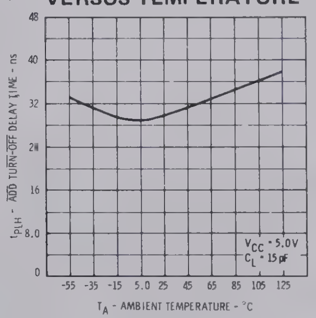


Fig. B

TTL/MSI 9305

VARIABLE MODULO COUNTER

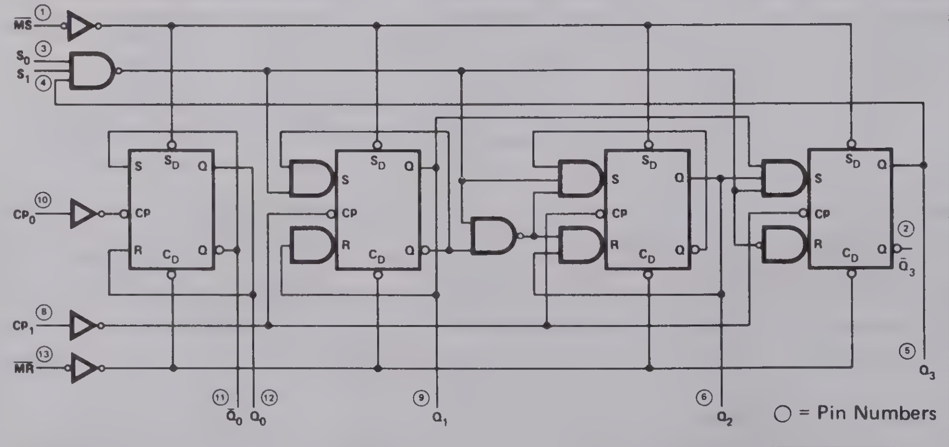
DESCRIPTION – The TTL/MSI 9305 is a monolithic, high speed, Variable Modulo Counter circuit, constructed with the Fairchild Planar* epitaxial process. It is a semisynchronous counter which can be programmed without extra logic to provide division or counting by either 2 and 4, 5, 6, 7, 8, or 10, 12, 14, 16. A binary count sequence can be obtained for all of the preceding counter modulos as well as 50% duty cycle output for dividers of 8, 10, 12, 14, 16. The device also features asynchronous overriding master reset and set inputs and the negation output of the final flip-flop output which allows the cascading of stages. The circuit uses TTL for high speed, high fanout operation and is compatible with all other members of the TTL family of digital integrated circuits.

- **VARIOUS BINARY COUNTING MODES**
  - **–MODULO 2 AND MODULO 5, 6, 7, 8**
  - **–MODULO 10 (8421 BCD), 12, 14, 16**
- **VARIOUS FREQUENCY DIVISION MODES WITH 50% DUTY CYCLE OUTPUT**
  - **–MODULO 8, 10, 12, 14, 16**
- **LOGIC SELECTION OF COUNTING MODE**
- **ASYNCHRONOUS MASTER RESET AND SET INPUTS**
- **MULTISTAGE COUNTING OPERATION**
- **TTL COMPATIBLE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)
S_0, S_1	Select Inputs	1 U.L.
CP_0	First Stage Clock Active HIGH Going Edge Input	1 U.L.
CP_1	Three Stage Clock Active HIGH Going Edge Input	1 U.L.
$\overline{MS}$	Master Set (Active LOW) Input	1 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0	First Stage Output (Note b)	8 U.L.
$\overline{Q}_0$	Complementary First Stage Output (Note b)	8 U.L.
Q_1, Q_2, Q_3	Three Stage Counter Outputs (Note b)	8 U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note c)	10 U.L.

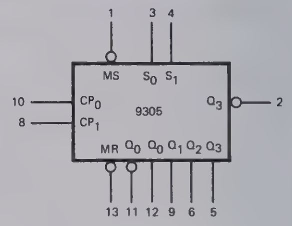
NOTES:
(a) 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
(b) 8 U.L. is the output LOW drive factor and 16 U.L. is the output HIGH drive factor.
(c) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



MS ①
S0 ③
S1 ④
CP0 ⑩
CP1 ⑧
MR ⑬
S
SD
Q
CP
R
CD
⑪ Q̄0
⑫ Q0
⑨ Q1
⑥ Q2
⑤ Q3
② Q̄3
○ = Pin Numbers

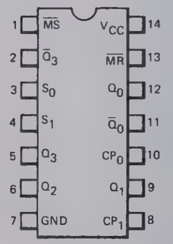
LOGIC SYMBOL



1
3
4
MS
S0
S1
10
CP0
8
CP1
9305
Q̄3
2
MR
Q̄0
Q0
Q1
Q2
Q3
13
11
12
9
6
5

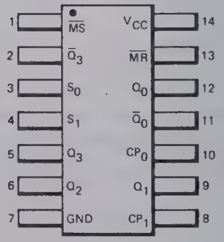
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 MS
2 Q̄3
3 S0
4 S1
5 Q3
6 Q2
7 GND
14 VCC
13 MR
12 Q0
11 Q̄0
10 CP0
9 Q1
8 CP1

FLATPAK (TOP VIEW)



1 MS
2 Q̄3
3 S0
4 S1
5 Q3
6 Q2
7 GND
14 VCC
13 MR
12 Q0
11 Q̄0
10 CP0
9 Q1
8 CP1

*Planar is a patented Fairchild process.

FUNCTIONAL DESCRIPTION — The MSI 9305 consists of four master-slave flip-flops which are separated into two functional units — a single toggle stage and a three stage synchronous counter. All four flip-flops change state on the LOW to HIGH transition of the clock. The three stage counter can be programmed with external connections as shown in the table below to provide modulo of either 5, 6, 7 or 8. This basic configuration allows synchronous binary counting by the last three stages and independent modulo 2 operation with the first single stage.

A four stage binary counter with a modulo of 10, 12, 14 or 16 is obtained by applying the incoming clock to the single toggle stage and feeding its negation output to the clock input of the three stage counter. A 4-stage divider with 50% duty cycle output is produced by feeding the incoming clock to the three stage counter and clocking the single stage with the $\overline{Q}_3$ output. In either the binary or 50% division mode the modulo (10, 12, 14, 16) is determined by the external programming connections for the three stage counter. These 4-stage counters or dividers are not fully synchronous (semisynchronous) but have only one flip-flop ripple delay in either configuration. Counter modulos other than 10, 12, 14, 16 can be formed with a few extra gates.

Several 9305 variable modulo counters programmed in any modulo can be connected together without extra logic to form asynchronous (ripple) type multistage counters. This is done by connecting the $\overline{Q}_3$ output of the less significant counter to the clock input of the following counter.

The Master Set and Reset will asynchronously set or reset all four stages when activated. The active LOW Reset input when LOW will clear the counter, overriding the clock and forcing the outputs (Q_{0-3}) LOW and outputs $\overline{Q}_0$, $\overline{Q}_3$ HIGH. The active LOW Set input when LOW will preset the counter, overriding the clock and forcing the outputs Q_{0-3} HIGH and outputs $\overline{Q}_0$, $\overline{Q}_3$ LOW. The master set provides a synchronous clear, since the first clock pulse following the asynchronous master set will reset all stages. This action is independent of the modulo programmed.

COUNTING MODE

The following are rules specifying the external connections required for various counter and divider modulos.

ASYNCHRONOUS MODE

$\overline{MS}$	$\overline{MR}$	Q_0	$\overline{Q}_0$	Q_1	Q_2	Q_3	$\overline{Q}_3$
L	H	H	L	H	H	H	L
H	L	L	H	L	L	L	H
H	H	COUNT*					

*As determined by programming connections.

PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

S_0	S_1	MODULO
NC	NC	5
Q_1	NC	6
NC	Q_1	6
Q_2	NC	7
NC	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

NC = Not Connected

ALTERNATE** PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

S_0	S_1	MODULO
Q_3	Q_3	5
Q_1	Q_1	6
Q_2	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

**The alternate programming connections program the counter and conveniently terminate unused select inputs (NC). Since these inputs form the inputs to a single NAND gate (see logic diagram), their connection to the counter outputs for the various count modulos provides the following output drive:

MODULO	OUTPUT	AVAILABLE OUTPUT FANOUT
5	Q_3	14/8
6	Q_1	14/7
7	Q_2	14/7
8	Q_1	15/7
8	Q_2	15/7

CONNECTIONS FOR MODULO 10, 12, 14, 16 BINARY COUNTERS AND 50% DUTY CYCLE DIVIDERS

For Binary Counting $\overline{Q}_0$ connected to CP_1 Incoming clock to CP_0
For 50% Duty Cycle Output $\overline{Q}_3$ connected to CP_0 Incoming Clock to CP_1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9305XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9305XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	I_{OH} = −800 μA (Pin 2) V_{CC} = MIN., I_{OH} = −640 μA V_{IN} = V_{IH} or V_{IL} per Mode Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	I_{OL} = 16 mA (Pin 2) V_{CC} = MIN., I_{OL} = 12.8 mA V_{IN} = V_{IH} or V_{IL} per Mode Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−30	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		42	66	mA	V_{CC} = MAX.

NOTES:

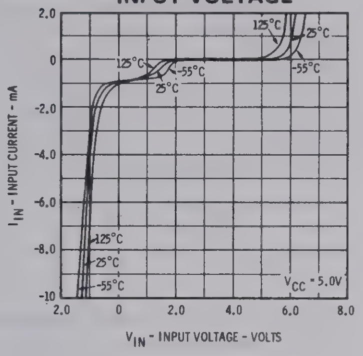
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

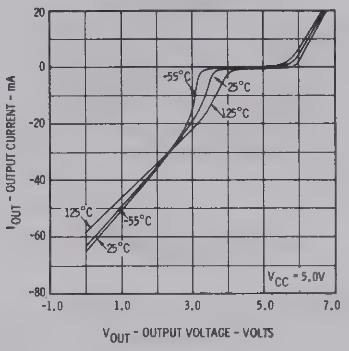
SYMBOL	PARAMETER	9305XM			9305XC			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
f_{COUNT}	Input Count Frequency	20	26		20	26		MHz	V_{CC} = 5.0 V, C_L = 15 pF Modulo 16 (S_0 to Q_1, S_1 to Q_2, $\overline{Q}_0$ to CP_1) Input CP_0
t_{PLH}	Turn-Off Delay Input to Output (CP_0 to Q_3, Modulo 16 Connection)		48	57		48	62	ns	
t_{PHL}	Turn-On Delay Input to Output (CP_0 to Q_3, Modulo 16 Connection)		44	53		44	58	ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

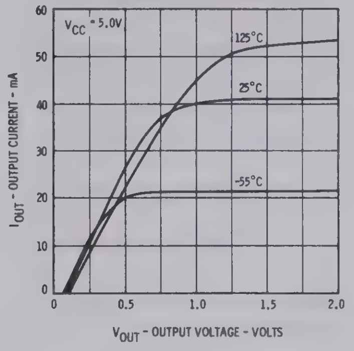
INPUT CURRENT VERSUS INPUT VOLTAGE



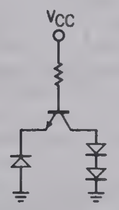
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



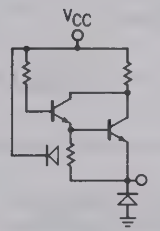
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



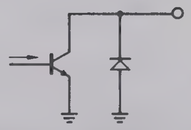
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)

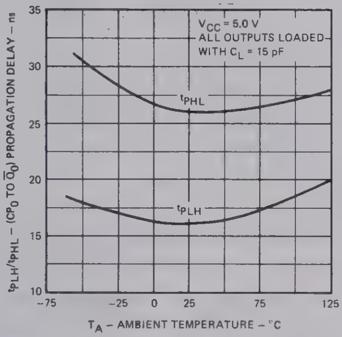


OUTPUT EQUIVALENT CIRCUIT (Output LOW)

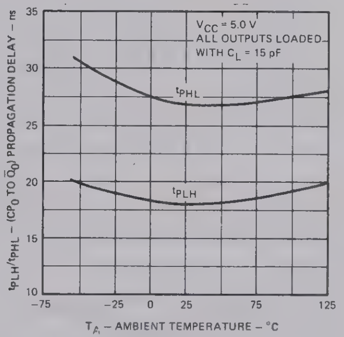


SWITCHING CHARACTERISTICS

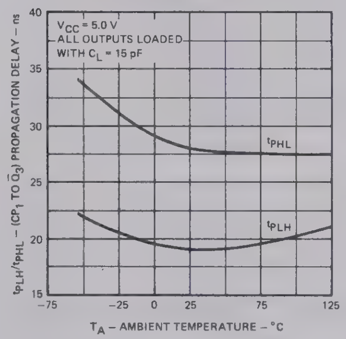
TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE CP_0 TO Q_0 MODULO 16

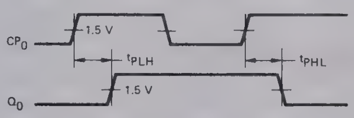


TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE CP_0 TO $\overline{Q}_0$ MODULO 16



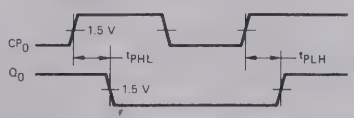
TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE CP_1 TO Q_3 MODULO 8





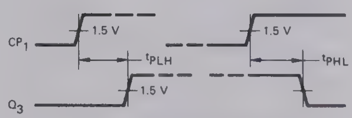
CP_0
1.5 V
t_{PLH}
t_{PHL}
1.5 V
Q_0

PIN 3 TO PIN 9, PIN 4 TO PIN 6
PIN 8 TO PIN 11, OTHERS OPEN



CP_0
1.5 V
t_{PHL}
t_{PLH}
Q_0
1.5 V

PIN 3 TO PIN 9, PIN 4 TO PIN 6
PIN 8 TO PIN 11, OTHERS OPEN

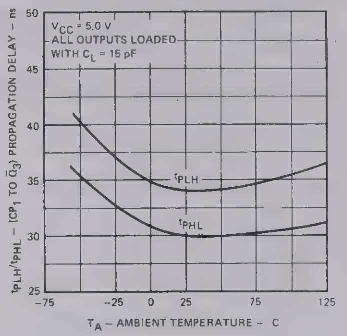


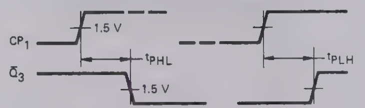
CP_1
1.5 V
1.5 V
t_{PLH}
t_{PHL}
1.5 V
Q_3

PIN 3 TO PIN 9, PIN 4 TO PIN 6
OTHERS OPEN

SWITCHING CHARACTERISTICS (Continued)

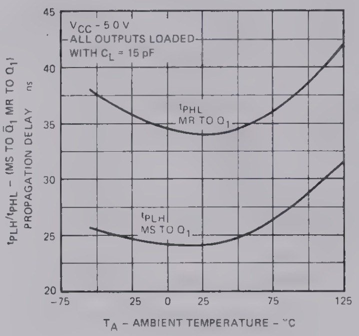
TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE CP_1 TO $\overline{Q}_3$ MODULO

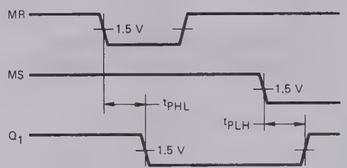



CP_1
1.5 V
t_{PHL}
t_{PLH}
$\overline{Q}_3$
1.5 V

PIN 3 TO PIN 9, PIN 4 TO PIN 6
OTHERS OPEN

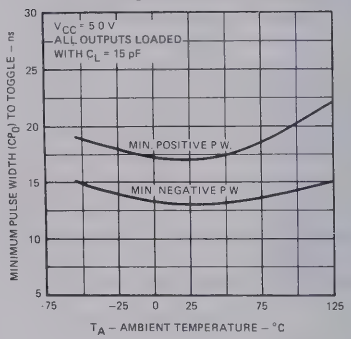
TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE t_{PLH} $\overline{MS}$ TO Q_1 t_{PHL} $\overline{MR}$ TO Q_1 MODULO 8

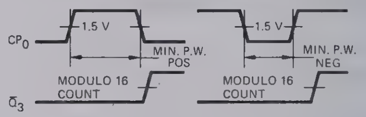



$\overline{MR}$
1.5 V
$\overline{MS}$
1.5 V
t_{PHL}
t_{PLH}
Q_1
1.5 V

PIN 3 TO PIN 9, PIN 4 TO PIN 6
OTHERS OPEN

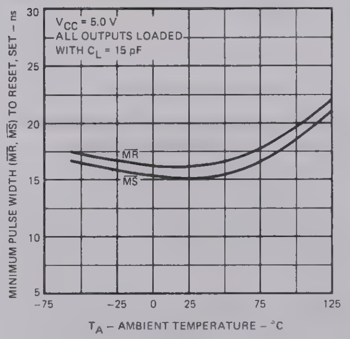
TYPICAL MINIMUM PULSE WIDTH TO TOGGLE VERSUS TEMPERATURE CP_0 MODULO 16

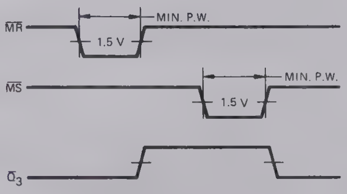



CP_0
1.5 V
MIN. P.W. POS
1.5 V
MIN. P.W. NEG
MODULO 16 COUNT
MODULO 16 COUNT
$\overline{Q}_3$

PIN 3 TO PIN 9, PIN 4 TO PIN 6
PIN 8 TO PIN 11, OTHERS OPEN

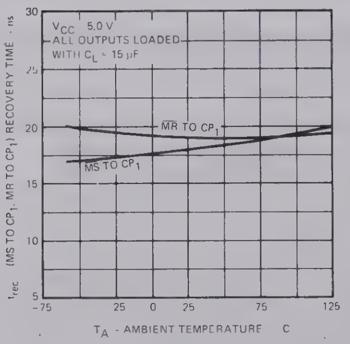
TYPICAL MINIMUM PULSE WIDTH TO RESET, SET VERSUS TEMPERATURE $\overline{MR}$, $\overline{MS}$ MODULO 16

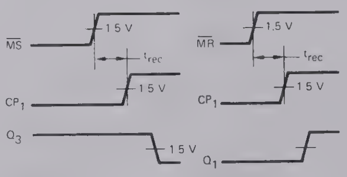



$\overline{MR}$
MIN. P.W.
1.5 V
$\overline{MS}$
MIN. P.W.
1.5 V
$\overline{Q}_3$

PIN 3 TO PIN 9, PIN 4 TO PIN 6
PIN 8 TO PIN 11, OTHERS OPEN

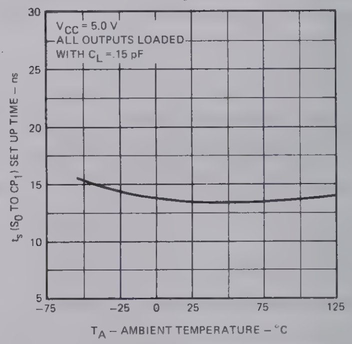
TYPICAL RECOVERY TIME VERSUS TEMPERATURE $\overline{MS}$ TO CP_1, $\overline{MR}$ TO CP_1 MODULO 8

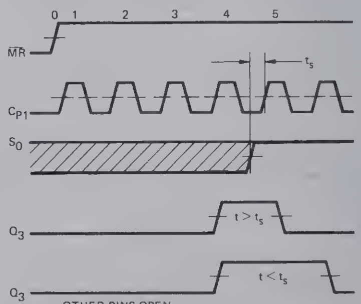



$\overline{MS}$
1.5 V
t_{rec}
CP_1
1.5 V
Q_3
1.5 V
$\overline{MR}$
1.5 V
t_{rec}
CP_1
1.5 V
Q_1

PIN 3 TO PIN 9, PIN 4 TO PIN 6
OTHERS OPEN

TYPICAL SET-UP TIME VERSUS TEMPERATURE S_0 TO CP_1 MODULO 6




0
1
2
3
4
5
$\overline{MR}$
t_s
CP_1
S_0
Q_3
$t > t_s$
Q_3
$t < t_s$

OTHER PINS OPEN

t_s is the time required that S_0 must go HIGH before CP_1 clock goes HIGH, such that the circuit recognizes the S_0 as being HIGH. The graph above indicates that times greater than t_s will result in Modulo 5 operation, and that values less than t_s will result in Modulo 6 operation. The shaded area indicates when the input is permitted to change for predictable output performance.

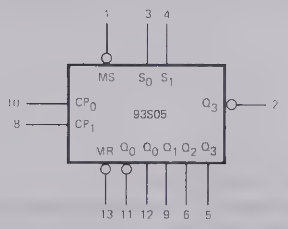
t_{rec} is the time that the $\overline{MR}$ (or $\overline{MS}$) must go HIGH before the clock (CP_1) goes HIGH such that the circuit recognizes the clock (CP_1) pulse.

TTL/MSI 93S05
VARIABLE MODULO COUNTER

DESCRIPTION – The TTL/MSI 93S05 is a monolithic, high speed, Variable Modulo Counter circuit, constructed with the TTL Schottky Barrier Diode process. It is a semisynchronous counter which can be programmed without extra logic to provide division or counting by either 2 and 4, 5, 6, 7, 8, or 10, 12, 14, 16. A binary count sequence can be obtained for all of the preceding counter modulos as well as 50% duty cycle output for dividers of 8, 10, 12, 14, 16. The device also features asynchronous overriding master reset and set inputs and the negation output of the final flip-flop output which allows the cascading of stages. The circuit uses Schottky TTL for super high speed, high fanout operation and is compatible with all other members of the TTL family of digital integrated circuits.

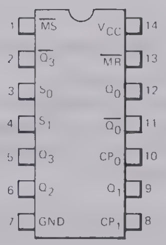
- VARIOUS BINARY COUNTING MODES
  - –MODULO 2 AND MODULO 5, 6, 7, 8
  - –MODULO 10 (8421 BCD), 12, 14, 16
- VARIOUS FREQUENCY DIVISION MODES WITH 50% DUTY CYCLE OUTPUT
  - –MODULO 8, 10, 12, 14, 16
- LOGIC SELECTION OF COUNTING MODE
- ASYNCHRONOUS MASTER RESET AND SET INPUTS
- MULTISTAGE COUNTING OPERATION
- TYPICAL COUNTING FREQUENCY OF 100 MHz
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

LOGIC SYMBOL

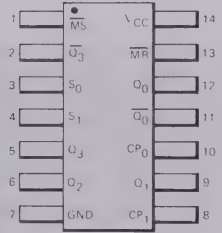

1
3
4
MS
S_0
S_1
10
8
CP_0
CP_1
93S05
$\overline{Q}_3$
2
MR
$\overline{Q}_0$
Q_0
Q_1
Q_2
Q_3
13
11
12
9
6
5

V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 $\overline{MS}$
2 $\overline{Q}_3$
3 S_0
4 S_1
5 Q_3
6 Q_2
7 GND
14 V_{CC}
13 $\overline{MR}$
12 Q_0
11 $\overline{Q}_0$
10 CP_0
9 Q_1
8 CP_1

FLATPAK (TOP VIEW)

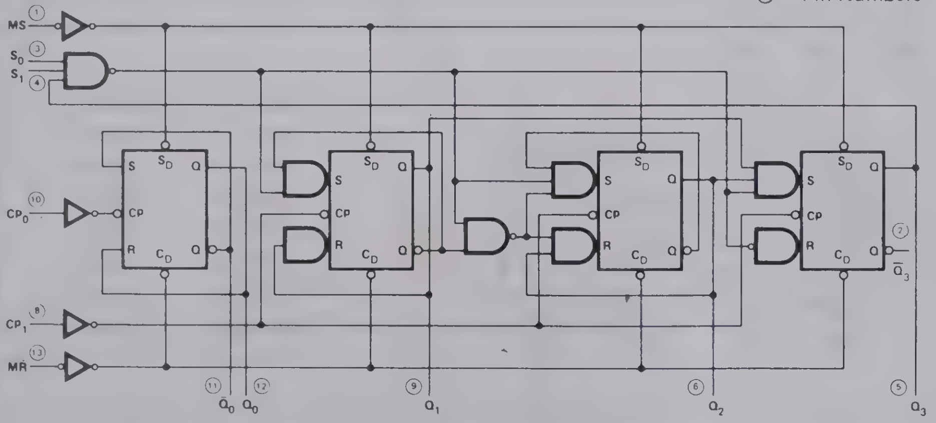

1 $\overline{MS}$
2 $\overline{Q}_3$
3 S_0
4 S_1
5 Q_3
6 Q_2
7 GND
14 V_{CC}
13 $\overline{MR}$
12 Q_0
11 $\overline{Q}_0$
10 CP_0
9 Q_1
8 CP_1

PIN NAMES

S_0, S_1	Select Inputs
CP_0	First Stage Clock Active HIGH Going Edge Input
CP_1	Three Stage Clock Active HIGH Going Edge Input
$\overline{MS}$	Master Set (Active LOW) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0	First Stage Output
$\overline{Q}_0$	Complementary First Stage Output
Q_1, Q_2, Q_3	Three Stage Counter Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOGIC DIAGRAM

○ = Pin Numbers


MS ①
S_0 ③
S_1 ④
CP_0 ⑩
CP_1 ⑧
MR ⑬
S
S_D
Q
CP
R
C_D
Q
⑦
$\overline{Q}_3$
⑪ $\overline{Q}_0$
⑫ Q_0
⑨ Q_1
⑥ Q_2
⑤ Q_3

TTL/MSI 9307

SEVEN SEGMENT DECODER

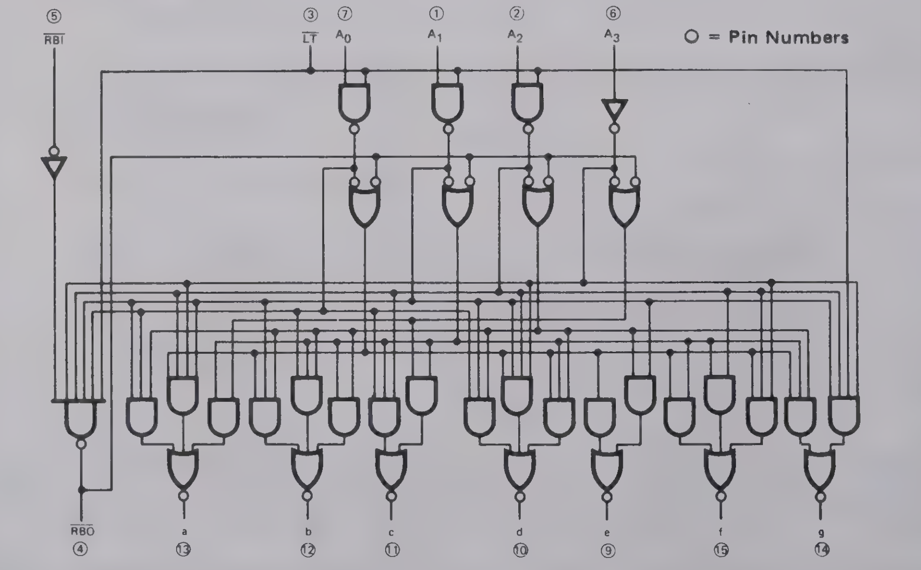
DESCRIPTION – The 9307 is a Seven Segment Decoder designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used with seven segment incandescent lamp, neon, electro-luminescent, or CRT numeric displays. The 9307 is compatible with all other Fairchild TTL devices.

- **TTL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE HIGH OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE**

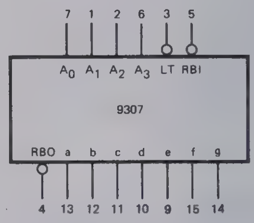
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7 V
Voltage Applied to Outputs for HIGH Output State	–0.5 V to +V_{CC} value
Input Voltage (dc)	–0.5 V to +5.5 V

LOGIC DIAGRAM

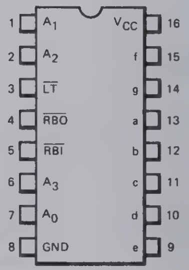

⑤
RBI
③ ⑦
LT
A0
①
A1
②
A2
⑥
A3
○ = Pin Numbers
RBO ④
a ⑬
b ⑫
c ⑪
d ⑩
e ⑨
f ⑮
g ⑭

LOGIC SYMBOL

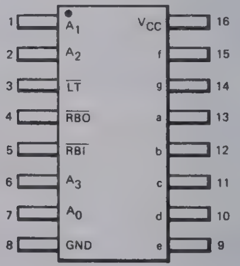

7 1 2 6 3 5
A0 A1 A2 A3 LT RBI
9307
RBO a b c d e f g
4 13 12 11 10 9 15 14

V_{CC}=PIN 16
GND=PIN 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 A1
2 A2
3 LT
4 RBO
5 RBI
6 A3
7 A0
8 GND
VCC 16
f 15
g 14
a 13
b 12
c 11
d 10
e 9

FLATPAK (TOP VIEW)


1 A1
2 A2
3 LT
4 RBO
5 RBI
6 A3
7 A0
8 GND
VCC 16
f 15
g 14
a 13
b 12
c 11
d 10
e 9

The 9307 seven segment decoder accepts a 4-bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0—9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in Figure 1. The numeric designations chosen to represent the decimal numbers are shown in Figure 3, together with the resulting displays for input code configurations in excess of binary nine.

The decoder has active HIGH outputs so that a buffer transistor may be used directly to provide the high currents required for incandescent displays. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. The value of this resistor is constrained by the 10 mA current sinking capability of the output transistors of the circuit.

The device has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{\text{RBO}}$) of a decoder to the Ripple Blanking Input ($\overline{\text{RBI}}$) of the next lower stage device. The most significant decoder stage should have the $\overline{\text{RBI}}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{\text{RBI}}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{\text{RBO}}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of DTL gates.

SEGMENT DESIGNATION

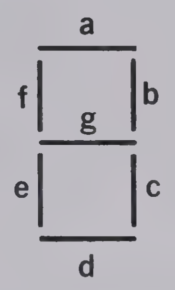


Fig. 1

TRUTH TABLE

$\overline{\text{LT}}$	$\overline{\text{RB}}$ IN	A_0	A_1	A_2	A_3	a	b	c	d	e	f	g	$\overline{\text{RB}}$ OUT	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
	X	H	L	L	L	L	H	H	L	L	L	L	H	1
		L	H	L	L	H	H	L	H	H	L	H	H	2
		H	H	L	L	H	H	H	H	L	L	H	H	3
		L	L	H	L	L	H	H	L	L	L	H	H	4
		H	L	H	L	H	L	H	H	L	H	H	H	5
		L	H	H	L	H	L	H	H	H	H	H	H	6
		H	H	H	L	H	H	H	L	L	L	L	H	7
		L	L	L	H	H	H	H	H	H	H	H	H	8
		H	L	L	H	H	H	H	H	L	H	H	H	9
		L	H	L	H	L	L	L	H	H	L	H	H	10
		H	H	L	H	L	L	L	H	L	L	H	H	11
		L	L	H	H	L	H	H	L	L	H	H	H	12
		H	L	H	H	H	L	H	H	L	H	H	H	13
		L	H	H	H	L	L	L	H	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	H	15

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Voltage Level

Fig. 2

NUMERICAL DESIGNATIONS

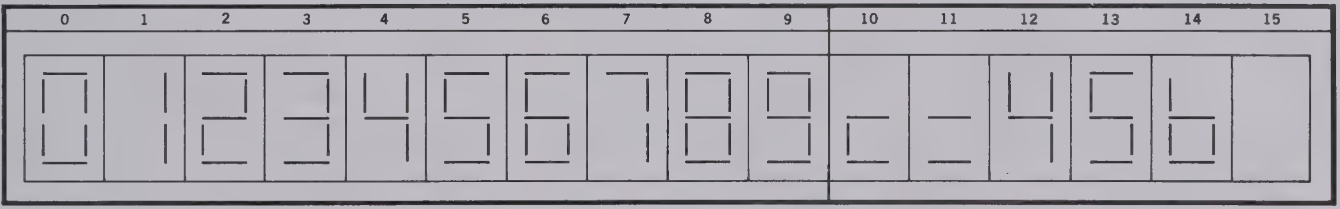


Fig. 3

Table 1 — LOADING RULES (1 U.L. = 1 DTL GATE INPUT LOAD)

Inputs	Loading (MIL & IND)	
	HIGH State	LOW State
A_0, A_1, A_2, A_3	1	1
$\overline{R}_{B(IN)}$	1	1/2
$\overline{\text{LT}}$	5	4.3

Outputs	Fan Out	
	MIL	IND
a, b, c, d, e, f, g	8	7
$\overline{R}_{B(OUT)}$	2.0	1.5

TABLE II – ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part No. 9307XM, see note)

SYMBOL	PARAMETER	LIMITS −55°C MIN.		+25°C MIN.			+125°C MIN.		UNITS	CONDITIONS
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	4.3 3.0		4.3 3.0	4.4 4.0		4.3 3.0		Volts	V_{CC} = 4.5 V I_{OH} = 0.0 mA (Pins 9–15) V_{CC} = 4.5 V I_{OH} = −70 µA (Pin 4) Inputs at Threshold Voltages (V_{IL} or V_{IH})
V_{OL}	Output LOW Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 12.5 mA (Pins 9–15) I_{OL} = 3.1 mA (Pin 4) V_{CC} = 4.5 V I_{OL} = 10 mA (Pins 9–15) I_{OL} = 2.4 mA (Pin 4) Inputs at Threshold Voltages (V_{IL} or V_{IH})
V_{IH}	Input HIGH Voltage	2.1		1.9			1.7		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		1.4			1.1		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL} (Pin 3) (Pins 1, 2, 6, 7) (Pin 5)	Input LOW Current		−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA	V_{CC} = 5.5 V V_{IN} = 0.4 V Other Inputs = 5.5 V
I_{IH} (Pin 3) (Pins 1, 2, 5, 6, 7)	Input HIGH Current					10 2.0		25 5.0	µA	V_{CC} = 5.5 V V_{IN} = 4.5 V Ground on Other Inputs
I_A (Pins 9–15)	Available Output Current	−1.4		−1.4			−1.0		mA	V_{OUT} = 0.85 V V_{CC} = 4.5 V Inputs at Threshold Voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9–15)	Short Circuit Current					−3.7			mA	V_{OUT} = 0.0 V V_{CC} = 5.5 V
I_{CC}	Supply Current		73			73		73	mA	V_{CC} = 5.5 V
t_{PLH}	Turn Off Delay					500			ns	V_{CC} = 5.0 V, See Fig. 5
t_{PHL}	Turn On Delay					500			ns	

TABLE III – ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9307X C, see note)

SYMBOL	PARAMETER	LIMITS 0°C		+25°C			+75°C		UNITS	CONDITIONS
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	4.3 2.7		4.3 2.7	4.6 4.0		4.3 2.7		Volts	V_{CC} = 4.75 V I_{OH} = 0.0 mA (Pins 9–15) V_{CC} = 4.75 V I_{OH} = −70 µA (Pin 4) Inputs at Threshold Voltages (V_{IL} or V_{IH})
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 11.5 mA (Pins 9–15) I_{OL} = 2.75 mA (Pin 4) V_{CC} = 4.75 V I_{OL} = 10 mA (Pins 9–15) I_{OL} = 2.4 mA (Pin 4) Inputs at Threshold Voltages (V_{IL} or V_{IH})
V_{IH}	Input HIGH Voltage	2.0		2.0			2.0		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL} (Pin 3) (Pins 1, 2, 6, 7) (Pin 5)	Input LOW Current		−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA	V_{CC} = 5.25 V V_{IN} = 0.45 V Other Inputs = 5.25 V
I_{IH} (Pin 3) (Pins 1, 2, 5, 6, 7)	Input HIGH Current					25 5.0		50 10	µA	V_{CC} = 5.25 V V_{IN} = 4.5 V Ground on Other Inputs
I_A (Pins 9–15)	Available Output Current	−1.4		−1.4			−1.1		mA	V_{OUT} = 0.75 V V_{CC} = 4.75 V Inputs at Threshold Voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9–15)	Short Circuit Current					−4.0			mA	V_{OUT} = 0.0 V V_{CC} = 5.25 V
I_{CC}	Supply Current		82			82		82	mA	V_{CC} = 5.25 V
t_{PLH}	Turn Off Delay					500			ns	V_{CC} = 5.0 V, See Fig. 5
t_{PHL}	Turn On Delay					500			ns	

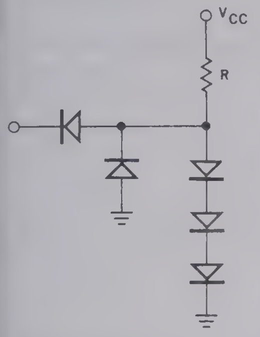
Note:
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

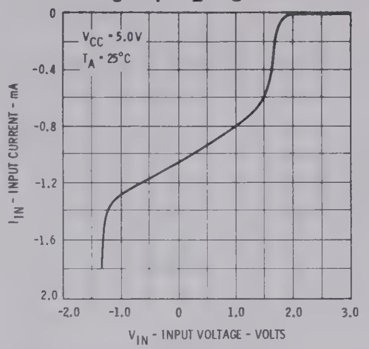
INPUTS

INPUT CURRENT VERSUS INPUT VOLTAGE

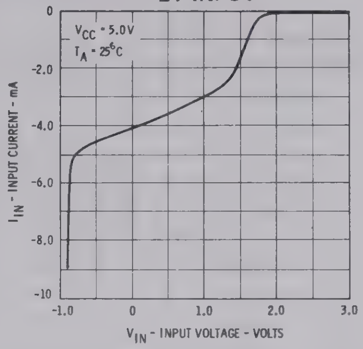
EQUIVALENT CIRCUIT



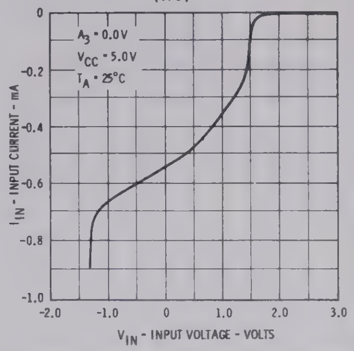
A_0, A_1, A_2, A_3 INPUTS



$\overline{LT}$ INPUT



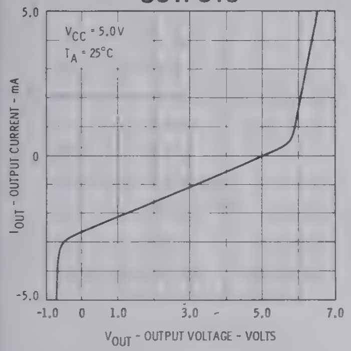
$\overline{RB}_{(IN)}$ INPUT



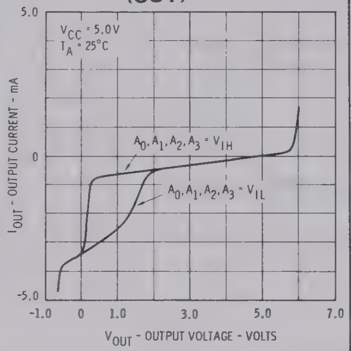
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

9307XM (−55°C to +125°C)
OUTPUT IN HIGH STATE

a, b, c, d, e, f, g
OUTPUTS

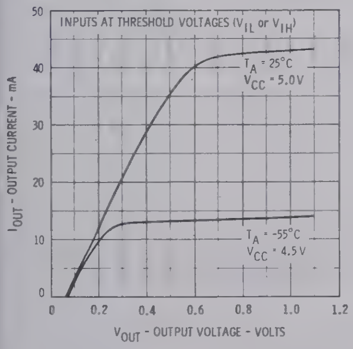


$\overline{RB}_{(OUT)}$ OUTPUT

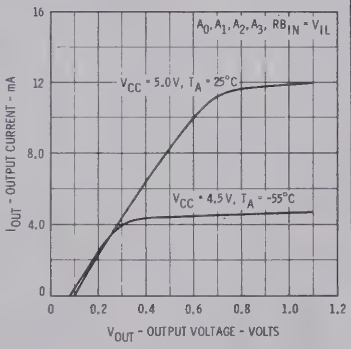


OUTPUT IN LOW STATE

a, b, c, d, e, f, g
OUTPUTS

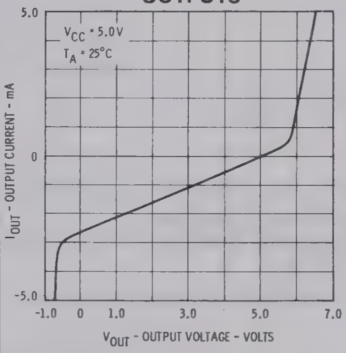


$\overline{RB}_{(OUT)}$ OUTPUT

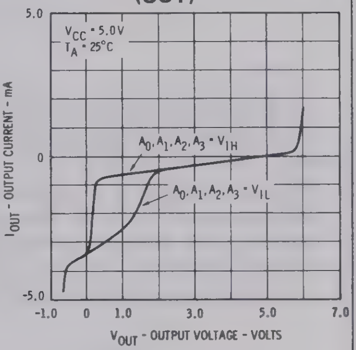


9307XC (0°C to +75°C)
OUTPUT IN HIGH STATE

a, b, c, d, e, f, g
OUTPUTS

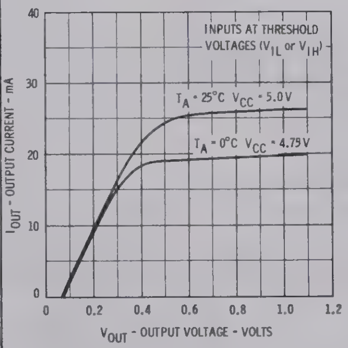


$\overline{RB}_{(OUT)}$ OUTPUT

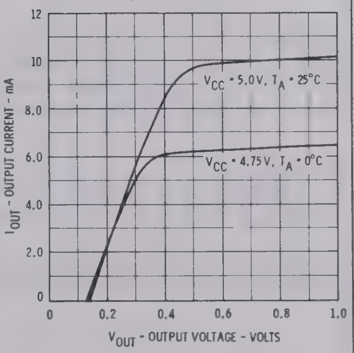


OUTPUT IN LOW STATE

a, b, c, d, e, f, g
OUTPUTS



$\overline{RB}_{(OUT)}$ OUTPUT



OUTPUT

EQUIVALENT CIRCUIT

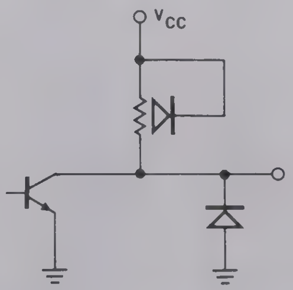


Fig. 4

SWITCHING WAVEFORMS

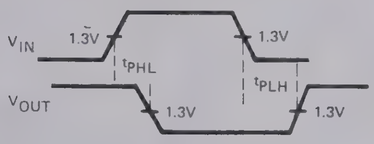


Fig. 5

TTL/MSI 9308

DUAL FOUR-BIT LATCH

DESCRIPTION — The MSI 9308 is a dual 4-Bit Latch designed for general purpose storage applications in high speed digital systems. The 9308 uses TTL technology and is compatible with DTL, TTL, and MSI families. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good ac noise immunity.

- ACTIVE LEVEL LOW ENABLE GATE INPUTS
- OVERRIDING MASTER RESET
- 25 ns THROUGH DELAY
- THE INPUT/OUTPUT CHARACTERISTICS PROVIDE DIRECT INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- HIGH CAPACITIVE DRIVE CAPABILITY
- ALL CERAMIC HERMETIC 24-LEAD DUAL IN-LINE PACKAGE

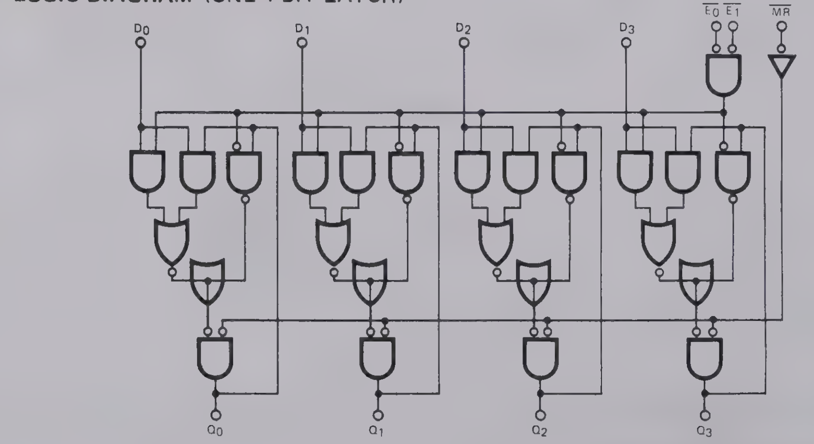
PIN NAMES		**LOADING**
		(Note a)
D_0, D_1, D_2, D_3	Parallel Latch Inputs	1.5 U.L.
$\overline{E}_0, \overline{E}_1$	AND Enable (Active LOW) Inputs	1 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Latch Outputs (Note b)	9 U.L.

NOTES:

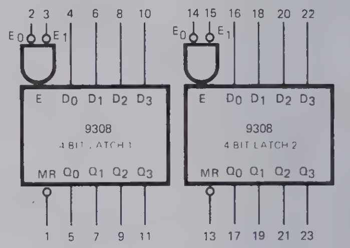
a. 1 unit load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. 9 U.L. is the output LOW drive factor and 18 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM (ONE 4-BIT LATCH)

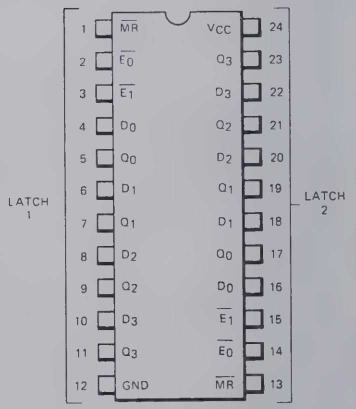

D0
D1
D2
D3
E0 E1
MR
Q0
Q1
Q2
Q3

LOGIC SYMBOL

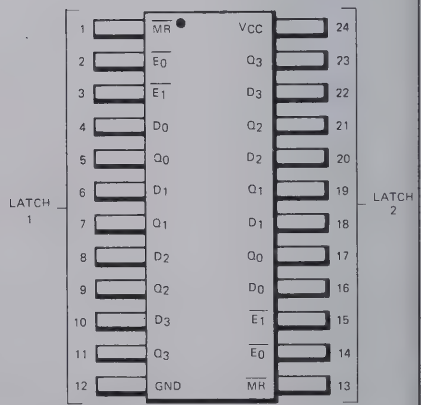

2 3 4 6 8 10
E0 E1
E D0 D1 D2 D3
9308
4 BIT LATCH 1
MR Q0 Q1 Q2 Q3
1 5 7 9 11
14 15 16 18 20 22
E0 E1
E D0 D1 D2 D3
9308
4 BIT LATCH 2
MR Q0 Q1 Q2 Q3
13 17 19 21 23

V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 MR
2 E0
3 E1
4 D0
5 Q0
6 D1
7 Q1
8 D2
9 Q2
10 D3
11 Q3
12 GND
24 VCC
23 Q3
22 D3
21 Q2
20 D2
19 Q1
18 D1
17 Q0
16 D0
15 E1
14 E0
13 MR
LATCH 1
LATCH 2

FLATPAK (TOP VIEW)


1 MR
2 E0
3 E1
4 D0
5 Q0
6 D1
7 Q1
8 D2
9 Q2
10 D3
11 Q3
12 GND
24 VCC
23 Q3
22 D3
21 Q2
20 D2
19 Q1
18 D1
17 Q0
16 D0
15 E1
14 E0
13 MR
LATCH 1
LATCH 2

FUNCTIONAL DESCRIPTION

LATCH OPERATION — Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input.

The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the master reset input.

TRUTH TABLE

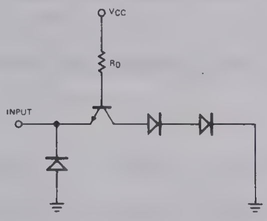
$\overline{MR}$	$\overline{E_0}$	$\overline{E_1}$	D	Q_n	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{n-1} = Previous Output State
Q_n = Present Output State

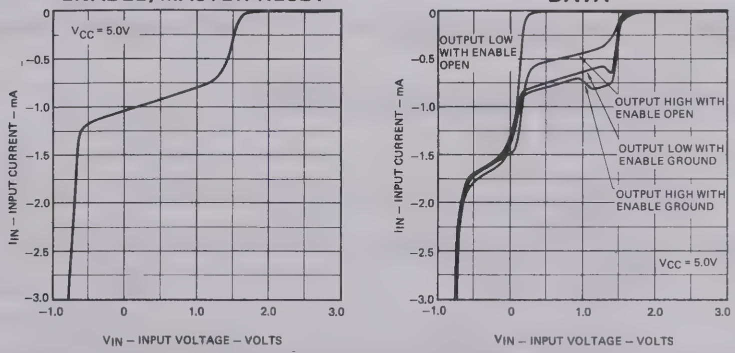
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS

EQUIVALENT CIRCUIT



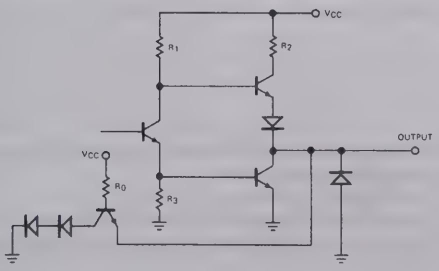
INPUT CURRENT VERSUS INPUT VOLTAGE


ENABLE, MASTER RESET

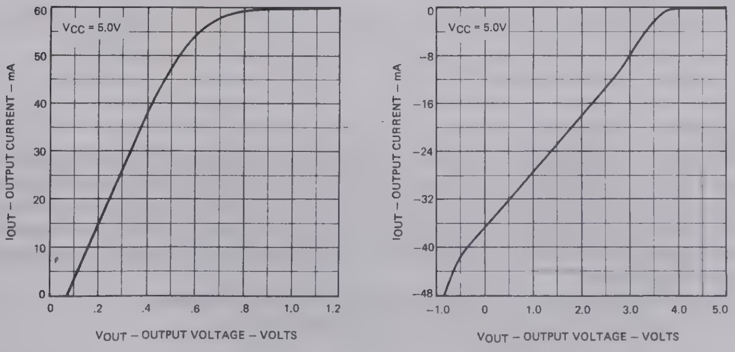
DATA

OUTPUTS

EQUIVALENT CIRCUIT



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE


LOW STATE

HIGH STATE

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9308XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9308XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC}=MIN., I_{IN}=−12 mA, T_A=25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC}=MIN., I_{OH}=−720 µA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 14.4 mA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
I_{IH}	Input HIGH Current					V_{CC} = MAX., V_{IN} = 2.4V
	$\overline{E}_0$, $\overline{E}_1$ & $\overline{MR}$		10	40	µA	
	D_0, D_1, D_2 & D_3		15	60	µA	
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current					V_{CC} = MAX., V_{IN} = 0.4V
	$\overline{E}_0$, $\overline{E}_1$ & $\overline{MR}$		−0.96	−1.6	mA	
	D_0, D_1, D_2 & D_3		−1.44	−2.4*	mA	* Max Instantaneous Current Out of The D Inputs
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−40	−70	mA	V_{CC} = MAX. V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		62	100	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	9308XM(MIL) MIN.	9308XM(MIL) TYP.	9308XM(MIL) MAX	9308XC(IND) MIN.	9308XC(IND) TYP.	9308XC(IND) MAX.	UNITS	TEST CONDITIONS	
t_{PLH}	Turn off Delay Enable to Output			30			35	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$pF
t_{PHL}	Turn on Delay Enable to Output			18			22	ns		
t_{PLH}	Turn off Delay Data to Output			20			23	ns	Fig. 2	
t_{PHL}	Turn on Delay Data To Output			18			20	ns		
t_{PHL}	Turn on Delay $\overline{MR}$ to Output			20			22	ns	Fig. 5	

SWITCHING SET-UP REQUIREMENTS ($T_A = 25°C$)

SYMBOL	PARAMETER	9308XM(MIL) MIN.	9308XM(MIL) TYP.	9308XM(MIL) MAX.	9308XC(IND) MIN.	9308XC(IND) TYP.	9308XC(IND) MAX.	UNITS	TEST CONDITIONS	
$t_s(H)$	Set-up Time HIGH Data to Enable	6.0	1.0		10	1.0		ns	Fig. 3	$V_{CC} = 5.0$ V
$t_h(H)$	Hold Time HIGH Data to Enable	–4.0	-7.0		–2.0	-7.0		ns		
$t_s(L)$	Set-up Time LOW Data to Enable	10	7.0		12	7.0		ns		
$t_h(L)$	Hold Time LOW Data to Enable	4.0	-1.0		8.0	-1.0		ns		
$t_{pw}\ \overline{E}$	Enable Pulse Width	15			18			ns	Fig. 4	
$t_{pw}\ \overline{MR}$	Master Reset Pulse Width	15			18			ns	Fig. 5	
t_{rec}	Recovery Time Master Reset to Enable	10			12			ns	Fig. 6	

SET UP TIME: t_s is defined as the time required for the logic level to be present at the Data Input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.

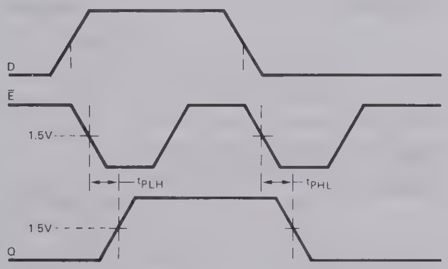
HOLD TIME: t_h is defined as the minimum time following the Enable transition from LOW to HIGH that the logic level must be maintained at the data input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the Enable transition from LOW to HIGH and still be recognized.

RECOVERY TIME: t_{rec} is defined as the time that the Enable must remain LOW after the Master Reset transition from LOW to HIGH in order for the latch to recognize and store HIGH data.

SWITCHING CHARACTERISTICS

All delays are measured with $V_{CC} = 5.0$ V applied to Pin 24 and Pin 12 grounded. Outputs under test are loaded with 15 pF (includes jig and probe). Pins not referenced are not connected.

Fig. 1 — t_{PLH}/t_{PHL} (ENABLE TO OUTPUT)



OTHER CONDITIONS: $\overline{MR}$ = H

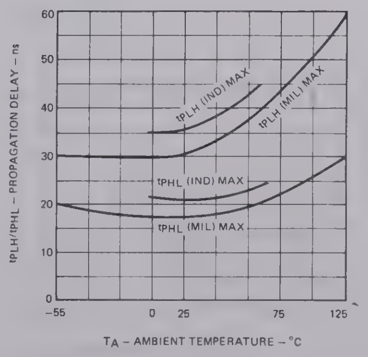
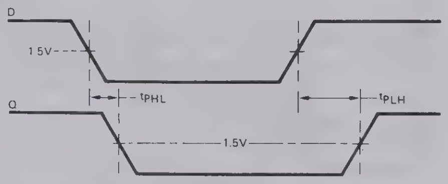
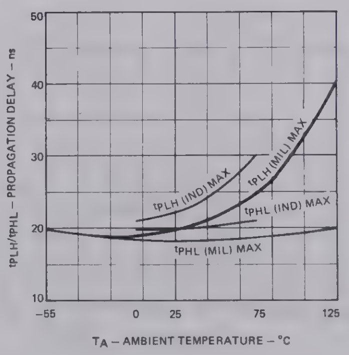


Fig. 2 — t_{PLH}/t_{PHL} (DATA TO OUTPUT)

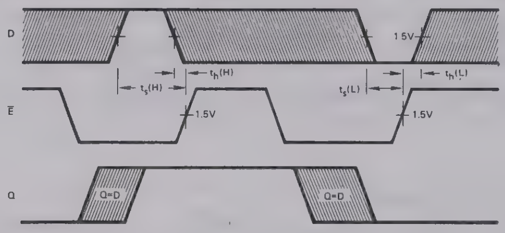


OTHER CONDITIONS $\overline{E}$ = L, $\overline{MR}$ = H



SWITCHING CHARACTERISTICS

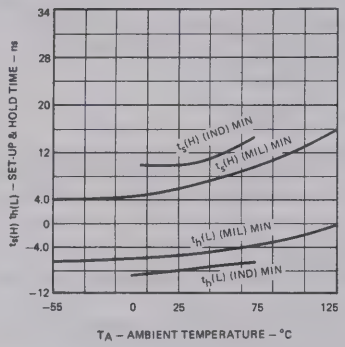
Fig. 3 – SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO ENABLE


D
1.5V
$t_h(H)$
$t_s(H)$
$t_s(L)$
$t_h(L)$
Ē
1.5V
1.5V
Q
Q=D
Q=D

OTHER CONDITIONS: $\overline{MR}$ = H

The shaded areas indicate when the Data input is permitted to change for predictable output performance.

NOTE: The polarities of the $t_h(H)$ and $t_h(L)$ values are inverted on the graphs. This representation allows the graphs to show the true distribution of the $t_{(set\text{-}up)}$ parameters.



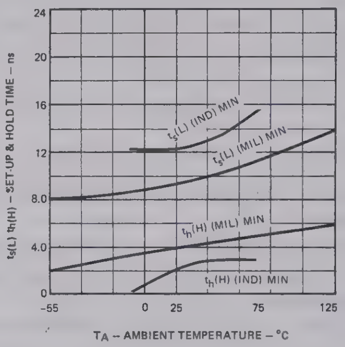
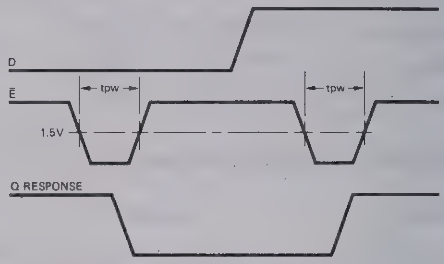


Fig. 4 – t_{pw} (MIN. ENABLE PULSE WIDTH)


D
Ē
tpw
tpw
1.5V
Q RESPONSE

OTHER CONDITION: $\overline{MR}$ = H

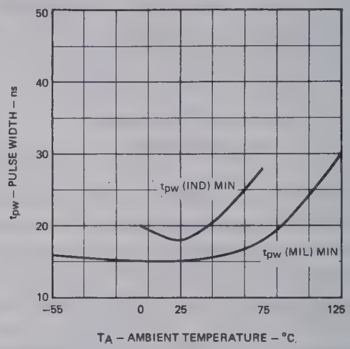
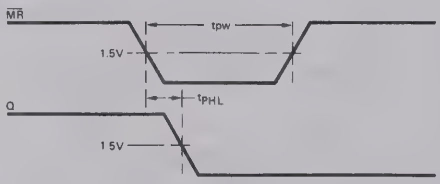


Fig. 5 – t_{pw} (MIN. MASTER RESET PULSE WIDTH) t_{PHL} (MASTER RESET TO OUTPUT)


$\overline{MR}$
tpw
1.5V
Q
t_{PHL}
1.5V

OTHER CONDITIONS: D = H, Ē = L

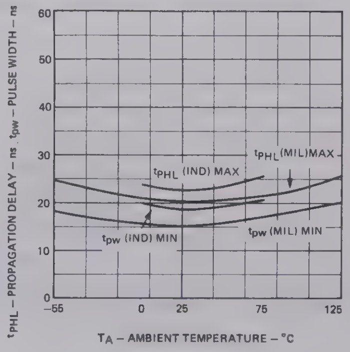
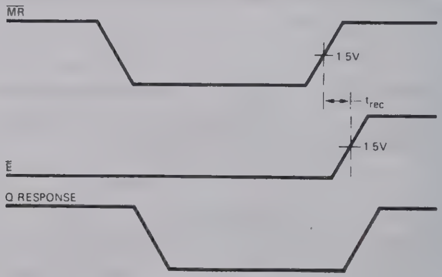
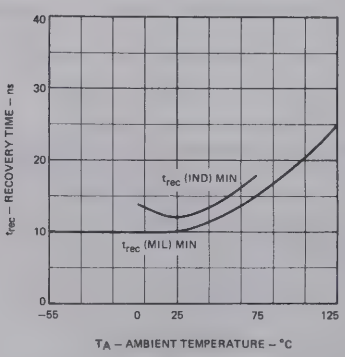


Fig. 6 – t_{rec} (MASTER RESET RECOVERY TIME)


$\overline{MR}$
1.5V
t_{rec}
1.5V
Ē
Q RESPONSE

OTHER CONDITIONS: D = H



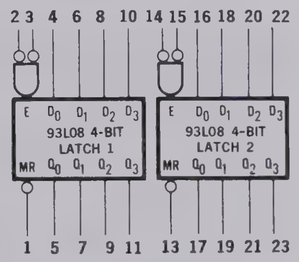
LPTTL/MSI 93L08

LOW POWER DUAL FOUR-BIT LATCH

DESCRIPTION The LPTTL/MSI 93L08 is a Dual 4-Bit Latch designed for general purpose storage applications in medium speed digital systems. The 93L08 uses TTL technology and is TTL compatible. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good ac noise immunity.

- **ACTIVE LEVEL LOW ENABLE GATE INPUTS**
- **OVERRIDING MASTER RESET**
- **TYPICAL PROPAGATION DELAY OF 53 ns**
- **TYPICAL POWER DISSIPATION OF 100 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 24-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

LOGIC SYMBOL


2 3 4 6 8 10 14 15 16 18 20 22
E D0 D1 D2 D3
93L08 4-BIT LATCH 1
MR Q0 Q1 Q2 Q3
93L08 4-BIT LATCH 2
1 5 7 9 11 13 17 19 21 23

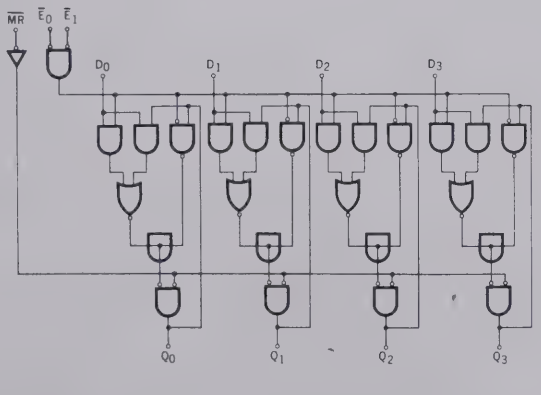
V_{CC} = Pin 24
GND = Pin 12

PIN NAMES

PIN NAMES		LOADING HIGH	LOADING LOW
D_0, D_1, D_2, D_3	Parallel Latch Inputs	0.75 U.L.	0.375 U.L.
$\overline{E}$	AND Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Latch Outputs	9.0 U.L.	2.25 U.L.

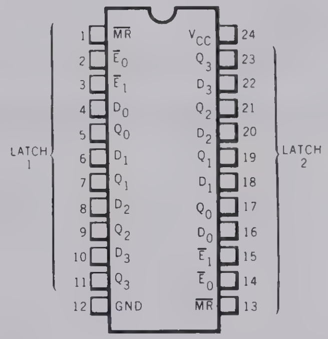
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

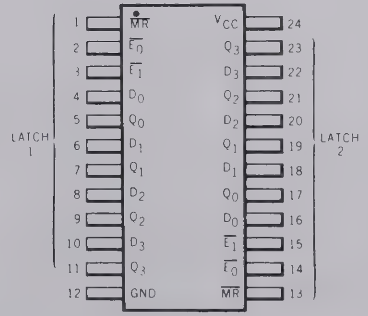

MR
E0 E1
D0
D1
D2
D3
Q0
Q1
Q2
Q3

NOTE: Only one 4-Bit Latch shown.

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 MR
2 E0
3 E1
4 D0
5 Q0
6 D1
7 Q1
8 D2
9 Q2
10 D3
11 Q3
12 GND
24 VCC
23 Q3
22 D3
21 Q2
20 D2
19 Q1
18 D1
17 Q0
16 D0
15 E1
14 E0
13 MR
LATCH 1
LATCH 2

FLATPAK (TOP VIEW)


1 MR
2 E0
3 E1
4 D0
5 Q0
6 D1
7 Q1
8 D2
9 Q2
10 D3
11 Q3
12 GND
24 VCC
23 Q3
22 D3
21 Q2
20 D2
19 Q1
18 D1
17 Q0
16 D0
15 E1
14 E0
13 MR
LATCH 1
LATCH 2

LATCH OPERATION — Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input.

The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the master reset input.

TRUTH TABLE

$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D	Q_0	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{n-1} = Previous Output State
Q_n = Present Output State

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L08XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L08XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 5)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.36 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All INputs
I_{IL}	Input LOW Current $\overline{E}_0$, $\overline{E}_1$ & $\overline{MR}$		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
	Input LOW Current D_0, D_1, D_2 & D_3		−0.38	−0.64	mA	V_{CC} = MAX., V_{IN} = 0 V (See Note 4)
I_{IH}	Input HIGH Current $\overline{E}_0$, $\overline{E}_1$ & $\overline{MR}$ D_0, D_1, D_2 & D_3		 2.0 3.0	 20 30	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 6)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		20	33	mA	V_{CC} = MAX., All Outputs LOW, Pins 2 & 14 GND, Other Inputs Open

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. This current is measured at V_{IN} = 0 V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at V_{IN} = 0.3 V is 0.6 mA.
5. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
6. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
t_{PLH}	Enable to Output		35	60	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Enable to Output		30	50			
t_{PLH}	Data to Output		30	50	ns	Fig. 2	
t_{PHL}	Data to Output		35	55			
t_{PHL}	Master Reset to Output		31	55	ns	Fig. 5	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS	
t_s (H)	HIGH Data to Enable	25	15		ns	Fig. 3	V_{CC} = 5.0 V
t_s (L)	LOW Data to Enable	35	22				
t_h (H)	HIGH Data to Enable	0			ns	Fig. 3	
t_h (L)	LOW Data to Enable	0					
$t_{pw}\,\overline{E}$	Enable Pulse Width	45	30		ns	Fig. 4	
$t_{pw}\,\overline{MR}$	Master Reset Pulse Width	40	25		ns	Fig. 5	
t_{rec}	Master Reset Recovery Time	30			ns	Fig. 6	

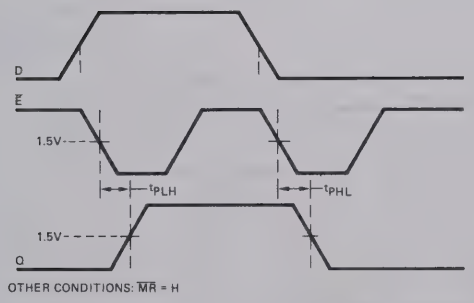
SET UP TIME: t_s is defined as the time required for the logic level to be present at the data input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.

HOLD TIME: t_h is defined as the minimum time following the Enable transition from LOW to HIGH that the logic level must be maintained at the data input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the Enable transition from LOW to HIGH and still be recognized.

RECOVERY TIME: t_{rec} is defined as the time that the enable must remain LOW after the master reset transition from LOW to HIGH in order for the latch to recognize and store HIGH data.

SWITCHING WAVEFORMS

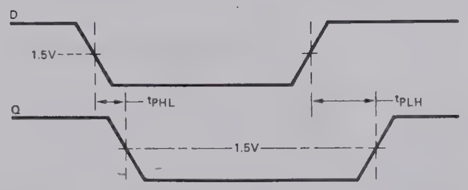
t_{PLH}/t_{PHL} (ENABLE TO OUTPUT)



OTHER CONDITIONS: $\overline{MR}$ = H

Fig. 1

t_{PLH}/t_{PHL} (DATA TO OUTPUT)

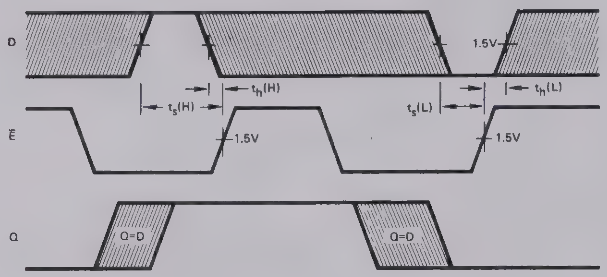


OTHER CONDITIONS: $\overline{E}$ = L, $\overline{MR}$ = H

Fig. 2

SWITCHING WAVEFORMS (Cont'd)

SETUP TIME (t_s) AND HOLD TIME (t_h) DATA TO ENABLE

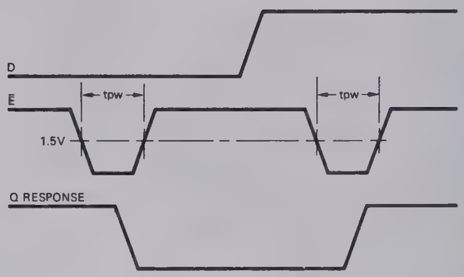

D
1.5V
$t_s(H)$
$t_h(H)$
$t_s(L)$
$t_h(L)$
$\overline{E}$
1.5V
1.5V
Q
Q=D
Q=D

OTHER CONDITIONS: $\overline{MR}$ = H

The shaded areas indicate when the Data input is permitted to change to predictable output performance.

Fig. 3

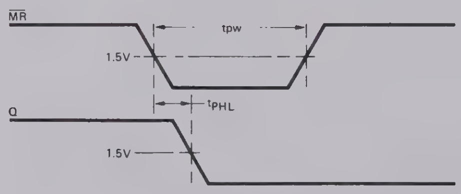
t_{pw} (MIN. ENABLE PULSE WIDTH)


D
$\overline{E}$
tpw
tpw
1.5V
Q RESPONSE

OTHER CONDITIONS: $\overline{MR}$ = H

Fig. 4

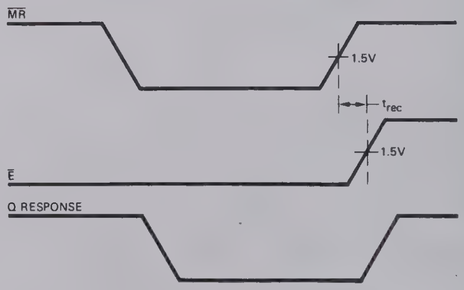
t_{pw} (MIN. MASTER RESET PULSE WIDTH)
t_{PHL} (MASTER RESET TO OUTPUT)


$\overline{MR}$
tpw
1.5V
t_{PHL}
Q
1.5V

OTHER CONDITIONS: D = H, $\overline{E}$ = L

Fig. 5

t_{rec} (MASTER RESET RECOVERY TIME)


$\overline{MR}$
1.5V
t_{rec}
1.5V
$\overline{E}$
Q RESPONSE

OTHER CONDITIONS: D = H

Fig. 6

TTL/MSI 9309

DUAL FOUR-INPUT MULTIPLEXER

DESCRIPTION — The 9309 is a monolithic, high speed, Dual Four-Input digital Multiplexer circuit, consisting of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to multiplexer operation, the 9309 can generate any two function of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTL for high speed, high fan out operation and is compatible with all other members of the Fairchild TTL family.

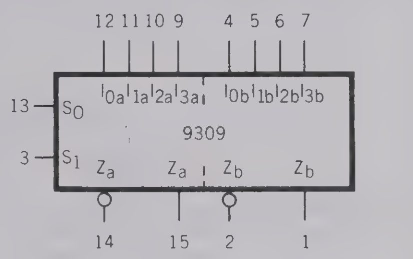
- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		**LOADING** (Note a)
S_0, S_1	Common Select Inputs	1 U.L.
Multiplexer A		
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs	1 U.L.
Z_a	Multiplexer Output (Note b)	10 U.L.
$\overline{Z}_a$	Complementary Multiplexer Output (Note c)	9 U.L.
Multiplexer B		
I_{0b}, I_{1b}, I_{2b}, I_{3b}	Multiplexer Inputs	1 U.L.
Z_b	Multiplexer Output (Note b)	10 U.L.
$\overline{Z}_b$	Complementary Multiplexer Output (Note c)	9 U.L.

NOTES:

a. 1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.
c. 9 U.L. is the output LOW drive factor and 18 U.L. is the output HIGH drive factor.

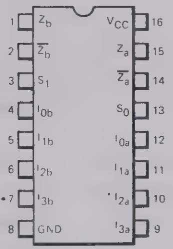
LOGIC SYMBOL



12 11 10 9
4 5 6 7
13
3
S0
S1
I0a I1a I2a I3a
I0b I1b I2b I3b
9309
Za
Za
Zb
Zb
14
15
2
1

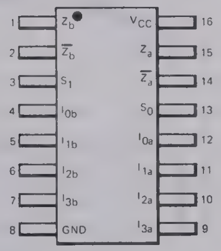
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



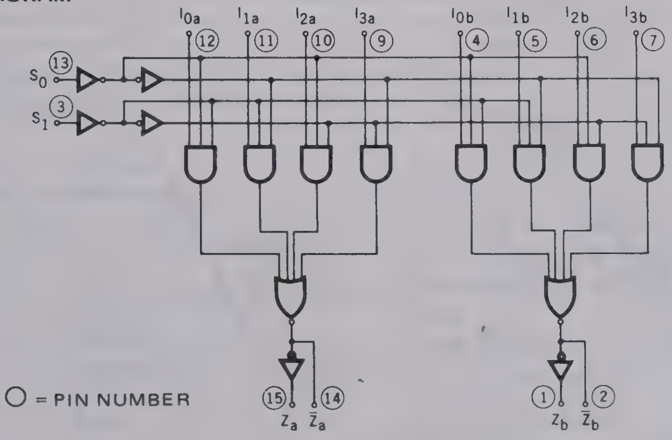
1 Zb
2 Z̄b
3 S1
4 I0b
5 I1b
6 I2b
7 I3b
8 GND
16 VCC
15 Za
14 Z̄a
13 S0
12 I0a
11 I1a
10 I2a
9 I3a

FLATPAK (TOP VIEW)



1 Zb
2 Z̄b
3 S1
4 I0b
5 I1b
6 I2b
7 I3b
8 GND
16 VCC
15 Za
14 Z̄a
13 S0
12 I0a
11 I1a
10 I2a
9 I3a

LOGIC DIAGRAM



I0a 12
I1a 11
I2a 10
I3a 9
I0b 4
I1b 5
I2b 6
I3b 7
S0 13
S1 3
15 Za
14 Z̄a
1 Zb
2 Z̄b
○ = PIN NUMBER

FUNCTIONAL DESCRIPTION — The 9309 dual four-input multiplexer is a member of the Fairchild family of compatible medium scale integrated (MSI) digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

The 9309 dual four-input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$Z_a = I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0$

$Z_b = I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0$

A common use of the 9309 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious use is as a function generator. The 9309 can generate any two functions of three variables. This is useful for implementing random gating functions.

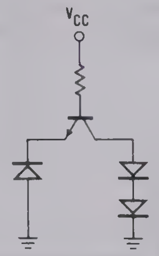
TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	$\overline{Z}_b$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

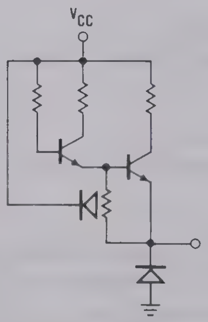
L = LOW Voltage Level
H = HIGH Voltage Level
X = Either HIGH or LOW Logic Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

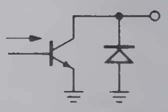
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE

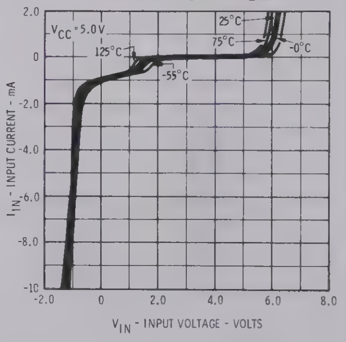


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

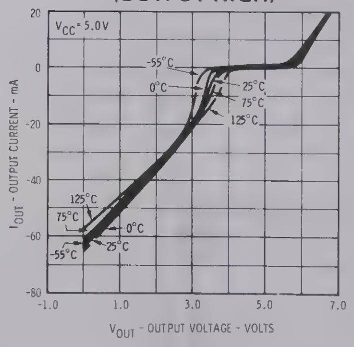


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

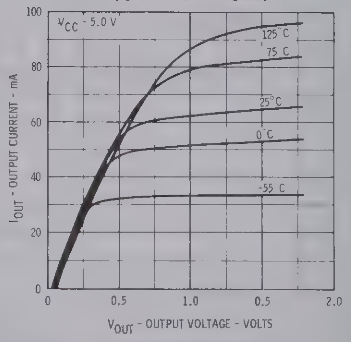


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
*Input Voltage (dc)	−0.5V to +5.5V
*Input Current (dc)	−30mA to +5.0mA
Voltage Applied to Outputs (Output HIGH)	−0.5V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9309XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9309XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 4)	MAX		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., $I_{IN} = -12$ mA, $T_A = 25°C$
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., $I_{OH} = -800\mu A$ $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−40	−70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		30	44	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0V, 25°C and maximum loading.

(5) Not more than one output should be shorted at a time.

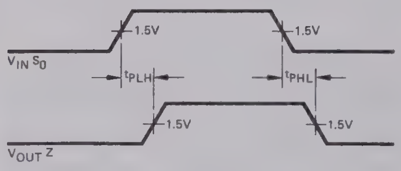
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output (S_0 to Z_a)		24	32	ns	V_{CC} = 5.0 V C_L = 15 pF (See Fig. 4)
t_{PHL}	Turn On Delay Input to Output (S_0 to Z_a)		24	32	ns	

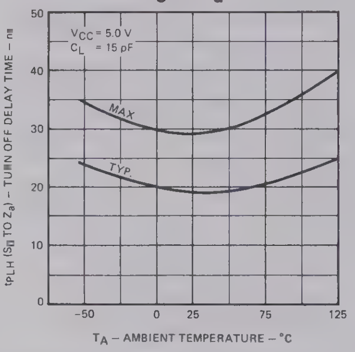
SWITCHING CHARACTERISTICS

Fig. 4

t_{PLH}/t_{PHL} S_0 to Z_a


1.5V
1.5V
V_IN S_0
t_PLH
t_PHL
1.5V
1.5V
V_OUT Z

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)



TURN ON DELAY TIME VERSUS TEMPERATURE (S_0 to Z_a)

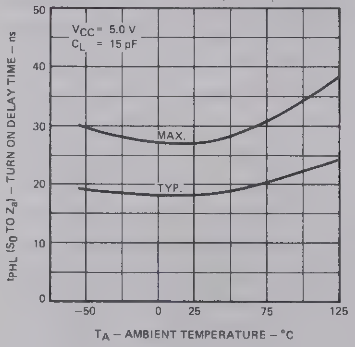
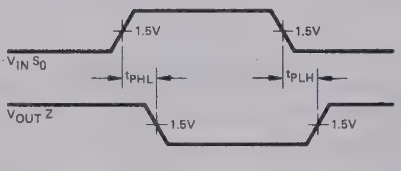
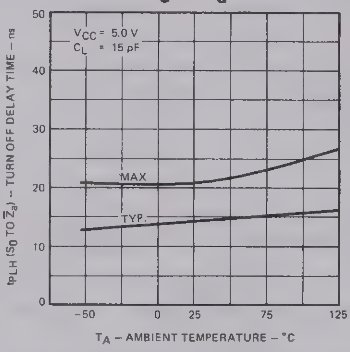


Fig. 5

t_{PLH}/t_{PHL} S_0 to $\overline{Z}_a$


1.5V
1.5V
V_IN S_0
t_PHL
t_PLH
V_OUT Z
1.5V
1.5V

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)

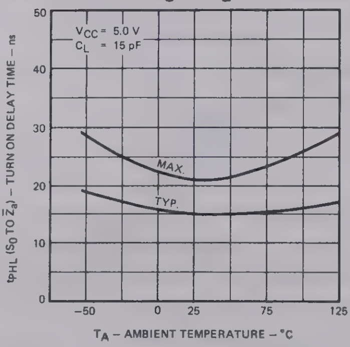
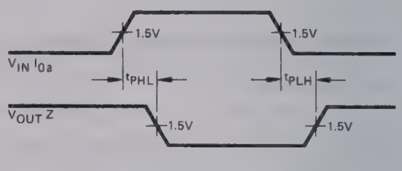
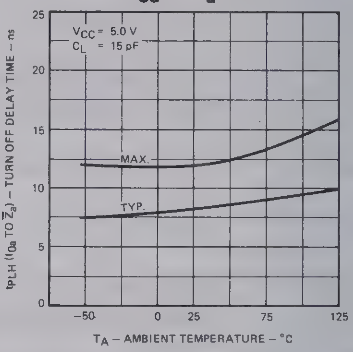


Fig. 6

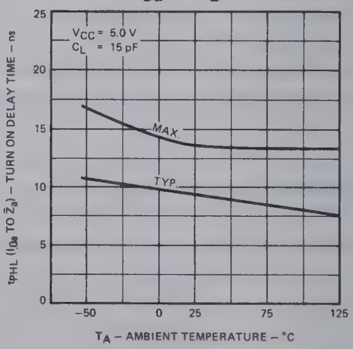
t_{PLH}/t_{PHL} I_{0a} to $\overline{Z}_a$


1.5V
1.5V
V_IN I_0a
t_PHL
t_PLH
V_OUT Z
1.5V
1.5V

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\overline{Z}_a$)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\overline{Z}_a$)



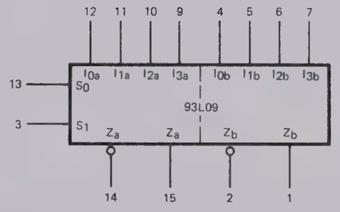
LPTTL/MSI 93L09

LOW POWER DUAL FOUR-INPUT MULTIPLEXER

DESCRIPTION – The LPTTL/MSI 93L09 is a Monolithic, Medium Speed, Dual 4-Input Digital Multiplexer. It consists of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the 93L09 can generate two functions of three variables. Active pullups in the outputs ensure good drive and speed performance. The 93L09 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTL technology and is compatible with all other members of the TTL family.

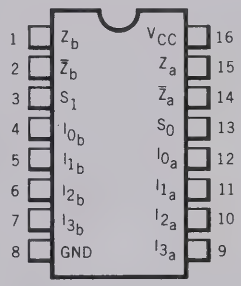
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- TYPICAL PROPAGATION DELAY OF 48 ns
- TYPICAL POWER DISSIPATION OF 40 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

LOGIC SYMBOL


12
11
10
9
4
5
6
7
13
3
I_{0a} I_{1a} I_{2a} I_{3a}
I_{0b} I_{1b} I_{2b} I_{3b}
S_0
S_1
93L09
$\overline{Z}_a$ Z_a $\overline{Z}_b$ Z_b
14
15
2
1

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)

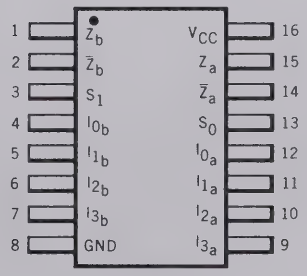

1 $\overline{Z}_b$
2 Z_b
3 S_1
4 I_{0b}
5 I_{1b}
6 I_{2b}
7 I_{3b}
8 GND
16 V_{CC}
15 Z_a
14 $\overline{Z}_a$
13 S_0
12 I_{0a}
11 I_{1a}
10 I_{2a}
9 I_{3a}

PIN NAMES

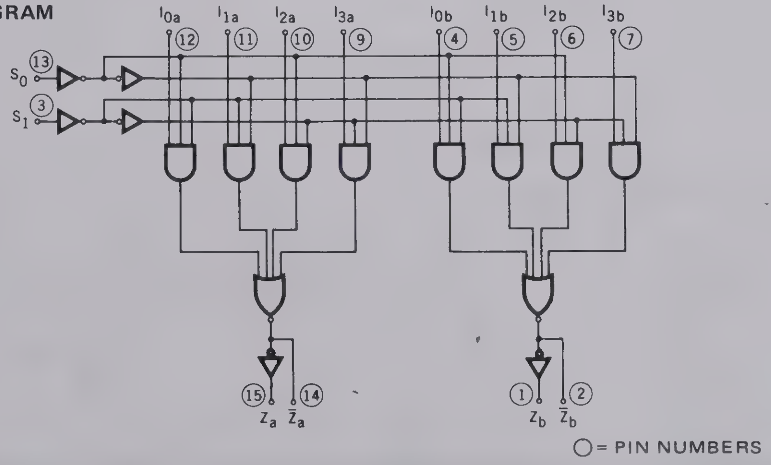
PIN NAMES		LOADING HIGH	LOADING LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_a	Multiplexer Output	10 U.L.	2.5 U.L.
$\overline{Z}_a$	Complementary Multiplexer Output	10 U.L.	2.25 U.L.
Multiplexer B			
I_{0b}, I_{1b}, I_{2b}, I_{3b}	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_b	Multiplexer Output	10 U.L.	2.5 U.L.
$\overline{Z}_b$	Complementary Multiplexer Output	10 U.L.	2.25 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

FLATPAK (TOP VIEW)


1 $\overline{Z}_b$
2 Z_b
3 S_1
4 I_{0b}
5 I_{1b}
6 I_{2b}
7 I_{3b}
8 GND
16 V_{CC}
15 Z_a
14 $\overline{Z}_a$
13 S_0
12 I_{0a}
11 I_{1a}
10 I_{2a}
9 I_{3a}

LOGIC DIAGRAM


I_{0a} ⑫
I_{1a} ⑪
I_{2a} ⑩
I_{3a} ⑨
I_{0b} ④
I_{1b} ⑤
I_{2b} ⑥
I_{3b} ⑦
S_0 ⑬
S_1 ③
⑮ Z_a
⑭ $\overline{Z}_a$
① Z_b
② $\overline{Z}_b$
○ = PIN NUMBERS

FUNCTIONAL DESCRIPTION – The 93L09 dual 4-input multiplexer is a member of the Fairchild family of compatible low power medium scale integrated digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

The 93L09 is the logical implementation of two-pole, four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Z_a = I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0$$
$$Z_b = I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0$$

The 93L09 is frequently used to move data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious application is as a function generator. The 93L09 can generate two functions of three variables. This is useful for implementing random gating functions.

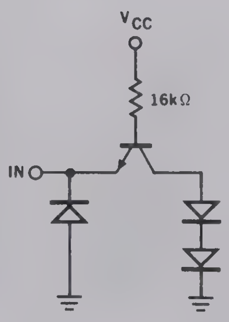
TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	Z_a
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	Z_b
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

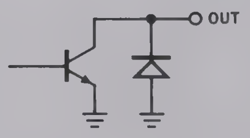
L = LOW Voltage Level
H = HIGH Voltage Level
X = Either HIGH or LOW Logic Level

TYPICAL INPUT AND OUTPUT CIRCUITS

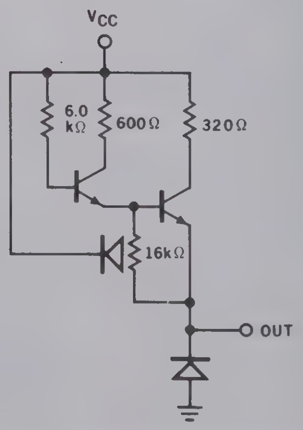
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L09XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L09XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pins 1 & 15) I_{OL} = 3.6 mA (Pins 2 & 14) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 5)	−10	−26	−40	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		7.5	11.5	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

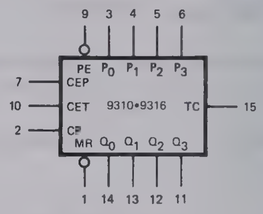
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{PLH} (S_0 to Z_a)	Turn Off Delay Input to Output		35	55	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL} (S_0 to Z_a)	Turn On Delay Input to Output		32	50	ns	

TTL/MSI 9310•9316
BCD DECADE COUNTER/4-BIT BINARY COUNTER

DESCRIPTION – The 9310 is a High Speed Synchronous BCD Decade Counter and the 9316 is a High Speed Synchronous 4-Bit Binary Counter. They are synchronously presetable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

- SYNCHRONOUS COUNTING AND PARALLEL ENTRY
- DECODED TERMINAL COUNT
- BUILT-IN CARRY CIRCUITRY
- TYPICAL COUNTING FREQUENCY OF 45 MHz
- TYPICAL POWER DISSIPATION OF 325 mW
- THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, AND TTL FAMILIES
- INPUT DIODE CLAMPING
- TTL COMPATIBLE

LOGIC SYMBOL

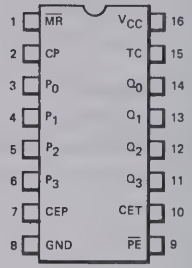

9
3
4
5
6
PE
P_0
P_1
P_2
P_3
7
CEP
10
CET
9310•9316
TC
15
2
CP
MR
Q_0
Q_1
Q_2
Q_3
1
14
13
12
11

V_{CC} = Pin 16
GND = Pin 8

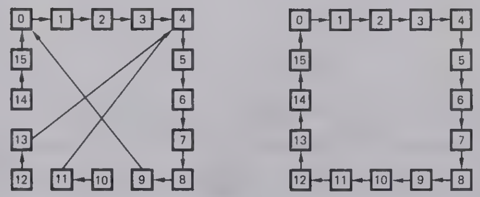
PIN NAMES		**LOADING** (Note a)
$\overline{PE}$	Parallel Enable (Active LOW) Input	2 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	2/3 U.L.
CEP	Count Enable Parallel Input	1 U.L.
CET	Count Enable Trickle Input	2 U.L.
CP	Clock (Active HIGH Going Edge) Input	2 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs (Note b)	8 U.L.
TC	Terminal Count Outputs (Note c)	10 U.L.

NOTES
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 8 U.L. is the output LOW drive factor and 16 U.L. is the output HIGH drive factor.
c. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1
$\overline{MR}$
2
CP
3
P_0
4
P_1
5
P_2
6
P_3
7
CEP
8
GND
16
V_{CC}
15
TC
14
Q_0
13
Q_1
12
Q_2
11
Q_3
10
CET
9
$\overline{PE}$

STATE DIAGRAM


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

9310

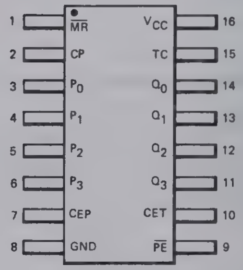
9316

LOGIC EQUATIONS

Count Enable = CEP • CET • PE
TC for 9310 = CET • $Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3$
TC for 9316 = CET • $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$
Preset = $\overline{PE}$ • CP+ (rising clock edge)
Reset = $\overline{MR}$

NOTE:
The 9310 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

FLATPAK (TOP VIEW)


1
$\overline{MR}$
2
CP
3
P_0
4
P_1
5
P_2
6
P_3
7
CEP
8
GND
16
V_{CC}
15
TC
14
Q_0
13
Q_1
12
Q_2
11
Q_3
10
CET
9
$\overline{PE}$

FUNCTIONAL DESCRIPTION — The 9310 is a high speed BCD decade counter, and the 9316 is a high speed binary counter. Both counters are fully synchronous with the clock pulse driving four master/slave flip-flops in parallel through a clock buffer. During the LOW to HIGH transition of the clock, the master is inhibited from further change. After the masters are locked out, data is transferred from the master to the slaves and reflected at the outputs. When the clock is HIGH, the masters are inhibited and the master/slave data path remains established. During the HIGH to LOW transition of the clock, the slave is inhibited from further change, followed by the enabling of the masters for the acceptance of data from the counting logic or the parallel entry logic. (See Clock Pulse Characteristics Figure 7)

The three control inputs, Parallel Enable ($\overline{\text{PE}}$), Count Enable Parrallel (CEP), and Count Enable Trickle (CET), select the mode of operation as shown in the tables below. When the conditions for counting are satisfied, the rising edge of a clock pulse will change the counters to the next state of the count sequence shown in the State Diagram on the previous page. The Count Mode is enabled when CEP and CET inputs and $\overline{\text{PE}}$ are HIGH.

The 9310 and 9316 can be synchronously preset from the four Parallel inputs, ($P_{0\text{-}3}$) when $\overline{\text{PE}}$ is LOW. When the Parallel Enable and Clock are LOW, each master of the flip-flops is connected to the appropriate parallel input (P_{0-3}) and the slaves (outputs) are steady in their previous state. When the clock goes HIGH, the masters are inhibited and this information is transferred to the slaves and reflected at the outputs. The parallel enable input overrides both count enable inputs, presetting the counter when LOW.

Terminal count is HIGH when the counter is at terminal count (state 9 for 9310, and state 15 for 9316), and Count Enable Trickle is HIGH, as is shown in the logic equations. Without additional logic, multistage synchronous counting at high speeds is made possible with a high speed lookahead technique utilizing the count enable and terminal count logic. A multistage counter illustrating these techniques is shown and discussed in the application section.

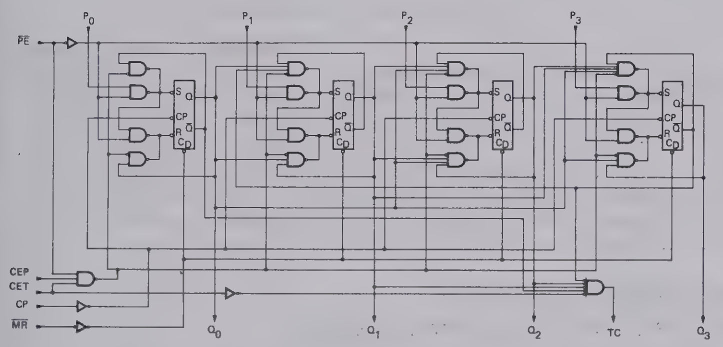
When LOW, the asynchronous master reset overrides all other inputs resetting the four outputs LOW.

Conventional operation of the 9310 • 9316, as shown in the Mode Selection table, requires that the mode control inputs ($\overline{\text{PE}}$, CEP, CET) are stable while the clock is LOW. This is no constraint for a normal synchronous system where all signals are generated by the rising edge of the clock.

For some applications, the designer may want to change those inputs while the clock is LOW. In this case the 9310 • 9316 will behave in a predictable manner. For example:

> If $\overline{\text{PE}}$ goes HIGH while the clock is LOW, but Count Enable is not aetive during the remaining clock LOW period (i.e. CEP or CET are LOW), the subsequent LOW to HIGH clock transition will change $Q_0 \ldots Q_3$ to the $P_0 \ldots P_3$ data that existed at the set-up time before the rising edge of $\overline{\text{PE}}$.
>
> If Count Enable is active (i.e. CEP and CET are HIGH) during some portion of the clock LOW period, but $\overline{\text{PE}}$ is HIGH (inactive) during the entire clock LOW period, the subsequent LOW to HIGH clock transition will change $Q_0 \ldots Q_3$ to the next count value.
>
> If $\overline{\text{PE}}$ goes HIGH while the clock is LOW, but Count Enable is active (CEP and CET are HIGH) during some portion of the remaining clock LOW period, the 9310 • 9316 will perform a mixture of counting and loading. On the LOW to HIGH clock transition, outputs $Q_0 \ldots Q_3$ will change as the count sequence or the loading requires. Only the outputs that would not change in the count sequence and are also reloaded with their present value stay constant.

LOGIC DIAGRAM
9310

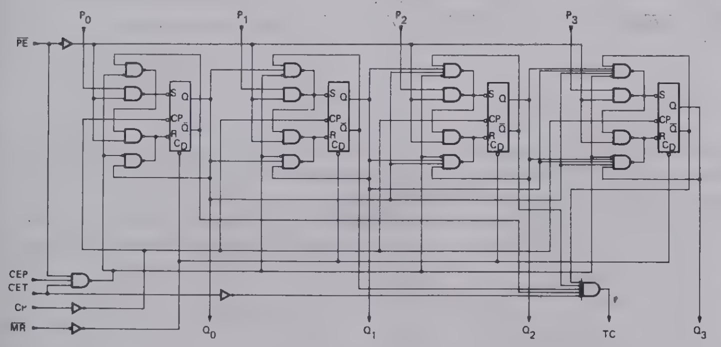


9310 AND 9316
MODE SELECTION

$\overline{\text{PE}}$	CEP	CET	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{\text{MR}}$ = HIGH)

9316



TERMINAL COUNT GENERATION

CET	9310 $(Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3)$	9316 $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$	TC
L	L	L	L
L	H	H	L
H	L	L	L
H	H	H	H

$TC = CET \bullet Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$ (9310)

$TC = CET \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$ (9316)

POSITIVE LOGIC = H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9310XM • 9316XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9310XC • 9316XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input Logical HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input Logical LOW Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −640 μA for Q I_{OH} = −800 μA for TC V_{IN} = V_{IH} or V_{IL}
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 12.8 mA for Q I_{OL} = 16 mA for TC V_{IN} = V_{IH} or V_{IL}
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V
	$\overline{MR}$, CEP		10	40		
	CP, $\overline{PE}$, CET		20	80		
	P_0, P_1, P_2 & P_3		7	27		
	Input HIGH Current all Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.4 V
	$\overline{MR}$, CEP		−0.96	−1.6		
	CP, $\overline{PE}$, CET		−1.92	−3.2		
	P_0, P_1, P_2 & P_3		−0.64	−1.07		
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−50	−80	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		65	94	mA	9310XM • 9316XM — V_{CC} = MAX., MR = 0V Other Inputs HIGH
			65	100	mA	9310XC • 9316XC

NOTES
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions testing, not shown in table, are chosen to guarantee operation under "worst case" conditions.
3. The Specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay CP to Q		12	20	ns	See Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PHL}	Turn On Delay CP to Q		15	23	ns		
t_{PLH}	Turn Off Delay CP to TC		25	35	ns	See Fig. 4	
t_{PHL}	Turn On Delay CP to TC		13	22	ns		
t_{PLH}	Turn Off Delay CET to TC		13	19	ns	See Fig. 3	
t_{PHL}	Turn On Delay CET to TC		13	19	ns		
t_{PHL}	Turn On Delay $\overline{MR}$ to Q		30	45	ns	See Fig. 2	
f_{count}	Input Count Frequency	30	45		MHz	See Fig. 1	

SWITCHING SET-UP REQUIREMENTS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{rec}	Recovery Time for $\overline{MR}$	15	11		ns	See Fig. 2	$V_{CC} = 5.0$ V
$t_{pw}\overline{MR}$	Master Reset Pulse Width	30	23		ns		
$t_{pw}CP$	Clock Pulse Width	17	11		ns	See Fig. 1	
t_s(H) or (L)	Set-up Time Data to Clock	30	20		ns	See Fig. 5	
t_h(H) or (L)	Hold Time Data to Clock	0	−19		ns		
t_s(H)	Set-up Time (HIGH) CE to Clock	22	11		ns	See Fig. 6	
t_h(H)	Hold Time (HIGH) CE to Clock	See Note 6					
t_s(L)	Set-up Time (LOW) CE to Clock	See Note 6					
t_h(L)	Hold Time (LOW) CE to Clock	0	−10		ns		
t_s(H)	Set-up Time (HIGH) $\overline{PE}$ to Clock	See Note 7					
t_h(H)	Hold Time (HIGH) $\overline{PE}$ to Clock	− 7	−19		ns		
t_s(L)	Set-up Time (LOW) $\overline{PE}$ to Clock	30	20		ns		
t_h(L)	Hold Time (LOW) $\overline{PE}$ to Clock	See Note 7					

6. The Set-up Time "t_s(L)" and Hold Time "t_h(H)" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH to LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.
7. The Set-Up Time "t_s(H)" and Hold Time "t_h(L)" between the Parallel Enable (PE) and the Clock (CP) indicate that the LOW to HIGH transition of the PE must occur only while the Clock is HIGH for conventional operation.

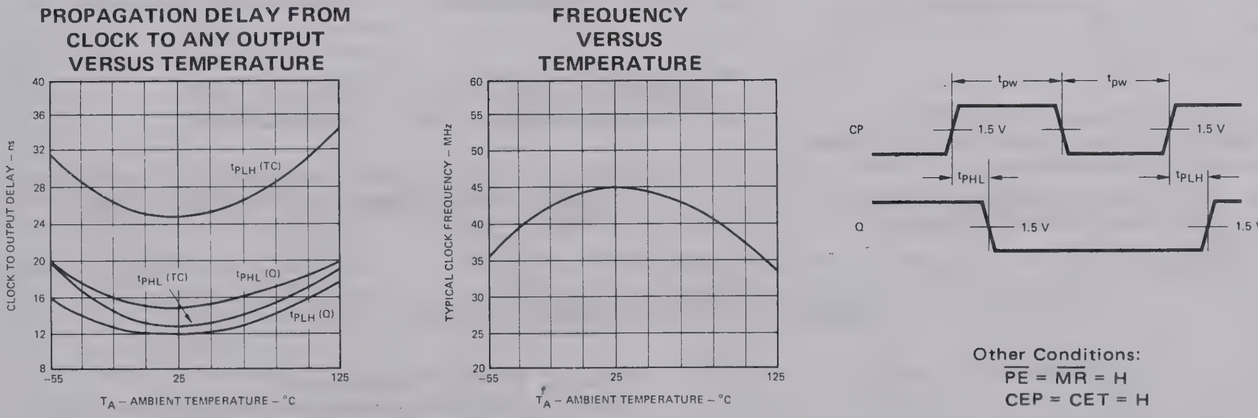
DEFINITION OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

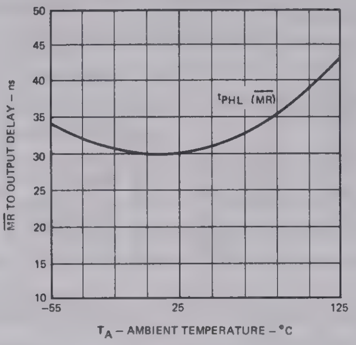
TYPICAL SWITCHING CHARACTERISTICS


PROPAGATION DELAY FROM CLOCK TO ANY OUTPUT VERSUS TEMPERATURE

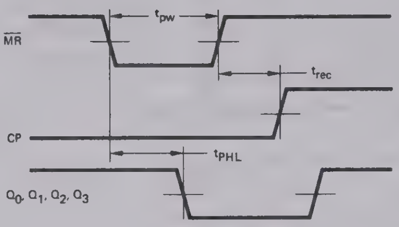
FREQUENCY VERSUS TEMPERATURE

Other Conditions:
$\overline{PE} = \overline{MR} = H$
CEP = CET = H

Fig. 1 CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY AND CLOCK PULSE WIDTH



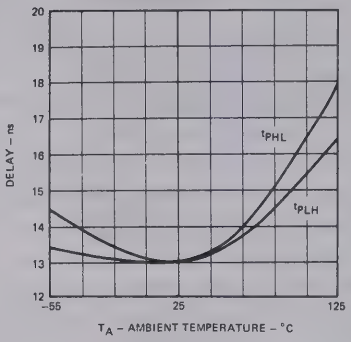
PROPAGATION DELAY FROM MASTER RESET TO OUTPUT VERSUS TEMPERATURE



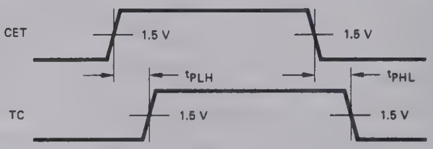
MR
tpw
trec
CP
tPHL
Q0, Q1, Q2, Q3

Other Conditions:
$\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2. MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.



PROPAGATION DELAY COUNT ENABLE TERMINAL TO TERMINAL COUNT

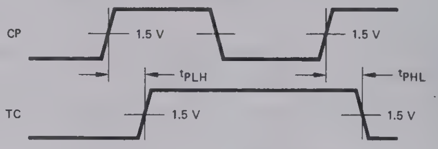


CET
1.5 V
1.5 V
tPLH
tPHL
TC
1.5 V
1.5 V

Other Conditions: CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H

The positive TC pulse occurs when the otuputs are in the $(Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3)$ state for the 9310 and the $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ state for the 9316.

Fig. 3. COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS.

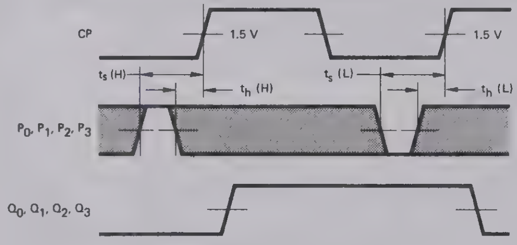


CP
1.5 V
1.5 V
tPLH
tPHL
TC
1.5 V
1.5 V

Other Conditions: $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H

The positive TC pulse is coincident with the output state $(Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3)$ for the 9310 and $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ for the 9316.

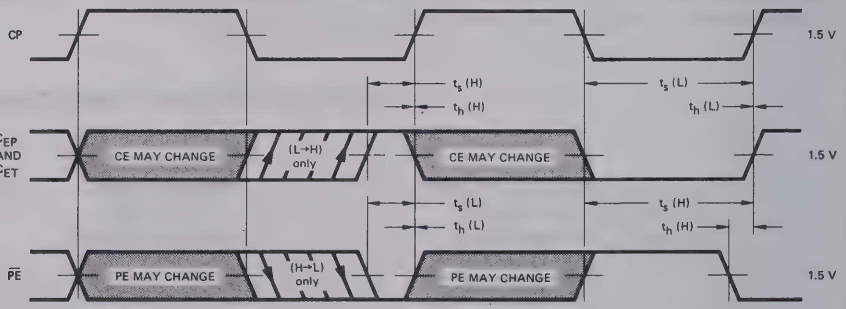
Fig. 4. CLOCK TO TERMINAL COUNT DELAYS.



CP
1.5 V
1.5 V
ts (H)
th (H)
ts (L)
th (L)
P0, P1, P2, P3
Q0, Q1, Q2, Q3

Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H
The shaded areas indicate when the input is permitted to change for predictable output performance.

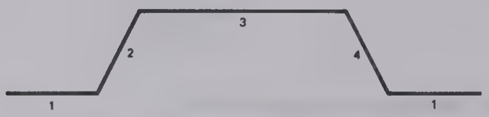
Fig. 5. SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.



CP
1.5 V
ts (H)
th (H)
ts (L)
th (L)
CEP AND CET
CE MAY CHANGE
(L→H) only
CE MAY CHANGE
1.5 V
ts (L)
th (L)
ts (H)
th (H)
PE
PE MAY CHANGE
(H→L) only
PE MAY CHANGE
1.5 V

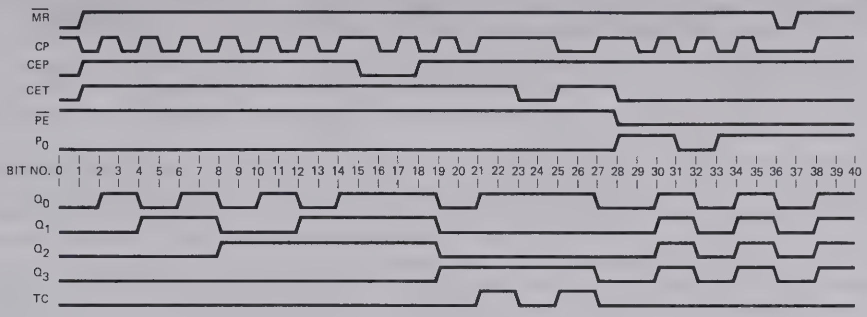
Fig. 6. SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ($\overline{PE}$) INPUTS.

Fig. 7. CLOCK PULSE CHARACTERISTICS.



Region 1: Enter R&S data into master
Region 2: Inhibit R&S inputs, transfer data from master to slave
Region 3: Latch master and slave
Region 4: Isolate slave from master, enable R&S inputs

9310 GENERALIZED FUNCTION TEST


MR
CP
CEP
CET
PE
P0
BIT NO. 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40
Q0
Q1
Q2
Q3
TC

MULTISTAGE COUNTING — The 9310 • 9316 counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in Figures 8 and 9.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The 9310 • 9316 internally decodes the terminal count condition and "ANDs" it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage, Figure 8. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in Figure 9 permits multistage counting up to 11 stages limited by the fan out of the terminal count. For an alternate scheme for more stages see Application Note 184.

The CEP input of the 9310 • 9316 is internally "ANDed" with the CET input and as a result, both must be HIGH for the counter to be enabled. The CET inputs are connected as before except for the second stage. There the CET input is left floating and is therefore HIGH. Also, all CEP inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (HIGH), all CEP inputs are activated, allowing all stages to count on the next clock.

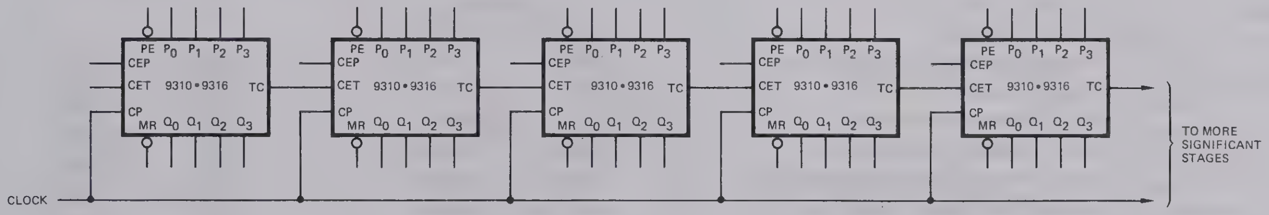

PE P0 P1 P2 P3
CEP
CET 9310•9316 TC
CP
MR Q0 Q1 Q2 Q3
TO MORE SIGNIFICANT STAGES
CLOCK

Fig. 8. SYNCHRONOUS MULTISTAGE COUNTING SCHEME (SLOW)

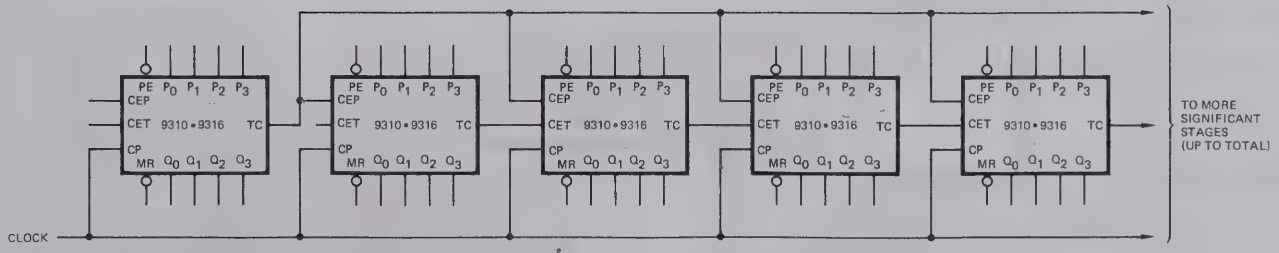

PE P0 P1 P2 P3
CEP
CET 9310•9316 TC
CP
MR Q0 Q1 Q2 Q3
TO MORE SIGNIFICANT STAGES (UP TO TOTAL)
CLOCK

Fig. 9. SYNCHRONOUS MULTISTAGE COUNTING SCHEME (FAST)

LPTTL/MSI 93L10 · 93L16

LOW POWER BCD DECADE COUNTER/4-BIT BINARY COUNTER

DESCRIPTION — The **93L10** is a High Speed Synchronous BCD Decade Counter and the **93L16** is a High Speed Synchronous 4-Bit Binary Counter. They are synchronously presetable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

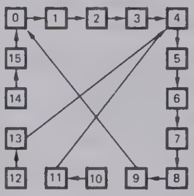
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **TYPICAL COUNTING FREQUENCY OF 20 MHz**
- **TYPICAL POWER DISSIPATION OF 85 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, AND TTL FAMILIES**
- **INPUT DIODE CLAMPING**
- **TTL COMPATIBLE**

PIN NAMES		**LOADING** HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	0.33 U.L.	0.17 U.L.
CEP	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	1.0 U.L.	0.5 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	8.0 U.L.	2.0 U.L.
TC	Terminal Count Outputs	8.0 U.L.	2.0 U.L.

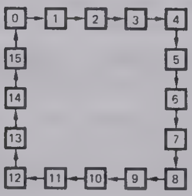
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

STATE DIAGRAM

93L10


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

93L16


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

LOGIC EQUATIONS

Count Enable = CEP · CET · PE

TC for 93L10 = CET · $Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3$

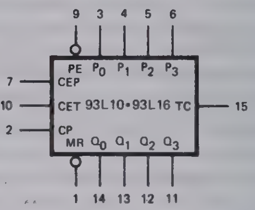
TC for 93L16 = CET · $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$

Preset = $\overline{PE}$ · CP+ (rising clock edge)

Reset = $\overline{MR}$

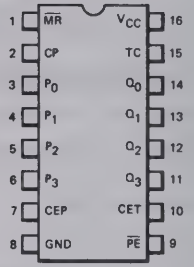
NOTE:
The 93L10 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

LOGIC SYMBOL

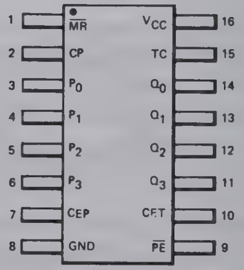

9
3
4
5
6
PE
P_0
P_1
P_2
P_3
7
CEP
10
CET
93L10•93L16
TC
15
2
CP
MR
Q_0
Q_1
Q_2
Q_3
1
14
13
12
11

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1
$\overline{MR}$
V_{CC}
16
2
CP
TC
15
3
P_0
Q_0
14
4
P_1
Q_1
13
5
P_2
Q_2
12
6
P_3
Q_3
11
7
CEP
CET
10
8
GND
$\overline{PE}$
9

FLATPAK (TOP VIEW)


1
$\overline{MR}$
V_{CC}
16
2
CP
TC
15
3
P_0
Q_0
14
4
P_1
Q_1
13
5
P_2
Q_2
12
6
P_3
Q_3
11
7
CEP
CET
10
8
GND
$\overline{PE}$
9

FUNCTIONAL DESCRIPTION — The 93L10 is a high speed BCD Decade Counter, and the 93L16 is a high speed Binary Counter. Both counters are fully synchronous with the clock pulse driving four master/slave flip-flops in parallel through a clock buffer. During the LOW to HIGH transition of the clock, the master is inhibited from further change. After the masters are locked out, data is transferred from the master to the slaves and reflected at the outputs. When the clock is HIGH, the masters are inhibited and the master/slave data path remains established. During the HIGH to LOW transition of the clock, the slave is inhibited from further change, followed bv the enabling of the masters for the acceptance of data from the counting logic or the parallel entry logic. (See Clock Pulse Characteristics **Figure 7.**)

The three control inputs, Parallel Enable ($\overline{PE}$), Count Enable Parrallel (CEP), and Count Enable Trickle (CET), select the mode of operation as shown in the tables below. When the conditions for counting are satisfied, the rising edge of a clock pulse will change the counters to the next state of the count sequence shown in the State Diagram on the previous page. The Count Mode is enabled when CEP and CET inputs and $\overline{PE}$ are HIGH.

The 93L10 and 93L16 can be synchronously preset from the four Parallel inputs, ($P_{0\text{-}3}$) when $\overline{PE}$ is LOW. When the Parallel Enable and Clock are LOW, each master of the flip-flops is connected to the appropriate parallel input (P_{0-3}) and the slaves (outputs) are steady in their previous state. When the clock goes HIGH, the masters are inhibited and this information is transferred to the slaves and reflected at the outputs. The parallel enable input overrides both count enable inputs, presetting the counter when LOW.

Terminal count is HIGH when the counter is at terminal count (state 9 for 93L10, and state 15 for 93L16), and Count Enable Trickle is HIGH, as is shown in the logic equations. Without additional logic, multistage synchronous counting at high speeds is made possible with a high speed lookahead technique utilizing the count enable and terminal count logic. A multistage counter illustrating these techniques is shown and discussed in the application section.

When LOW, the asynchronous master reset overrides all other inputs resetting the four outputs LOW.

Conventional operation of the 93L10•93L16, as shown in the Mode Selection table, requires that the mode control inputs ($\overline{PE}$, CEP, CET) are stable while the clock is LOW. This is no constraint for a normal synchronous system where all signals are generated by the rising edge of the clock.

For some applications, the designer may want to change those inputs while the clock is LOW. In this case the 93L10•93L16 will behave in a predictable manner. For example:

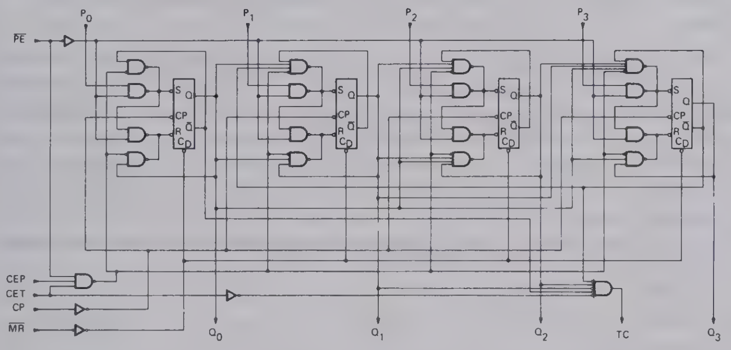
If $\overline{PE}$ goes HIGH while the clock is LOW, but Count Enable is not active during the remaining clock LOW period (i.e. CEP or CET are LOW), the subsequent LOW to HIGH clock transition will change $Q_0 \ldots Q_3$ to the $P_0 \ldots P_3$ data that existed at the set-up time before the rising edge of $\overline{PE}$.

If Count Enable is active (i.e. CEP and CET are HIGH) during some portion of the clock LOW period, but $\overline{PE}$ is HIGH (inactive) during the entire clock LOW period, the subsequent LOW to HIGH clock transition will change $Q_0 \ldots Q_3$ to the next count value.

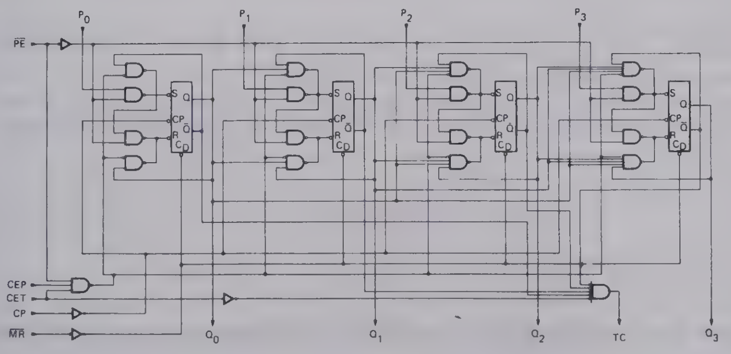
If $\overline{PE}$ goes HIGH while the clock is LOW, but Count Enable is active (CEP and CET are HIGH) during some portion of the remaining clock LOW period, the 93L10•93L16 will perform a mixture of counting and loading. On the LOW to HIGH clock transition, outputs $Q_0 \ldots Q_3$ will change as the count sequence or the loading requires. Only the outputs that would not change in the count sequence and are also reloaded with their present value stay constant.

LOGIC DIAGRAMS

93L10



93L16



93L10 AND 93L16 MODE SELECTION

$\overline{PE}$	CEP	CET	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

TERMINAL COUNT GENERATION

CET	93L10 ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$)	93L16 ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$)	TC
L	L	L	L
L	H	H	L
H	L	L	L
H	H	H	H

TC = CET • $Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$ (93L10)

TC = CET • $Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$ (93L16)

POSITIVE LOGIC = H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L10XM·93L16XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L10XC·93L16XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA $V_{IN} = V_{IH}$ or V_{IL}
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA $V_{IN} = V_{IH}$ or V_{IL}
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.3 V
	$\overline{MR}$, CEP		−0.25	−0.40		
	CP, $\overline{PE}$, CET		−0.50	−0.80		
	P_0, P_1, P_2 & P_3		−0.13	−0.27		
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V
	$\overline{MR}$, CEP		2.0	20		
	CP, $\overline{PE}$, CET		4.0	40		
	P_0, P_1, P_2 & P_3		1.0	13.3		
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		17	27.5	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

COUNTING APPLICATIONS

For typical counting applications, see Multistage Counter and Synchronous Multistage Counting Scheme in 9310·9316 data sheet in TTL/MSI section of this catalog.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{PLH} t_{PHL}	Turn Off Delay CP to Q Turn On Delay CP to Q		20 26	32 39	ns ns	See Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Turn Off Delay CP to TC Turn On Delay CP to TC		44 20	66 30	ns ns	See Fig. 4	
t_{PLH} t_{PHL}	Turn Off Delay CET to TC Turn On Delay CET to TC		20 20	30 30	ns ns	See Fig. 3	
t_{PHL}	Turn On Delay MR to Q		40	72	ns	See Fig. 2	
f_{count}	Input Count Frequency	13	23		MHz	See Fig. 1	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{rec} t_{pw}MR	Recovery Time for MR Master Reset Pulse Width	30 35	20 20		ns ns	See Fig. 2	V_{CC} = 5.0 V
t_{pw}CP	Clock Pulse Width	25	15		ns	See Fig. 1	
t_s(H) or (L) t_h(H) or (L)	Set-up Time Data to Clock Hold Time Data to Clock	75 0	50 −20		ns ns	See Fig. 5	
t_s(H)	Set-up Time (HIGH) CE to Clock	26	17		ns	See Fig. 6	
t_h(H) t_s(L)	Hold Time (HIGH) CE to Clock Set-up Time (LOW) CE to Clock	See Note 6 See Note 6					
t_h(L)	Hold Time (LOW) CE to Clock	0	−17		ns		
t_s(H)	Set-up Time (HIGH) PE to Clock	See Note 7					
t_h(H)	Hold Time (HIGH) PE to Clock	0	−35		ns		
t_s(L)	Set-up Time (LOW) PE to Clock	53	35		ns		
t_h(L)	Hold Time (LOW) PE to Clock	See Note 7					

NOTES:

6. The Set-up Time "t_s(L)" and Hold Time "t_h(H)" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH to LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.
7. The Set-up Time "t_s(H)" and Hold Time "t_h(L)" between the Parallel Enable (PE) and the Clock (CP) indicate that the LOW to HIGH transition of the PE must occur only while the clock is HIGH for conventional operation.

DEFINITION OF TERMS:

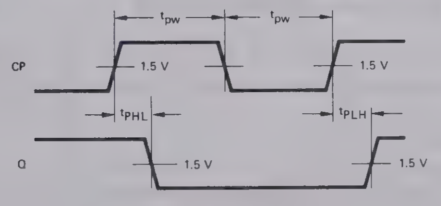
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SWITCHING CHARACTERISTICS

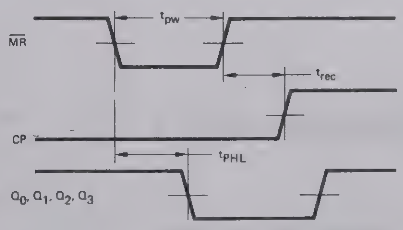
CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.



Other Conditions:
$\overline{PE}$ = $\overline{MR}$ = H
CEP = CET = H

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.



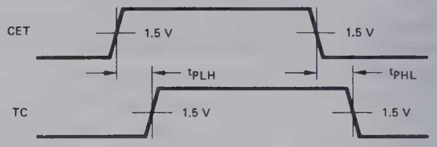
Other Conditions:
$\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2

SWITCHING CHARACTERISTICS (cont'd)

COUNT ENABLE TRÍCKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS.

The positive TC pulse occurs when the outputs are in the $(Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3)$ state for the 93L10 and the $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ state for the 93L16.

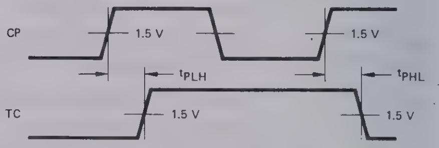

CET
1.5 V
1.5 V
t_{PLH}
t_{PHL}
TC
1.5 V
1.5 V

Other Conditions: $CP = \overline{PE} = CEP = \overline{MR} = H$

Fig. 3

CLOCK TO TERMINAL COUNT DELAYS.

The positive TC pulse is coincident with the output state $(Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3)$ for the 93L10 and $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ for the 93L16.

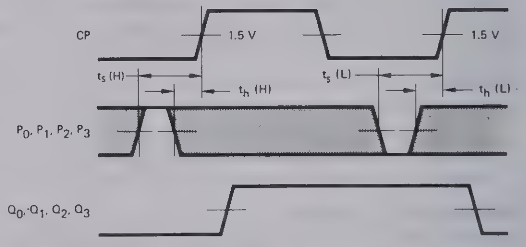

CP
1.5 V
1.5 V
t_{PLH}
t_{PHL}
TC
1.5 V
1.5 V

Other Conditions: $\overline{PE} = CEP = CET = \overline{MR} = H$

Fig. 4

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.


CP
1.5 V
1.5 V
t_s (H)
t_h (H)
t_s (L)
t_h (L)
P_0, P_1, P_2, P_3
Q_0, Q_1, Q_2, Q_3

Other Conditions: $\overline{PE} = L$, $\overline{MR} = H$

Fig. 5

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ($\overline{PE}$) INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

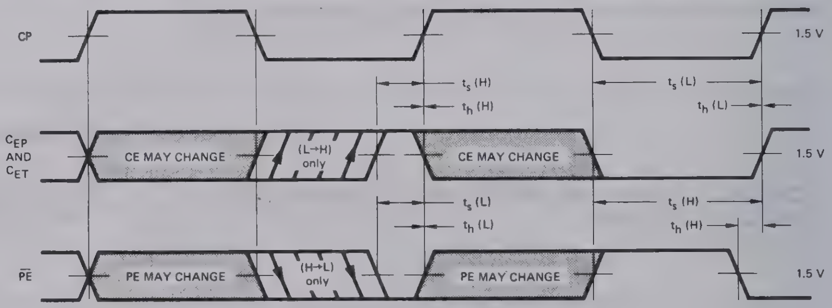

CP
1.5 V
t_s (H)
t_h (H)
t_s (L)
t_h (L)
C_{EP} AND C_{ET}
CE MAY CHANGE
(L→H) only
CE MAY CHANGE
1.5 V
t_s (L)
t_h (L)
t_s (H)
t_h (H)
$\overline{PE}$
PE MAY CHANGE
(H→L) only
PE MAY CHANGE
1.5 V

Fig. 6

CLOCK PULSE CHARACTERISTICS.

Region 1: Enter R&S data into master
Region 2: Inhibit R&S inputs, transfer data from master to slave
Region 3: Latch master and slave
Region 4: Isolate slave from master, enable R&S inputs

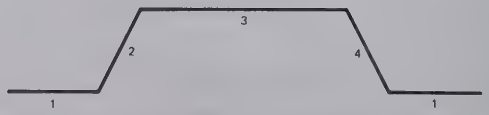


Fig. 7

TTL/MSI 93S10 •93S16

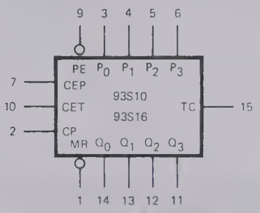
BCD DECADE COUNTER/4-BIT BINARY COUNTER

TO BE ANNOUNCED

DESCRIPTION — The 93S10 is a super high speed synchronous BCD Decade Counter and the 93S16 is a super high speed synchronous 4-Bit Binary Counter. They are synchronously presetable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several stages of sunchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique. Each device utilizes Schottky TTL processing to achieve the ultra high speeds.

- **TYPICAL COUNTING FREQUENCY OF 100 MHz**
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **THE INPUT/OUPTUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, AND TTL FAMILIES**
- **INPUT DIODE CLAMPING**

LOGIC SYMBOL



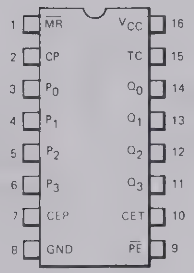
9
3
4
5
6
PE
P_0
P_1
P_2
P_3
7
CEP
10
CET
93S10
93S16
TC
15
2
CP
MR
Q_0
Q_1
Q_2
Q_3
1
14
13
12
11

V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

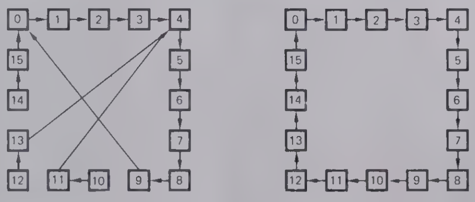
$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0, P_1, P_2, P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock (Active HIGH) Going Edge Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
TC	Terminal Count Outputs

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1
$\overline{MR}$
2
CP
3
P_0
4
P_1
5
P_2
6
P_3
7
CEP
8
GND
16
V_{CC}
15
TC
14
Q_0
13
Q_1
12
Q_2
11
Q_3
10
CET
9
$\overline{PE}$

STATE DIAGRAM



0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

93S10

93S16

LOGIC EQUATIONS

Count Enable = CEP • CET • PE

TC for 93S10 = CET • Q_0 • $\overline{Q}_1$ • $\overline{Q}_2$ • Q_3

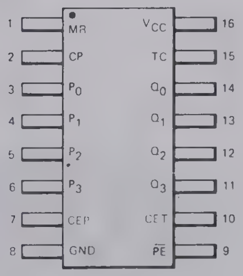
TC for 93S16 = CET • Q_0 • Q_1 • Q_2 • Q_3

Preset = $\overline{PE}$ • CP+ (rising clock edge)

Reset = $\overline{MR}$

NOTE:
The 93S10 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

FLATPAK (TOP VIEW)



1
MR
2
CP
3
P_0
4
P_1
5
P_2
6
P_3
7
CEP
8
GND
16
V_{CC}
15
TC
14
Q_0
13
Q_1
12
Q_2
11
Q_3
10
CET
9
$\overline{PE}$

TTL/MSI 9311

ONE-OF-SIXTEEN DECODER/DEMULTIPLEXER

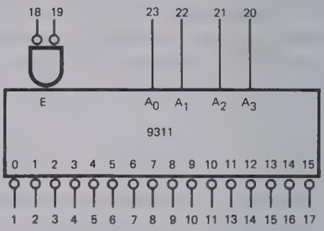
DESCRIPTION — The 9311 is a TTL/MSI Multi-Purpose Decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The circuit uses TTL for high speed and high fan out capability, and is compatible with all members of the Fairchild TTL family.

- **MUTUALLY EXCLUSIVE OUTPUTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 175 mW**
- **INPUT CLAMP DIODES**
- **2-INPUT ENABLE GATE**
- **TTL COMPATIBLE**

PIN NAMES		**LOADING** (Note a)
A_0, A_1, A_2, A_3	Address Inputs	1 U.L.
$\overline{E}_0, \overline{E}_1$	AND Enable (Active LOW) Inputs	1 U.L.
$\overline{0}$ to $\overline{15}$	(Active LOW) Outputs (Note b)	10 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

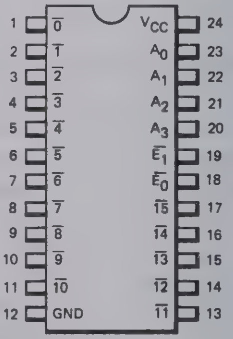
LOGIC SYMBOL



18 19 23 22 21 20
E
A_0 A_1 A_2 A_3
9311
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
1 2 3 4 5 6 7 8 9 10 11 13 14 15 16 17

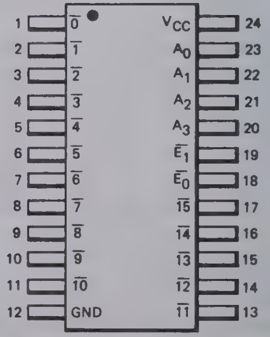
V_{CC} = PIN 24
GND = PIN 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)



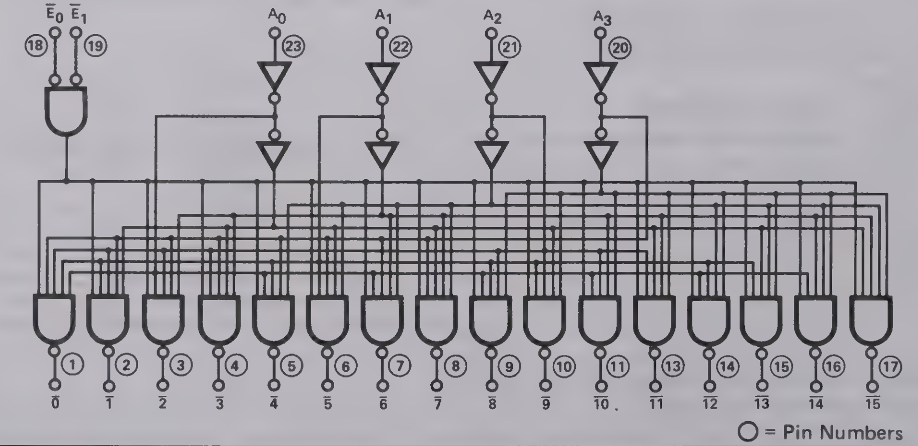
1 $\overline{0}$ V_{CC} 24
2 $\overline{1}$ A_0 23
3 $\overline{2}$ A_1 22
4 $\overline{3}$ A_2 21
5 $\overline{4}$ A_3 20
6 $\overline{5}$ $\overline{E}_1$ 19
7 $\overline{6}$ $\overline{E}_0$ 18
8 $\overline{7}$ $\overline{15}$ 17
9 $\overline{8}$ $\overline{14}$ 16
10 $\overline{9}$ $\overline{13}$ 15
11 $\overline{10}$ $\overline{12}$ 14
12 GND $\overline{11}$ 13

FLATPAK (TOP VIEW)



1 $\overline{0}$ V_{CC} 24
2 $\overline{1}$ A_0 23
3 $\overline{2}$ A_1 22
4 $\overline{3}$ A_2 21
5 $\overline{4}$ A_3 20
6 $\overline{5}$ $\overline{E}_1$ 19
7 $\overline{6}$ $\overline{E}_0$ 18
8 $\overline{7}$ $\overline{15}$ 17
9 $\overline{8}$ $\overline{14}$ 16
10 $\overline{9}$ $\overline{13}$ 15
11 $\overline{10}$ $\overline{12}$ 14
12 GND $\overline{11}$ 13

LOGIC DIAGRAM



$\overline{E}_0$ $\overline{E}_1$
18 19
A_0 23
A_1 22
A_2 21
A_3 20
1 2 3 4 5 6 7 8 9 10 11 13 14 15 16 17
$\overline{0}$ $\overline{1}$ $\overline{2}$ $\overline{3}$ $\overline{4}$ $\overline{5}$ $\overline{6}$ $\overline{7}$ $\overline{8}$ $\overline{9}$ $\overline{10}$ $\overline{11}$ $\overline{12}$ $\overline{13}$ $\overline{14}$ $\overline{15}$
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The 9311 decoder accepts four inputs and provides 16 mutually exclusive active LOW outputs, as shown by the logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW enable.

The 9311 can demultiplex data by routing it from one input to one of 16 possible decoder outputs. The desired output is addressed and the data is applied to one of the enable inputs. Providing that the other enable is LOW, the addressed output will follow the state of the applied data.

TRUTH TABLE

$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{12}$	$\overline{13}$	$\overline{14}$	$\overline{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

TYPICAL SWITCHING PERFORMANCE

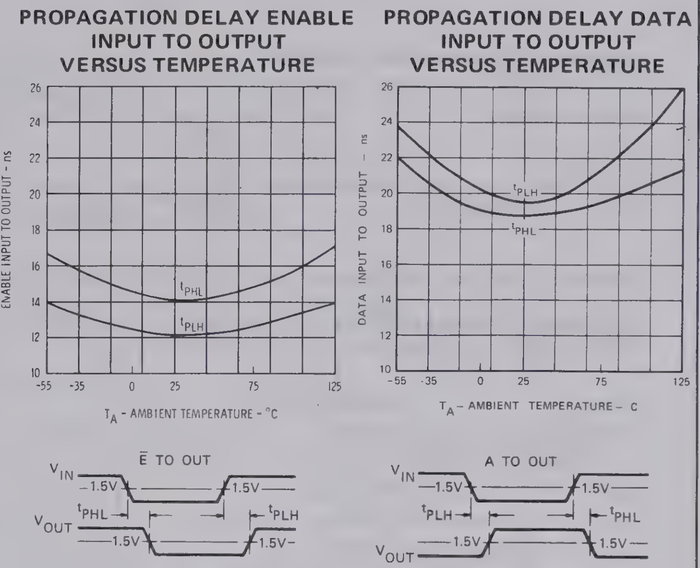
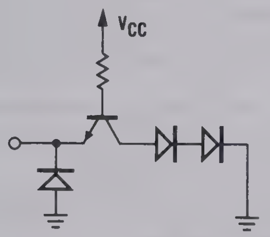


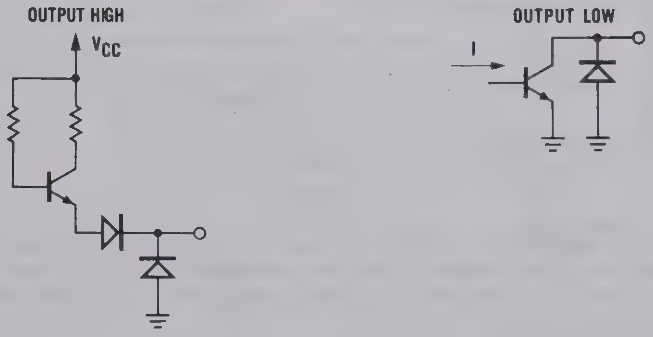
Fig. 1.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

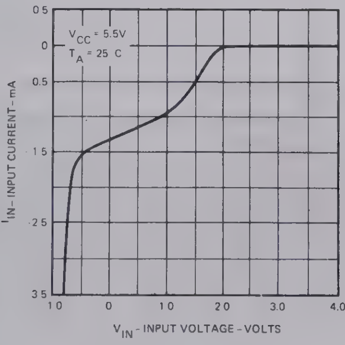


Fig. 2.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH

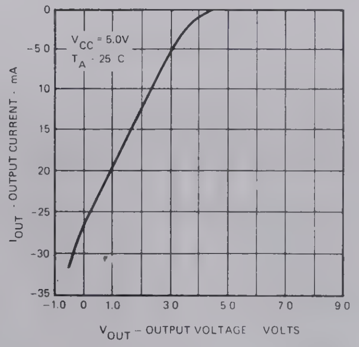


Fig. 3.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

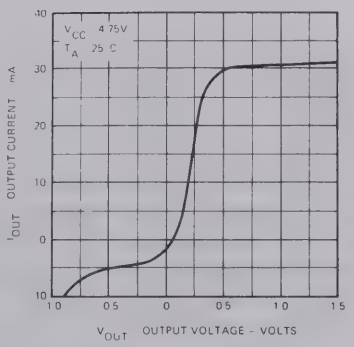


Fig. 4.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9311XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9311XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN}=−12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 µA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−40	−70	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		35	62	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	9311XM			9311XC			UNITS	CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay A Input to Output		19	28		19	31	ns	V_{CC} = 5.0 V C_L = 15 pF Pin 12 = GND (See Fig. 1)
t_{PHL}	Turn On Delay A Input to Output		19	25		19	28		
t_{PLH}	Turn Off Delay $\overline{E}$ Input to Output		12	20		12	23	ns	
t_{PHL}	Turn On Delay $\overline{E}$ Input to Output		14	21		14	24		

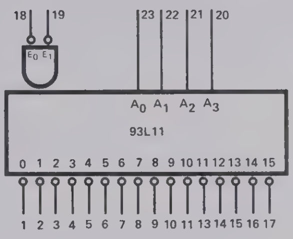
LPTTL/MSI 93L11

LOW POWER ONE-OF-SIXTEEN DECODER

DESCRIPTION — The LPTTL/MSI 93L11 is a Multi-Purpose Decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The circuit uses TTL technology and is compatible with the Fairchild TTL family.

- MULTI-FUNCTION CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- HIGH CAPACITIVE DRIVE CAPABILITY
- DEMULTIPLEXING CAPABILITY
- TWO INPUT ENABLE GATE
- TYPICAL PROPAGATION DELAY OF 70 ns
- TYPICAL POWER DISSIPATION OF 58 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 24-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

LOGIC SYMBOL


18
19
$\overline{E}_0$ $\overline{E}_1$
23
22
21
20
A_0 A_1 A_2 A_3
93L11
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
1 2 3 4 5 6 7 8 9 10 11 13 14 15 16 17

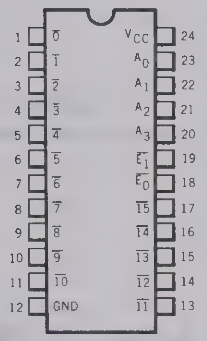
V_{CC} = Pin 24
GND = Pin 12

PIN NAMES		LOADING HIGH	LOADING LOW
A_0, A_1, A_2, A_3	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_0, \overline{E}_1$	AND Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{15}$	(Active LOW) Outputs	10 U.L.	2.5 U.L.

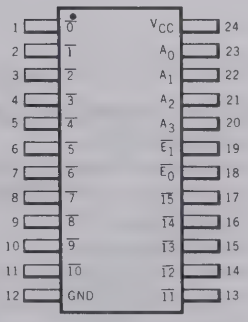
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

CONNECTION DIAGRAMS

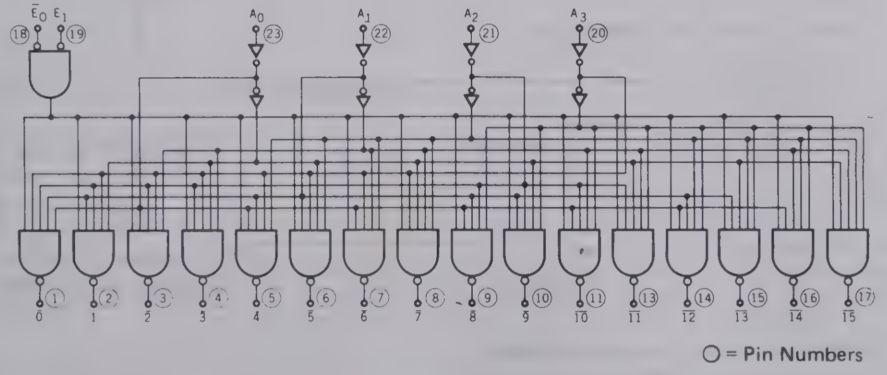
DIP (TOP VIEW)


1 $\overline{0}$
2 $\overline{1}$
3 $\overline{2}$
4 $\overline{3}$
5 $\overline{4}$
6 $\overline{5}$
7 $\overline{6}$
8 $\overline{7}$
9 $\overline{8}$
10 $\overline{9}$
11 $\overline{10}$
12 GND
24 V_{CC}
23 A_0
22 A_1
21 A_2
20 A_3
19 $\overline{E}_1$
18 $\overline{E}_0$
17 $\overline{15}$
16 $\overline{14}$
15 $\overline{13}$
14 $\overline{12}$
13 $\overline{11}$

FLATPAK (TOP VIEW)


1 $\overline{0}$
2 $\overline{1}$
3 $\overline{2}$
4 $\overline{3}$
5 $\overline{4}$
6 $\overline{5}$
7 $\overline{6}$
8 $\overline{7}$
9 $\overline{8}$
10 $\overline{9}$
11 $\overline{10}$
12 GND
24 V_{CC}
23 A_0
22 A_1
21 A_2
20 A_3
19 $\overline{E}_1$
18 $\overline{E}_0$
17 $\overline{15}$
16 $\overline{14}$
15 $\overline{13}$
14 $\overline{12}$
13 $\overline{11}$

LOGIC DIAGRAM


$\overline{E}_0$ $\overline{E}_1$
⑱ ⑲
A_0 ㉓
A_1 ㉒
A_2 ㉑
A_3 ⑳
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪ ⑬ ⑭ ⑮ ⑯ ⑰
$\overline{0}$ $\overline{1}$ $\overline{2}$ $\overline{3}$ $\overline{4}$ $\overline{5}$ $\overline{6}$ $\overline{7}$ $\overline{8}$ $\overline{9}$ $\overline{10}$ $\overline{11}$ $\overline{12}$ $\overline{13}$ $\overline{14}$ $\overline{15}$
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 93L11 decoder accepts four active HIGH binary inputs and provides 16 mutually exclusive active LOW outputs, as shown by logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW enables.

The 93L11 can demultiplex data by routing it from one input to one of sixteen possible decoder outputs. The desired output is addressed and the data is applied to one of the enable inputs. When the other enable is LOW,the addressed output will follow the state of the applied data.

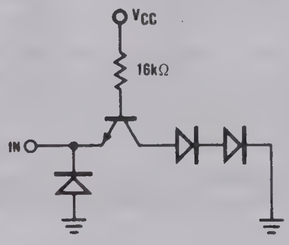
TRUTH TABLE

$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{12}$	$\overline{13}$	$\overline{14}$	$\overline{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

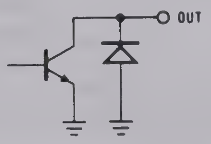
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

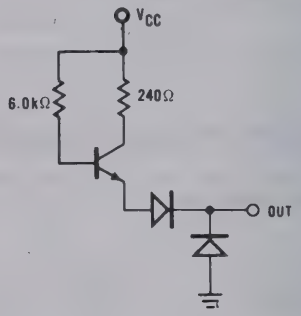


OUTPUTS
EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L11XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L11XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		11.5	16.5	mA	V_{CC} = MAX.

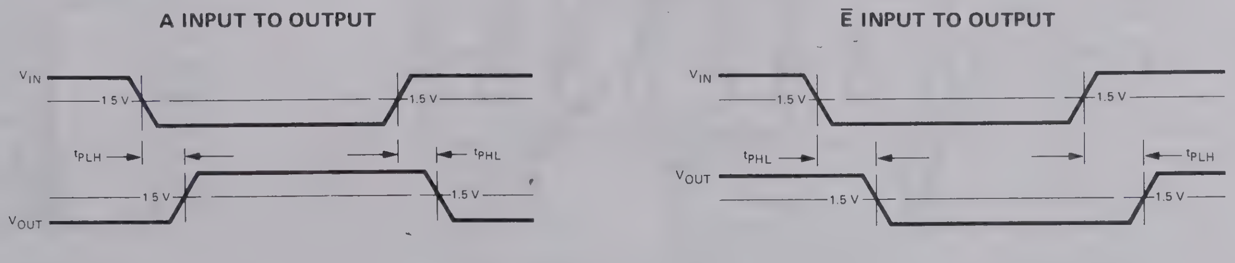
NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay A Input to Output		50	75	ns	V_{CC} = 5.0 V C_L = 15 pF See Fig. 1
t_{PHL}	Turn On Delay A Input to Output		60	85	ns	
t_{PLH}	Turn Off Delay $\overline{E}$ Input to Output		30	60	ns	
t_{PHL}	Turn On Delay $\overline{E}$ Input to Output		43	65	ns	

SWITCHING TIME WAVEFORMS


A INPUT TO OUTPUT

$\overline{E}$ INPUT TO OUTPUT

Fig. 1.

TTL/MSI 9312

EIGHT-INPUT MULTIPLEXER

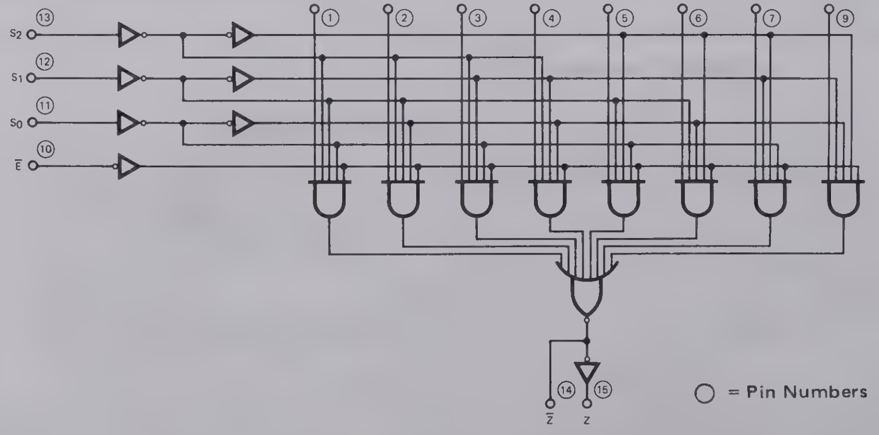
DESCRIPTION — The 9312 is a monolithic, high speed, Eight-Input digital Multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The 9312 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with all other members of the Fairchild TTL family.

- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, and MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

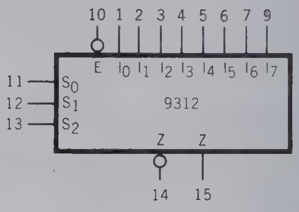
PIN NAMES		**LOADING** (Note a)
S_0, S_1, S_2	Select Inputs	1 U.L.
$\overline{E}$	Enable (Active LOW) Input	1 U.L.
I_0 to I_7	Multiplexer Inputs	1 U.L.
Z	Multiplexer Output (Note b)	10 U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM


I0 I1 I2 I3 I4 I5 I6 I7
1 2 3 4 5 6 7 9
S2 13
S1 12
S0 11
E 10
14 15
Z̄ Z
○ = Pin Numbers

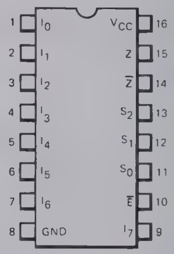
LOGIC SYMBOL


10 1 2 3 4 5 6 7 9
E I0 I1 I2 I3 I4 I5 I6 I7
11 S0
12 S1
13 S2
9312
Z̄ Z
14 15

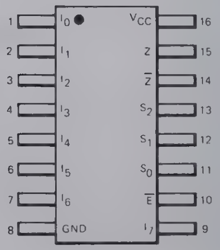
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS

DIP (TOP VIEW)


1 I0
2 I1
3 I2
4 I3
5 I4
6 I5
7 I6
8 GND
16 VCC
15 Z
14 Z̄
13 S2
12 S1
11 S0
10 Ē
9 I7

FLATPAK (TOP VIEW)


1 I0
2 I1
3 I2
4 I3
5 I4
6 I5
7 I6
8 GND
16 VCC
15 Z
14 Z̄
13 S2
12 S1
11 S0
10 Ē
9 I7

FUNCTIONAL DESCRIPTION – The 9312 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three Select Inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable Input ($\bar{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Z = E \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The 9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9312 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one 9312.

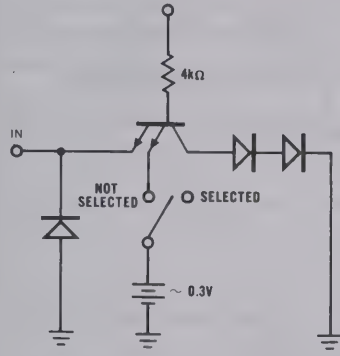
TRUTH TABLE

$\bar{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\bar{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

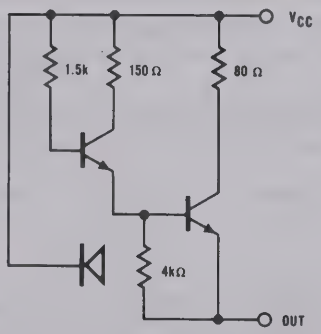
H = HIGH voltage level
L = LOW voltage level
X = Level does not affect output.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

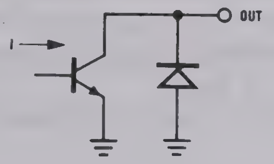
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

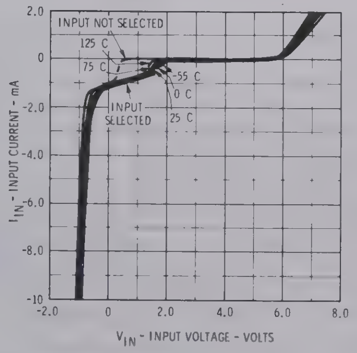


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

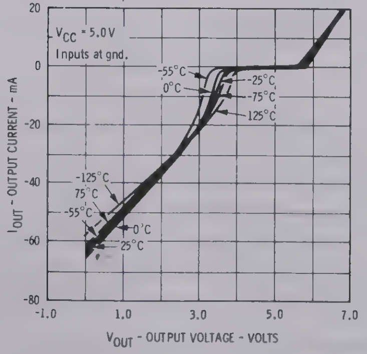


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

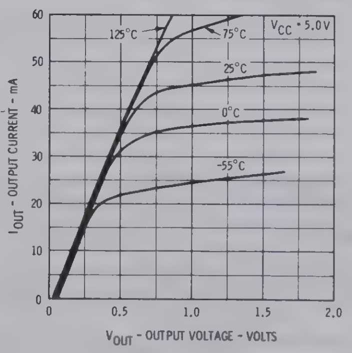


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
*Input Voltage (dc)	−0.5V to +5.5V
*Input Current (dc)	−30mA to +5.0mA
Voltage Applied to Outputs (Output HIGH)	−0.5V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9312XM	4.5V	5.0V	5.5V	−55°C to 125°C
9312XC	4.75V	5.0V	5.25V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC}=MIN., I_{IN}=−12mA, T_A=25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−30	−60	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0V
I_{CC}	Power Supply Current		27	44	mA	V_{CC} = MAX.

NOTES:

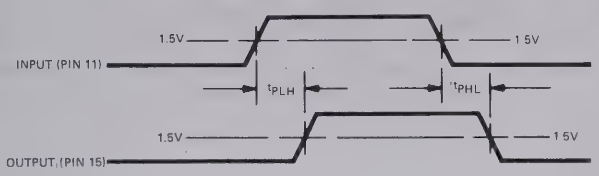
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output (S_0 to Z)		23	34	ns	V_{CC} = 5.0V C_L = 15 pF (See following page)
t_{PHL}	Turn On Delay Input to Output (S_0 to Z)		25	36	ns	

SWITCHING CHARACTERISTICS

t_{PLH}/t_{PHL} : S_0 to Z


1.5V
1.5V
INPUT (PIN 11)
tPLH
tPHL
1.5V
1.5V
OUTPUT (PIN 15)

OTHER CONDITIONS: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

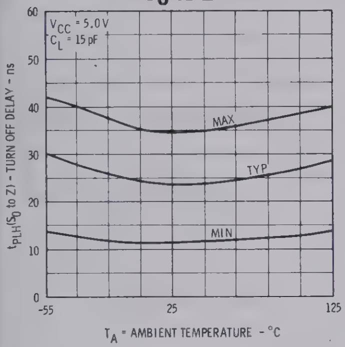


Fig. 4

TURN ON DELAY VERSUS AMBIENT TEMPERATURE: S_0 to Z

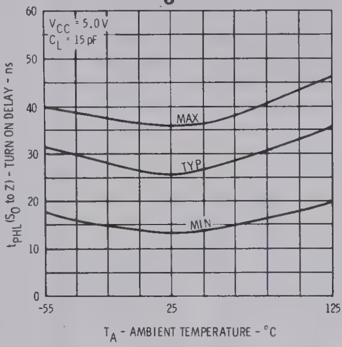
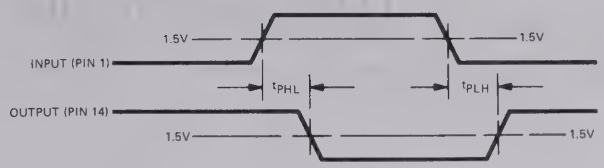


Fig. 5

t_{PLH}/t_{PHL} : I_0 to $\bar{Z}$


1.5V
1.5V
INPUT (PIN 1)
tPHL
tPLH
OUTPUT (PIN 14)
1.5V
1.5V

OTHER CONDITIONS: Pins 8, 10, 11, 12, 13 = GND
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\bar{Z}$

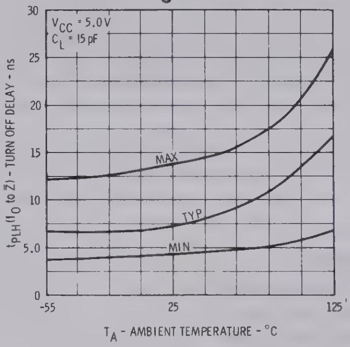


Fig. 6

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\bar{Z}$

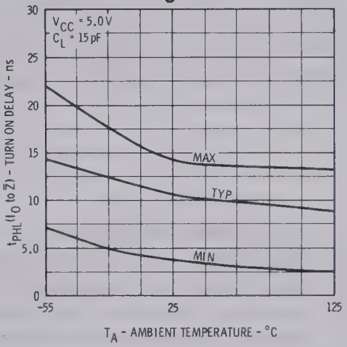
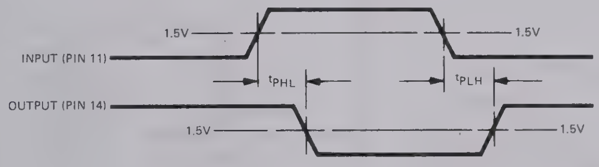


Fig. 7

t_{PLH}/t_{PHL}: S_0 to $\bar{Z}$


1.5V
1.5V
INPUT (PIN 11)
tPHL
tPLH
OUTPUT (PIN 14)
1.5V
1.5V

OTHER CONDITIONS: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE: S_0 to $\bar{Z}$

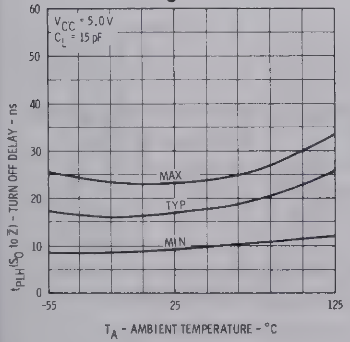


Fig. 8

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\bar{Z}$

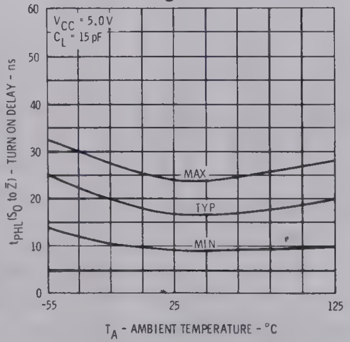
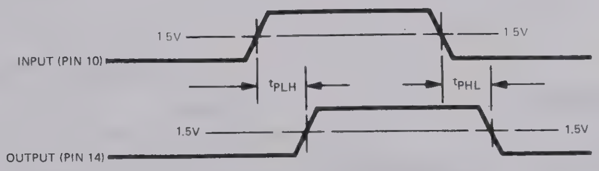


Fig. 9

t_{PLH}/t_{PHL}: $\bar{E}$ to $\bar{Z}$


1.5V
1.5V
INPUT (PIN 10)
tPLH
tPHL
1.5V
1.5V
OUTPUT (PIN 14)

OTHER CONDITIONS: Pins 8, 11, 12, 13 = GND
Pin 1 = V_{CC} through 1 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; $\bar{E}$ to $\bar{Z}$

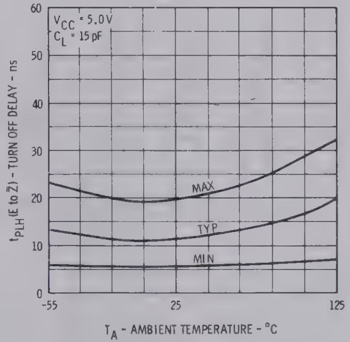


Fig. 10

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; $\bar{E}$ to $\bar{Z}$

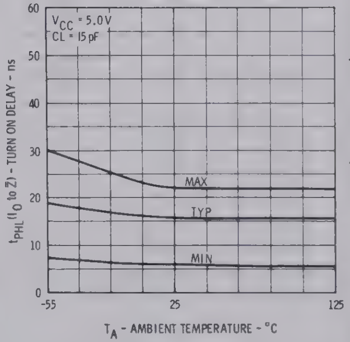


Fig. 11

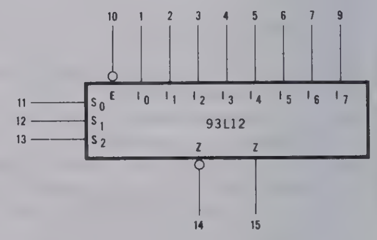
LPTTL/MSI 93L12

LOW POWER EIGHT-INPUT MULTIPLEXER

DESCRIPTION – The LPTTL/MSI 93L12 is a monolithic, medium speed, eight input digital Multiplexer. It provides in one package the ability to select one bit of data from up to eight sources. The 93L12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with the Fairchild TTL family.

- MULTIFUNCTION CAPABILITY •
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS
- TYPICAL PROPAGATION DELAY OF 80 ns
- TYPICAL POWER DISSIPATION OF 45 mW
- INPUT CLAMP DIDOES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

LOGIC SYMBOL


10
1
2
3
4
5
6
7
9
11
12
13
S_0
S_1
S_2
$\overline{E}$
I_0
I_1
I_2
I_3
I_4
I_5
I_6
I_7
93L12
$\overline{Z}$
Z
14
15

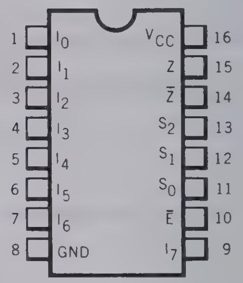
V_{CC} = Pin 16
Gnd = Pin 8

PIN NAMES

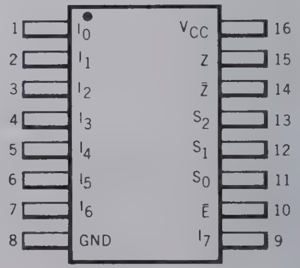
		LOADING	
		HIGH	LOW
S_0, S_1, S_2	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0 to I_7	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output	10 U.L.	2.5 U.L.
$\overline{Z}$	Complementary Multiplexer Output	10 U.L.	2.25 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

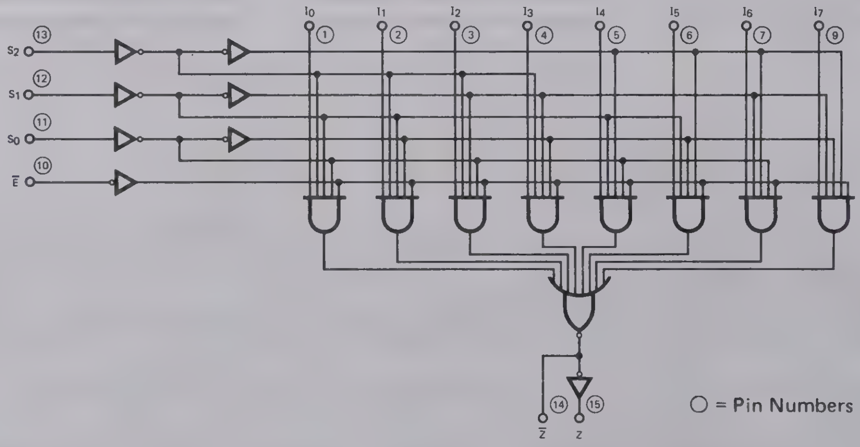
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 I_0
2 I_1
3 I_2
4 I_3
5 I_4
6 I_5
7 I_6
8 GND
16 V_{CC}
15 Z
14 $\overline{Z}$
13 S_2
12 S_1
11 S_0
10 $\overline{E}$
9 I_7

FLATPAK (TOP VIEW)


1 I_0
2 I_1
3 I_2
4 I_3
5 I_4
6 I_5
7 I_6
8 GND
16 V_{CC}
15 Z
14 $\overline{Z}$
13 S_2
12 S_1
11 S_0
10 $\overline{E}$
9 I_7

LOGIC DIAGRAM


S_2 ⑬
S_1 ⑫
S_0 ⑪
$\overline{E}$ ⑩
I_0 ①
I_1 ②
I_2 ③
I_3 ④
I_4 ⑤
I_5 ⑥
I_6 ⑦
I_7 ⑨
$\overline{Z}$ ⑭
Z ⑮

○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 93L12 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = E\cdot(I_0\cdot\overline{S_0}\cdot\overline{S_1}\cdot\overline{S_2} + I_1\cdot S_0\cdot\overline{S_1}\cdot\overline{S_2} + I_2\cdot\overline{S_0}\cdot S_1\cdot\overline{S_2} + I_3\cdot S_0\cdot S_1\cdot\overline{S_2} + I_4\cdot\overline{S_0}\cdot\overline{S_1}\cdot S_2 + I_5\cdot S_0\cdot\overline{S_1}\cdot S_2 + I_6\cdot\overline{S_0}\cdot S_1\cdot S_2 + I_7\cdot S_0\cdot S_1\cdot S_2).$$

The 93L12 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 93L12 can provide any logic function of four variables and its negation.

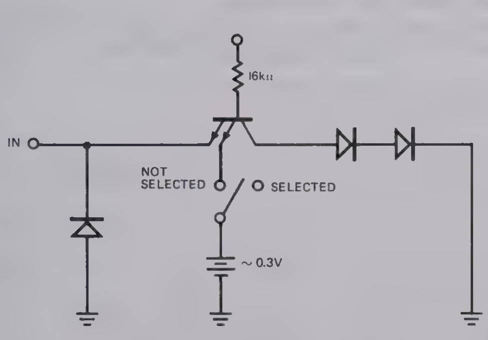
TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

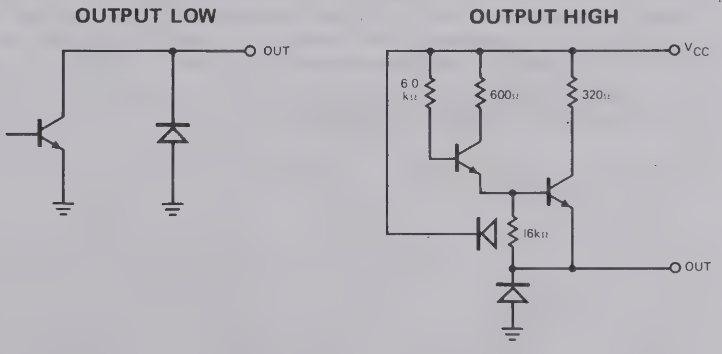
H = HIGH Voltage Level
L = LOW Voltage Level
X = Level does not affect output

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT



OUTPUTS
EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L12XM	4.5 V	5.0 V	5.5 V	–55°C to 125°C
93L12XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pin 15) 3.6 mA (Pin 14) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		–0.25	–0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	–10	–22	–40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		9.0	13.3	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH} (S_0 to Z)	Turn Off Delay Input to Output		52	90	ns	V_{CC} = 5.0 V , C_L = 15 pF
t_{PHL} (S_0 to Z)	Turn On Delay Input to Output		68	105	ns	V_{CC} = 5.0 V, C_L = 15 pF

TTL/MSI 93S12

EIGHT-INPUT MULTIPLEXER

TO BE ANNOUNCED

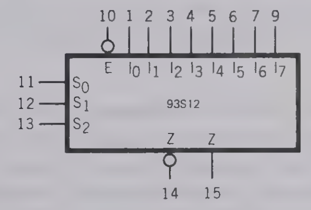
DESCRIPTION — The 93S12 is a monolithic, super high speed, 8-Input digital Multiplexer circuit utilizing the Schottky TTL process. It provides in one package the ability to select one bit of data from up to eight sources. The 93S12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTL circuitry with active pullups on the outputs provides high speed, high fan out operation and is compatible with all other members of the Fairchild TTL family.

- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, and MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

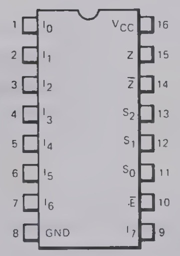
S_0, S_1, S_2	Select Inputs
$\overline{E}$	Enable (Active LOW) Input
I_0 to I_7	Multiplexer Inputs
Z	Multiplexer Output
$\overline{Z}$	Complementary Multiplexer Output

LOGIC SYMBOL

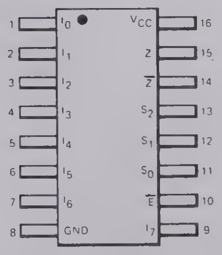

10
1
2
3
4
5
6
7
9
E
I0
I1
I2
I3
I4
I5
I6
I7
11
12
13
S0
S1
S2
93S12
Z
Z
14
15

V_{CC} = pin 16
GND = pin 8

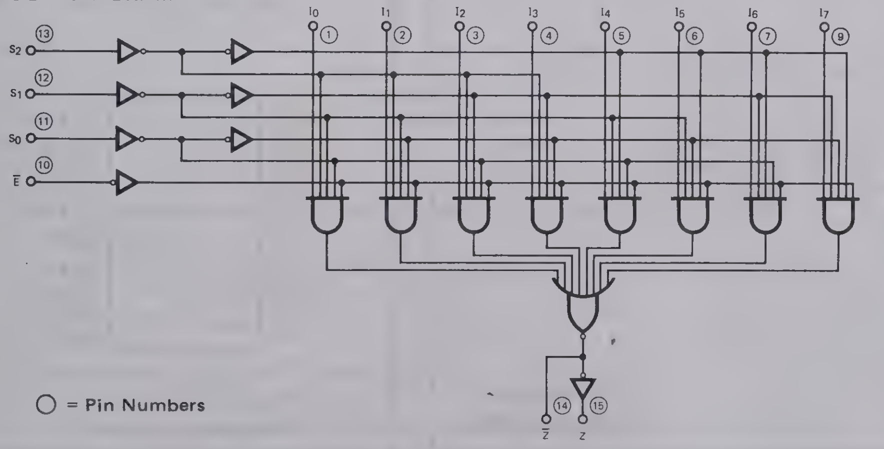
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 I0
2 I1
3 I2
4 I3
5 I4
6 I5
7 I6
8 GND
16 VCC
15 Z
14 Z̄
13 S2
12 S1
11 S0
10 Ē
9 I7

FLATPAK (TOP VIEW)


1 I0
2 I1
3 I2
4 I3
5 I4
6 I5
7 I6
8 GND
16 VCC
15 Z
14 Z̄
13 S2
12 S1
11 S0
10 Ē
9 I7

LOGIC DIAGRAM


S2 13
S1 12
S0 11
Ē 10
I0 1
I1 2
I2 3
I3 4
I4 5
I5 6
I6 7
I7 9
14 Z̄
15 Z
○ = Pin Numbers

TTL/MSI 9313

EIGHT-INPUT MULTIPLEXER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION — The TTL/MSI 9313 is an 8-Input Multiplexer with open collector output. The 9313 has the same pinning and logic configuration as the 9312, but with an open collector $\overline{Z}$ output which allows for easy expansion of input terms. The device can select one bit of data from up to eight sources. It has an active LOW enable, and internal select decoding. The 9313 is fully compatible with all members of the Fairchild TTL family.

- **PIN FOR PIN REPLACEMENT FOR THE SIGNETICS 8231**
- **SAME PINNING AND LOGIC CONFIGURATION AS THE 9312 BUT WITH OPEN COLLECTOR OUTPUT**
- **OPEN COLLECTOR OUTPUT $\overline{Z}$ FOR EASY EXPANSION OF INPUT TERMS (WIRED-OR APPLICATIONS)**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED Z OUTPUT**
- **INPUT CLAMP DIODES**
- **TTL COMPATIBLE**

PIN NAMES		**LOADING** (Note a)
S_0, S_1, S_2	Select Inputs	1 U.L.
$\overline{E}$	Enable (Active LOW) Input	1 U.L.
I_0 to I_7	Multiplexer Inputs	1 U.L.
Z	Multiplexer Output (Note b)	10 U.L.
$\overline{Z}$	Complementary Open Collector Multiplexer Output (Note c)	10 U.L.

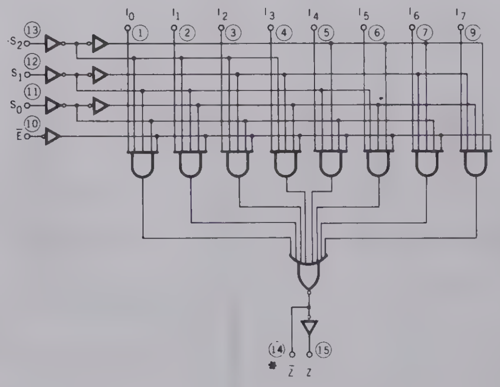
NOTES:

a. 1 Unit Load (U.L.) = 40µA HIGH/1.6mA LOW

b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

c. An external pull-up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at V_{out} = 0.4 V.

LOGIC DIAGRAM

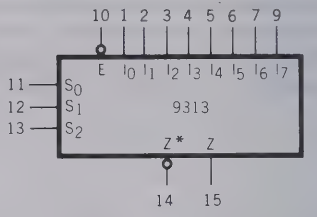


I_0 ① I_1 ② I_2 ③ I_3 ④ I_4 ⑤ I_5 ⑥ I_6 ⑦ I_7 ⑨
⑬ S_2
⑫ S_1
⑪ S_0
⑩ $\overline{E}$
⑭ * $\overline{Z}$
⑮ Z

○ = PIN NUMBERS

*OPEN COLLECTOR

LOGIC SYMBOL



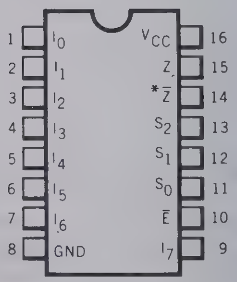
10 1 2 3 4 5 6 7 9
E I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7
11 S_0
12 S_1
13 S_2
9313
Z* Z
14 15

V_{CC} = 16

GND = 8

* OPEN COLLECTOR

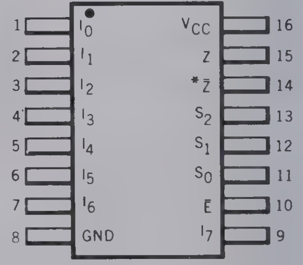
CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 I_0
2 I_1
3 I_2
4 I_3
5 I_4
6 I_5
7 I_6
8 GND
16 V_{CC}
15 Z
14 *$\overline{Z}$
13 S_2
12 S_1
11 S_0
10 $\overline{E}$
9 I_7

* OPEN COLLECTOR

FLATPAK (TOP VIEW)



1 I_0
2 I_1
3 I_2
4 I_3
5 I_4
6 I_5
7 I_6
8 GND
16 V_{CC}
15 Z
14 *$\overline{Z}$
13 S_2
12 S_1
11 S_0
10 $\overline{E}$
9 I_7

* OPEN COLLECTOR

FUNCTIONAL DESCRIPTION — The TTL/MSI 9313 is a logical implementation of a single pole, eight-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. An open collector output $\overline{Z}$ is provided for easy expansion of input terms. Also a fully buffered Z output is available. The Enable input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = E\cdot(I_0\cdot\overline{S}_0\cdot\overline{S}_1\cdot\overline{S}_2 + I_1\cdot S_0\cdot\overline{S}_1\cdot\overline{S}_2 + I_2\cdot\overline{S}_0\cdot S_1\cdot\overline{S}_2 + I_3\cdot S_0\cdot S_1\cdot\overline{S}_2 + I_4\cdot\overline{S}_0\cdot\overline{S}_1\cdot S_2 + I_5\cdot S_0\cdot\overline{S}_1\cdot S_2 + I_6\cdot\overline{S}_0\cdot S_1\cdot S_2 + I_7\cdot S_0\cdot S_1\cdot S_2).$$

The 9313 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9313 can provide any logic function of four variables and its negation.

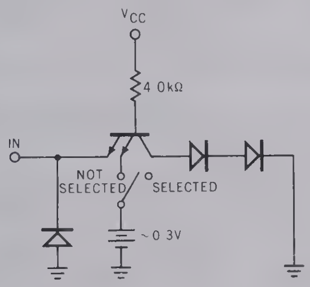
TABLE I TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

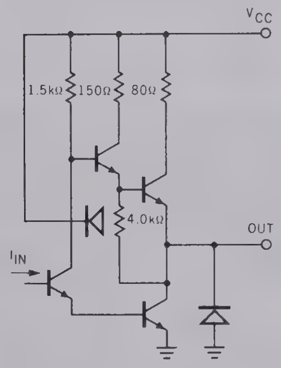
H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

TYPICAL INPUT AND OUTPUT CIRCUITS

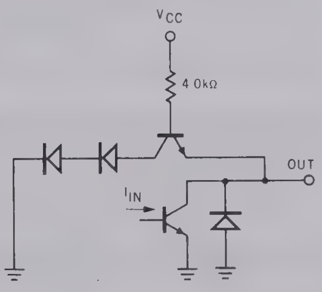
INPUTS
EQUIVALENT CIRCUIT



Z Output (Pin 15)
EQUIVALENT CIRCUIT



$\overline{Z}$ Output (Pin 14)
EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
*Input Voltage (dc)	-0.5V to +5.5V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9313XM	4.5V	5.0V	5.5V	−55°C to 125°C
9313XC	4.75V	5.0V	5.25V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage on Z (Pin 15)	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		-1.0	-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{IH}	Input HIGH Current		5.0	40	μA	V_{CC} = MAX., V_{IN} = 2.4V
			0.02	1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{CEX}	Output HIGH Leakage Current on $\bar{Z}$ (Pin 14)		5.0	150	μA	V_{CC} = 4.5V, V_{OUT} = 4.5V, V_{IN} = 0.6V on Data Input V_{IN} (E & S Inputs) = V_{IL} or V_{IH} per Truth Table
I_{SC}	Output Short Circuit Current on Z (Pin 15)	−30	−75	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0V
I_{CC}	Power Supply Current		28	47	mA	V_{CC} = MAX., I_0-I_7 = GND
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

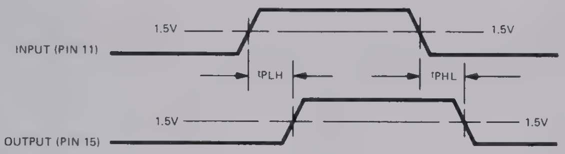
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS				UNITS	CONDITIONS
		9313XM(MIL)		9313XC(IND)			
		TYP.	MAX.	TYP.	MAX.		
t_{PLH} (S_0 to Z)	Turn Off Delay Input to Output	25	32	25	36	ns	V_{CC} = 5.0V
t_{PHL} (S_0 to Z)	Turn On Delay Input to Output	33	40	33	45	ns	C_T = C_L = 15 pF, R_X = 400 Ω to V_{CC}

SWITCHING CHARACTERISTIC CURVES

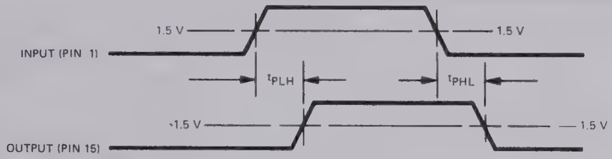
All measurements are made with V_{CC} = 5.0 V applied to pin 16 and with pin 8 grounded.

t_{PLH} / t_{PHL} : S_0 to Z


1.5V
1.5V
INPUT (PIN 11)
tPLH
tPHL
1.5V
1.5V
OUTPUT (PIN 15)

OTHER CONDITIONS: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

t_{PLH} / t_{PHL} : I_0 to Z


1.5 V
1.5 V
INPUT (PIN 1)
tPLH
tPHL
1.5 V
1.5 V
OUTPUT (PIN 15)

OTHER CONDITIONS: Pins 8, 10, 11, 12, 13 = GND
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

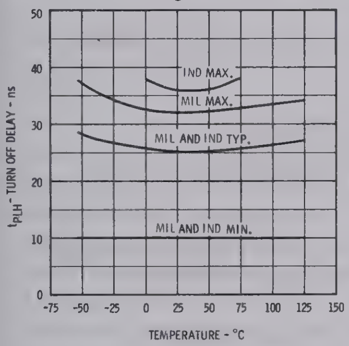


Fig. 1

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

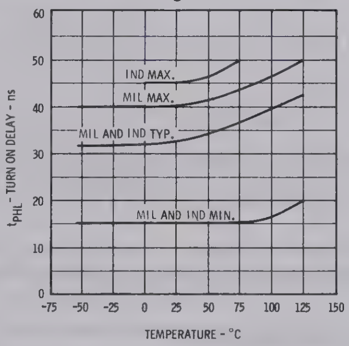


Fig. 2

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

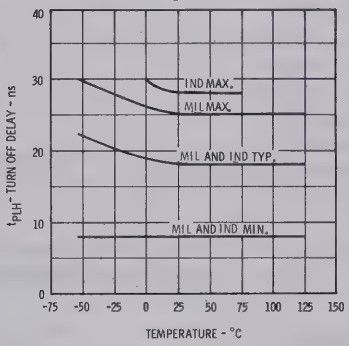


Fig. 3

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

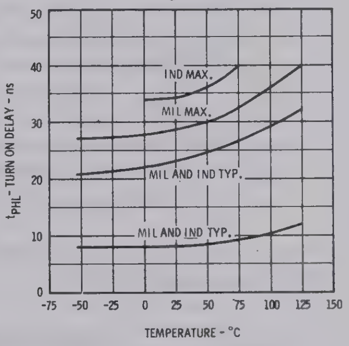
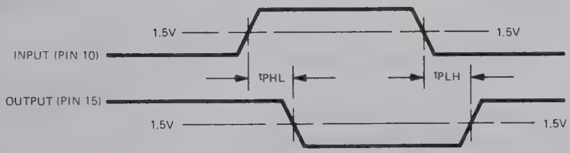


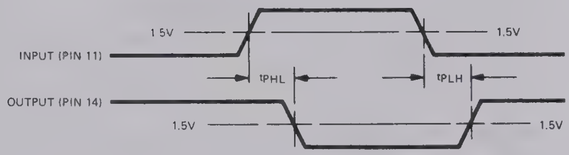
Fig. 4

t_{PLH} / t_{PHL} : $\overline{E}$ to Z


1.5V
1.5V
INPUT (PIN 10)
tPHL
tPLH
OUTPUT (PIN 15)
1.5V
1.5V

OTHER CONDITIONS: Pins 8, 11, 12, 13 = GND
Pin 1 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

t_{PLH} / t_{PHL} : S_0 to $\overline{Z}$


1.5V
1.5V
INPUT (PIN 11)
tPHL
tPLH
OUTPUT (PIN 14)
1.5V
1.5V

OTHER CONDITIONS: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; $\overline{E}$ to Z

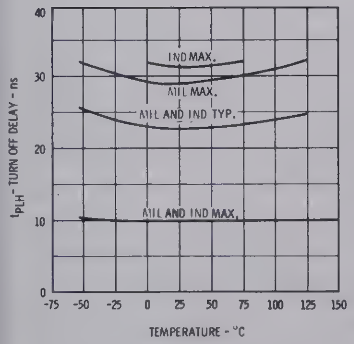


Fig. 5

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; $\overline{E}$ to Z

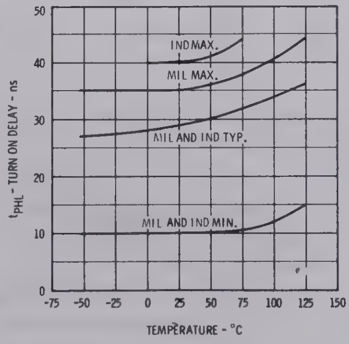


Fig. 6

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

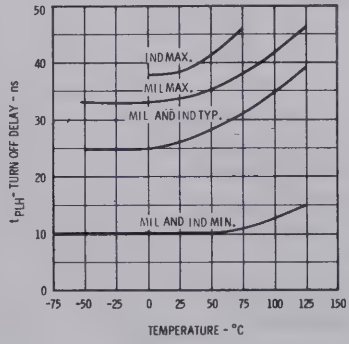


Fig. 7

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

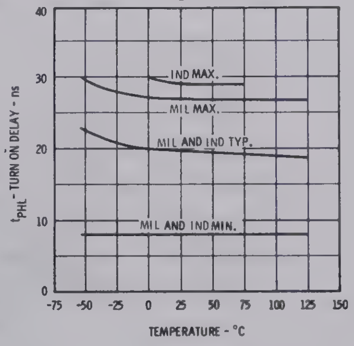


Fig. 8

WIRED-OR APPLICATIONS

It is possible to perform the "Wired OR" function by connecting the open collector $\overline{Z}$ outputs together and adding an external pull up resistor.

The value of the pull up is determined by considering the fanout of the "OR Tie" and the number of devices in the "OR Tie". The pull up resistor value is chosen from a range between a maximum value (determined such that the required V_{OH} is maintained with all the OR tied outputs off) and a minimum value (determined such that with only one output on in the "OR-Tie", its fanout is not exceeded.

Minimum and Maximum Pull up Values

$$R_X\text{ (Min.)} = \frac{V_{CC}\text{ (max.)} - V_{OL}}{I_{OL} - N_2 I_{IL} - (N_1 - 1) I_{IL}}$$

$$R_X\text{ (Max.)} = \frac{V_{CC}\text{ (min.)} - V_{OH}}{N_1 I_{CEX} + N_2 I_{IH}}$$

Where

N_1 = Number of "Wired OR" Outputs
N_2 = Fanout of "OR Tie"
V_{CC} = Power Supply Voltage
R_X = External Pull-up Resistor
I_{CEX} = Output HIGH Leakage Current on $\overline{Z}$ (150 μA)
I_{IH} = Input HIGH Current (40 μA)
I_{IL} = Input LOW Current (1.6 mA)
V_{OL} = Output LOW Voltage (0.4 V)
V_{OH} = Output HIGH Voltage (2.4 V)
I_{OL} = Maximum Current Sinking Capability of Single Output (16 mA)

Example R_L (Min) and R_L (Max.) for four 9313's OR Tied and driving 1 TTL gate. (Industrial V_{CC} tolerances used)

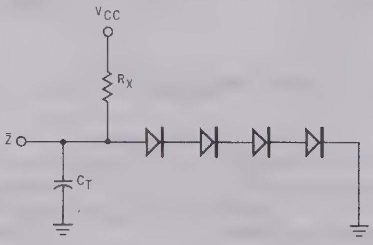
$$R_X\text{ (Min.)} = \frac{5.25\text{ V} - 0.4\text{ V}}{16\text{ mA} - 1\text{ (1.6 mA)} - (4 - 1)\text{ 1.6 mA}} = \frac{4.85\text{V}}{9.6\text{ mA}} = 505\ \Omega$$

$$R_X\text{ (Max.)} = \frac{4.75\text{ V} - 2.4\text{ V}}{4\text{ (150 }\mu\text{A) + 1 (40 }\mu\text{A)}} = \frac{2.35\text{V}}{640\ \mu\text{A}} = 3.7\text{ k}\Omega$$

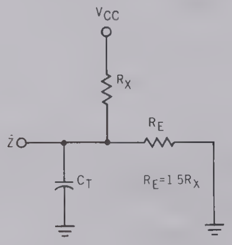
The pull up resistor value (± resistor tolerance) selected should be between these max. and min. values.

Minimum propagation delay results when the minimum value of external pull-up resistor is used in circuit 1. Diodes should be fast recovery 1N4376 or equivalent. External pull-up resistor circuits 2 and 3 give progressively slower propagation delays. (See Figures 9 and 10.)

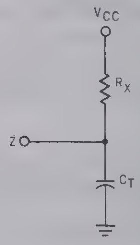
LOAD CIRCUIT 1



LOAD CIRCUIT 2



LOAD CIRCUIT 3



C_T = Total Capacitance at Output

SWITCHING DELTA FOR TURN OFF DELAY (Δt_{PLH}) ANY INPUT TO Z OUTPUT, VERSUS LOAD CAPACITANCE (C_T)

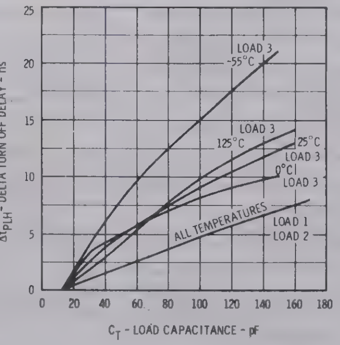


Fig. 9

SWITCHING DELTA FOR TURN ON DELAY (Δt_{PHL}) ANY INPUT TO Z OUTPUT, VERSUS LOAD CAPACITANCE (C_T)

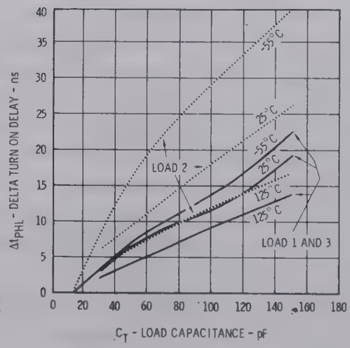


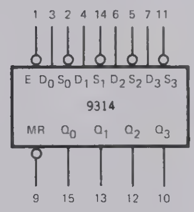
Fig. 10

TTL/MSI 9314
QUAD LATCH

DESCRIPTION — The MSI 9314 is a multifunctional 4-Bit Latch. The latch is designed for general purpose storage applications in high speed digital systems. All inputs feature diode clamping to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good ac noise immunity.

- **CAN BE USED AS SINGLE INPUT D LATCHES OR SET/RESET LATCHES**
- **ACTIVE LEVEL LOW ENABLE GATE INPUT**
- **OVERRIDING MASTER RESET**
- **25 ns THROUGH DELAY**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE DIRECT INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL

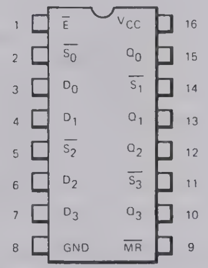

1 3 2 4 14 6 5 7 11
E D0 S0 D1 S1 D2 S2 D3 S3
9314
MR Q0 Q1 Q2 Q3
9 15 13 12 10

V_{CC} = Pin 16
Gnd = Pin 8

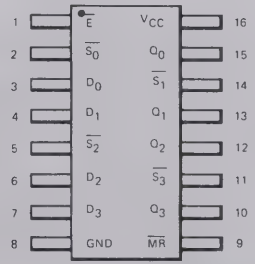
PIN NAMES		**LOADING** (Note a)
$\overline{E}$	(Active LOW) Enable Input	1 U.L.
D_0, D_1, D_2, D_3	Data Inputs	1.5 U.L.
$\overline{S}_0, \overline{S}_1, \overline{S}_2, \overline{S}_3$	Set (Active LOW) Inputs	1 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Latch Outputs (Note b)	10 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

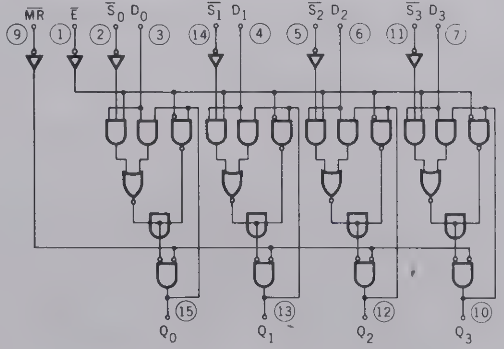
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 E
2 S0
3 D0
4 D1
5 S2
6 D2
7 D3
8 GND
16 VCC
15 Q0
14 S1
13 Q1
12 Q2
11 S3
10 Q3
9 MR

FLATPAK (TOP VIEW)


1 E
2 S0
3 D0
4 D1
5 S2
6 D2
7 D3
8 GND
16 VCC
15 Q0
14 S1
13 Q1
12 Q2
11 S3
10 Q3
9 MR

LOGIC DIAGRAM


MR 9
E 1
S0 2
D0 3
S1 14
D1 4
S2 5
D2 6
S3 11
D3 7
15 Q0
13 Q1
12 Q2
10 Q3

○ = PIN NUMBERS

FUNCTIONAL DESCRIPTION

LATCH OPERATION — The 9314 consists of four latches with a common active LOW enable and active LOW master reset. When the common enable goes HIGH, data present in the latches is stored and the state of a latch is no longer affected by the $\overline{S}$ and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs LOW.

Each of the four latches can be operated in one of two modes:

D TYPE LATCH — For D type operation the $\overline{S}$ input of a latch is held LOW. While the common enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the enable goes HIGH.

SET/RESET LATCH — During set/reset operation when the common enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch will be reset. When the enable goes HIGH, the latch remains in the last state prior to the LOW to HIGH transition.

The two modes of operation of the 9314 latches are shown in the Truth Table below.

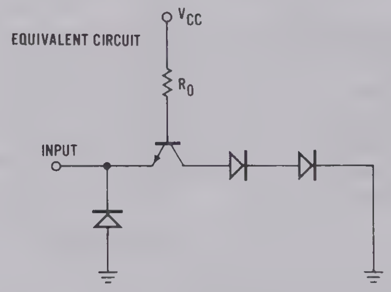
TRUTH TABLE

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_N	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{N-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{N-1}	
H	H	X	X	Q_{N-1}	
L	X	X	X	L	RESET

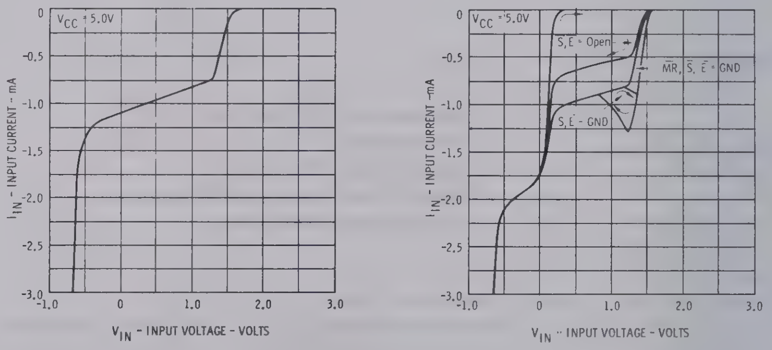
X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State
Q_N = Present Output State

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS

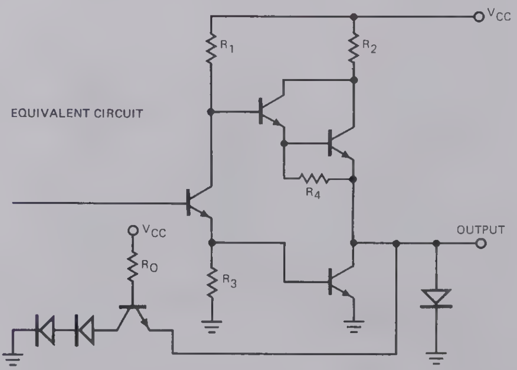


INPUT CURRENT VERSUS INPUT VOLTAGE


$\overline{MR}$, $\overline{E}$, $\overline{S}$

D

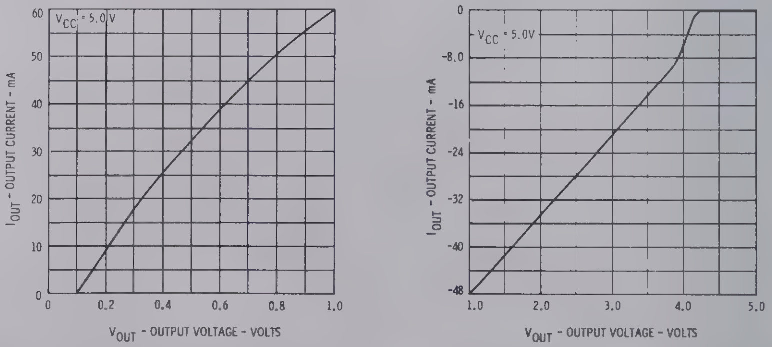
OUTPUTS



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

LOW STATE

HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
9314XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9314XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OL} = −800μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{MR}$, $\overline{E}$, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$, $\overline{S}_3$ D_0, D_1, D_2, D_3		 10 15	 40 60	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current $\overline{MR}$, $\overline{E}$, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$, $\overline{S}_3$		-0.96	-1.6	mA	V_{IN} = 0.4 V, V_{CC} = MAX. (Note 6)
	D_0, D_1, D_2, D_3		-1.9	-2.7	mA	V_{IN} = 0.0 V,
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-20	−40	-70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		35	55	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.

(5) Not more than one output should be shorted at a time.

(6) This current is measured at V_{IN} = 0.0 V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at V_{IN} = 0.4 V is 2.4 mA.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
t_{PLH}	Turn off Delay Enable to Output		18	24	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn on Delay Enable to Output		18	24	ns		
t_{PLH}	Turn off Delay Data to Output		8	12	ns	Fig. 2	
t_{PHL}	Turn on Delay Data to Output		18	24	ns		
t_{PHL}	Turn on Delay MR to Output		12	18	ns	Fig. 5	
t_{PLH}	Turn off Delay Set to Output		18	24	ns	Fig. 7	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	
$t_s(H)$	Set-up Time HIGH Data to Enable	5.0	0		ns	Fig. 3	V_{CC} = 5.0 V
t_h (H)	Hold Time HIGH Data to Enable	0	−12		ns		
$t_s(l)$	Set-up Time LOW Data to Enable	18	13		ns		
$t_h(L)$	Hold Time LOW Data to Enable	5.0	1.0		ns		
$t_{pw}\overline{E}$	Enable Pulse Width	18	12		ns	Fig. 4	
$t_{pw}\overline{MR}$	Master Reset Pulse Width	18	7.0		ns	Fig. 5	
t_{rec}	Recovery Time Master Reset to Enable	0	−7		ns	Fig. 6	
$t_s(H)$	Set-up Time HIGH Data to Set Input	8.0	0		ns	Fig. 7	
$t_h(L)$	Hold Time LOW Data to Set Input	8.0	0		ns		

SET UP TIME: t_s is defined as the minimum time required for the logic level to be present at the Data Input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.

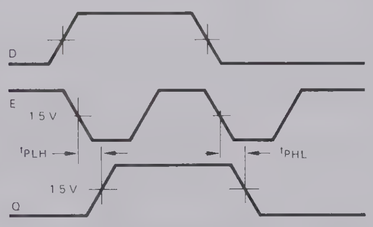
HOLD TIME: t_h is defined as the minimum time following the Enable (E) or Set (S) transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the Enable (E) or Set (S) transition from LOW to HIGH and still be recognized.

RECOVERY TIME: t_{rec} is defined as the minimum time that the Enable must remain LOW after the Master Reset transition from LOW to HIGH in order for the latch to recognize and store HIGH data.

SWITCHING CHARACTERISTICS

All delays are measured with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. Outputs under test are loaded with 15 pF (includes jig and probe). Pins not reference are not connected.

t_{PLH}/t_{PHL} (ENABLE TO OUTPUT)



Other Conditions: $\overline{S}$ = L, $\overline{MR}$ = H

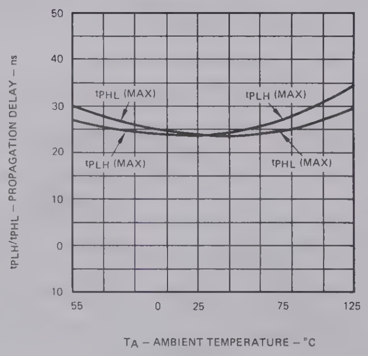
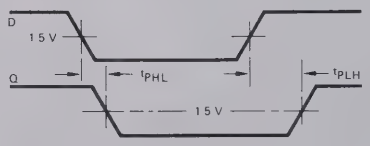


Fig. 1

t_{PLH}/t_{PHL} (DATA TO OUTPUT)



Other Conditions: $\overline{E}$ = L, $\overline{S}$ = L, $\overline{MR}$ = H

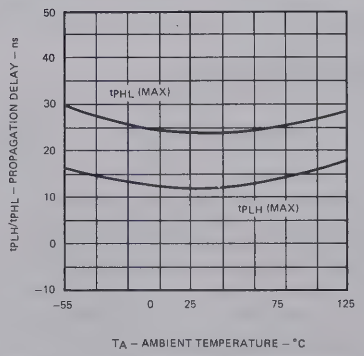
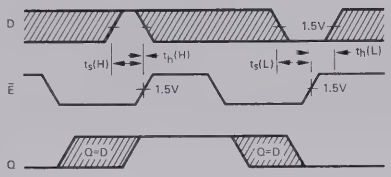


Fig. 2

SWITCHING CHARACTERISTICS

SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO ENABLE


D
1.5V
$t_s(H)$
$t_h(H)$
$t_s(L)$
$t_h(L)$
$\overline{E}$
1.5V
1.5V
Q
Q=D
Q=D

OTHER CONDITIONS: $\overline{MR}$ = H, $\overline{S}$ = L

The shaded areas indicate when the Data input is permitted to change for predictable output performance.

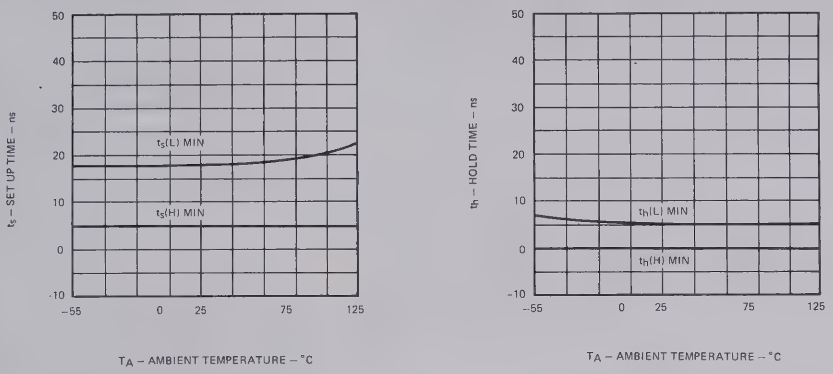
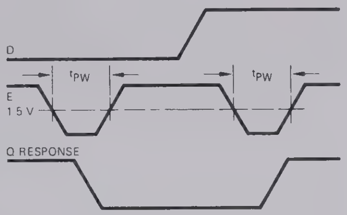


Fig. 3

t_{pw} (MIN. ENABLE PULSE WIDTH)


D
t_{PW}
t_{PW}
E
1.5 V
Q RESPONSE

Other Conditions: $\overline{S}$ = L, $\overline{MR}$ = H

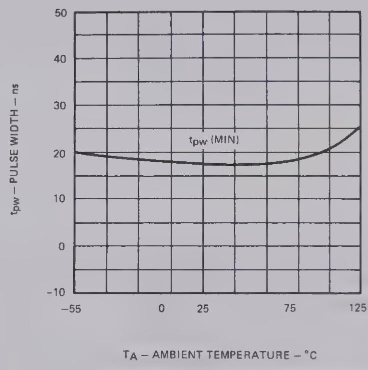
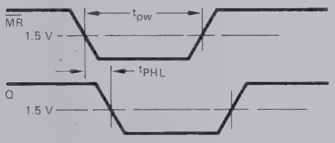


Fig. 4

t_{pw} (MIN. MASTER RESET PULSE WIDTH)
t_{PHL} (MASTER RESET TO OUTPUT)


$\overline{MR}$
1.5 V
t_{pw}
t_{PHL}
Q
1.5 V

Other Conditions: $\overline{S}$ & $\overline{E}$ = L

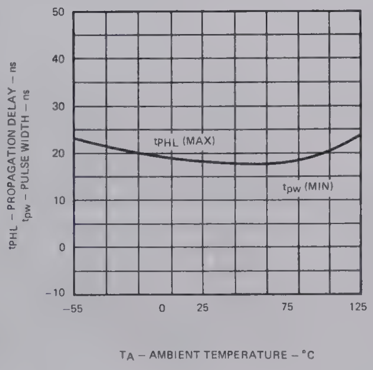
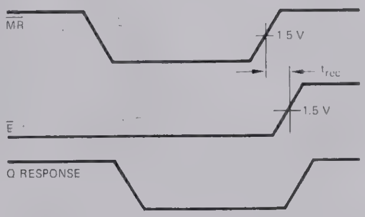


Fig. 5

t_{rec} (MASTER RESET RECOVERY TIME)


$\overline{MR}$
1.5 V
t_{rec}
1.5 V
$\overline{E}$
Q RESPONSE

Other Conditions: $\overline{S}$ = L, D = H

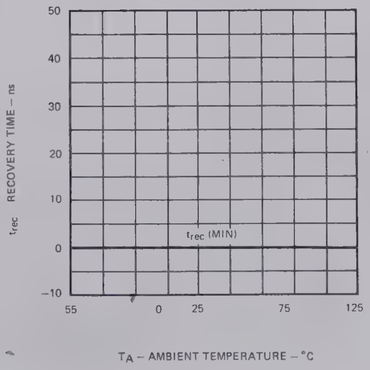
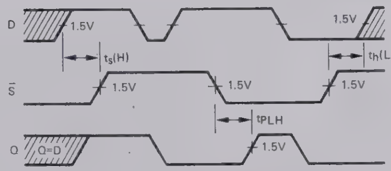


Fig. 6

SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO SET INPUT, AND SET TO OUTPUT DELAY.


D
1.5V
1.5V
$t_s(H)$
$t_h(L)$
$\overline{S}$
1.5V
1.5V
1.5V
t_{PLH}
Q
Q=D
1.5V

OTHER CONDITIONS: $\overline{MR}$ = H, $\overline{E}$ = L

The shaded area indicates when the Data input is permitted to change for predictable output performance.

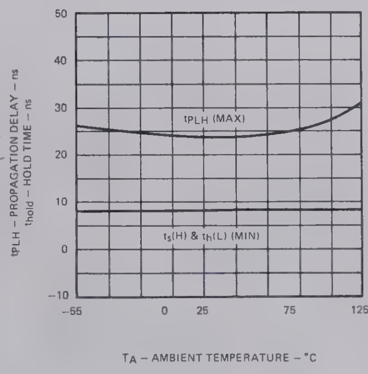


Fig. 7

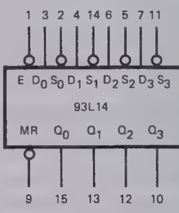
LPTTL/MSI 93L14

LOW POWER QUAD LATCH

DESCRIPTION – The LPTTL/MSI 93L14 is a multifunctional 4-Bit Latch. The latch is designed for general purpose storage applications in high speed digital systems. The 93L14 uses TTL technology and is compatible with the Fairchild TTL family. All inputs feature diode clamping to reduce negative line transients. All outputs have active pull-up circuitry to provide low impedance in both logic states for good ac noise immunity.

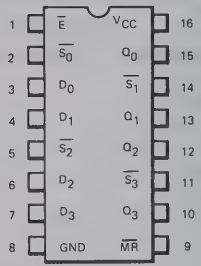
- **CAN BE USED AS SINGLE INPUT D LATCHES OR SET/RESET LATCHES**
- **ACTIVE LEVEL LOW ENABLE GATE INPUT**
- **OVERRIDING MASTER RESET**
- **TYPICAL PROPAGATION DELAY OF 68 ns**
- **TYPICAL POWER DISSIPATION OF 50 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

LOGIC SYMBOL


1 3 2 4 14 6 5 7 11
E D0 S0 D1 S1 D2 S2 D3 S3
93L14
MR Q0 Q1 Q2 Q3
9 15 13 12 10

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)

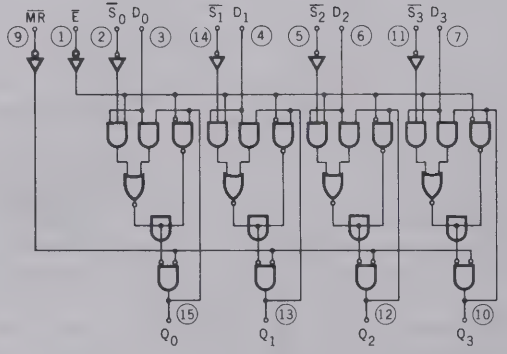

1 Ē
2 S̄0
3 D0
4 D1
5 S̄2
6 D2
7 D3
8 GND
16 VCC
15 Q0
14 S̄1
13 Q1
12 Q2
11 S̄3
10 Q3
9 M̄R̄

PIN NAMES

PIN NAMES		LOADING HIGH	LOADING LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0, D_1, D_2, D_3	Data Inputs	0.75 U.L.	0.375 U.L.
$\overline{S}_0, \overline{S}_1, \overline{S}_2, \overline{S}_3$	Set (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0, Q_1, Q_2, Q_3	Latch Outputs	10 U.L.	2.25 U.L.

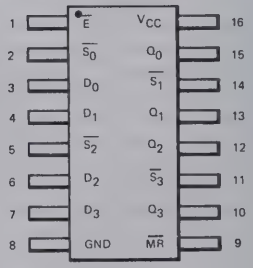
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM


M̄R̄ 9
Ē 1
S̄0 2
D0 3
S̄1 14
D1 4
S̄2 5
D2 6
S̄3 11
D3 7
15 Q0
13 Q1
12 Q2
10 Q3

○ = Pin Numbers

FLATPAK (TOP VIEW)


1 Ē
2 S̄0
3 D0
4 D1
5 S̄2
6 D2
7 D3
8 GND
16 VCC
15 Q0
14 S̄1
13 Q1
12 Q2
11 S̄3
10 Q3
9 M̄R̄

FUNCTIONAL DESCRIPTION

LATCH OPERATION – The 93L14 consists of four latches with a common active LOW enable and active LOW master reset. When the common enable goes HIGH, data present in the latches is stored and the state of a latch is no longer affected by the $\overline{S}$ and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs LOW.

Each of the four latches can be operated in one of two modes:

D TYPE LATCH – For D type operation the $\overline{S}$ input of a latch is held LOW. While the common enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the enable goes HIGH.

SET/RESET LATCH – During set/reset operation when the common enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch will be reset. When the enable goes HIGH, the latch remains in the last state prior to disablement.

The two modes of operation of the 93L14 latches are shown in the Truth Table below.

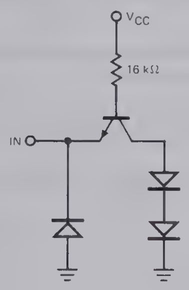
TRUTH TABLE

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_n	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	RESET

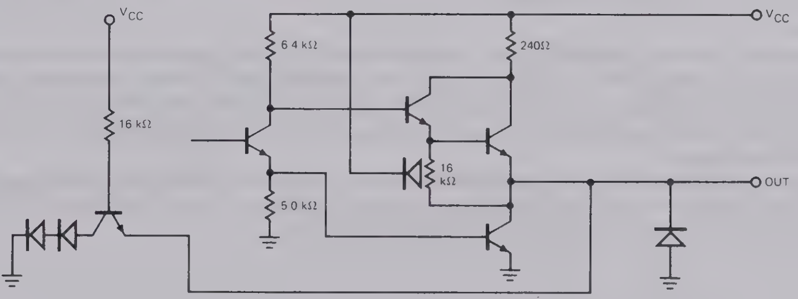
X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{n-1} = Previous Output State
Q_n = Present Output State

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT



OUTPUTS
EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L14XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L14XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 5)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current $\overline{S}$, $\overline{E}$ & $\overline{MR}$		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
	Input LOW Current D Inputs		−0.38	−0.64	mA	V_{CC} = MAX., V_{IN} = 0.0 V (See Note 4)
I_{IH}	Input HIGH Current $\overline{S}$, $\overline{E}$ & $\overline{MR}$ D Inputs		 2.0 3.0	 20 30	µA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 6)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		10	16.5	mA	V_{CC} = MAX., All Outputs LOW, Inputs Disabled

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) This current is measured at V_{IN} = 0.0 V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at V_{IN} = 0.3 V is 0.6 mA.

(5) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

(6) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
t_{PLH}	Turn off Delay Enable to Output		46	80	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn off Delay Enable to Output		51	80	ns		
t_{PLH}	Turn off Delay Data to Output		24	40	ns	Fig. 2	
t_{PHL}	Turn on Delay Data to Output		45	70	ns		
t_{PHL}	Turn on Delay $\overline{MR}$ to Output		28	55	ns	Fig. 5	
t_{PLH}	Turn off Delay Set to Output		35	60	ns	Fig. 7	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

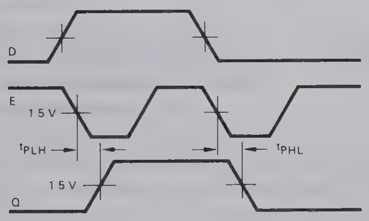
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
$t_s(H)$	Set-up Time HIGH Data to Enable	15	10		ns	Fig. 3	V_{CC} = 5.0 V
$t_h(H)$	Hold Time HIGH Data to Enable	−10	−20		ns		
$t_s(L)$	Set-up Time LOW Data to Enable	30	20		ns		
$t_h(L)$	Hold Time LOW Data to Enable	0	−10		ns		
$t_{pw}E$	Enable Pulse Width	50	30		ns	Fig. 4	
$t_{pw}MR$	Master Reset Pulse Width	45	25		ns	Fig. 5	
t_{rec}	Recovery Time Master Reset to Enable	−20	−40		ns	Fig. 6	
$t_s(H)$	Set-up Time HIGH Data to Set Input	15	10		ns	Fig. 7	
$t_h(L)$	Hold Time LOW Data to Set Input	0	−4		ns		

SET UP TIME: t_s is defined as the minimum time required for the logic level to be present at the Data Input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.
HOLD TIME: t_h is defined as the minimum time following the Enable ($\overline{E}$) or Set ($\overline{S}$) transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the Enable ($\overline{E}$) or Set ($\overline{S}$) transition from LOW to HIGH and still be recognized.
RECOVERY TIME: t_{rec} is defined as the minimum time that the Enable must remain LOW after the Master Reset transition from LOW to HIGH in order for the latch to recognize and store HIGH data. A negative Recovery Time indicates that the Enable may go HIGH prior to the Master Reset transition from LOW to HIGH and still retain HIGH data.

TYPICAL SWITCHING CHARACTERISTICS

All delays are measured with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. Outputs under test are loaded with 15 pF (includes jig and probe). Pins not reference are not connected.

t_{PLH}/t_{PHL} (ENABLE TO OUTPUT)



Other Conditions: $\overline{S}$ = L, $\overline{MR}$ = H

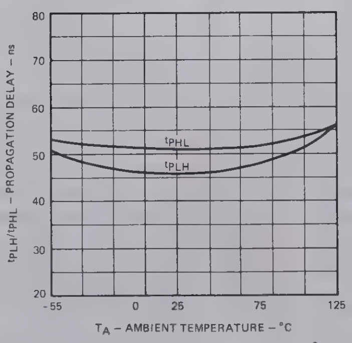
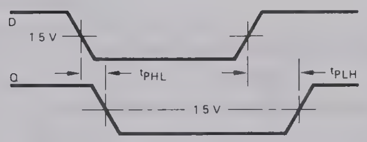


Fig. 1.

t_{PLH}/t_{PHL} (DATA TO OUTPUT)



Other Conditions: $\overline{E}$ = L, $\overline{S}$ = L, $\overline{MR}$ = H

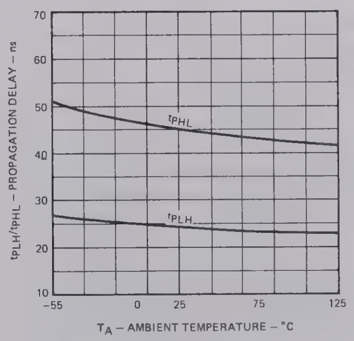
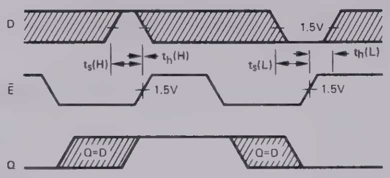


Fig. 2.

SWITCHING CHARACTERISTICS

SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO ENABLE


D
1.5V
$t_s(H)$
$t_h(H)$
$t_s(L)$
$t_h(L)$
Ē
1.5V
1.5V
Q
Q=D
Q=D

OTHER CONDITIONS: $\overline{MR}$ = H, $\overline{S}$ = L

The shaded areas indicate when the Data input is permitted to change for predictable output performance.

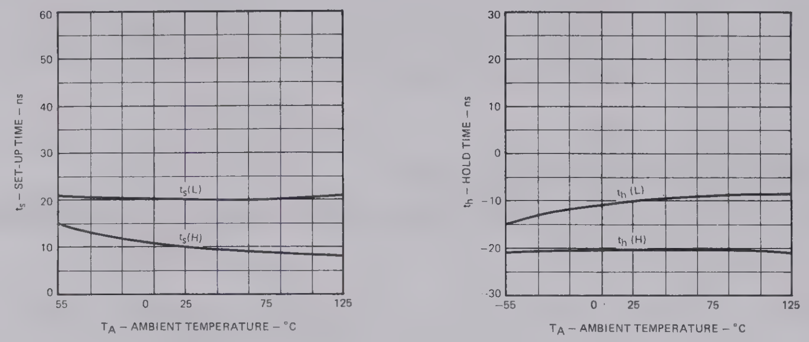
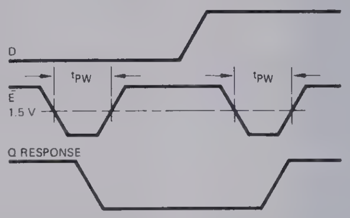


Fig. 3

t_{pw} (MIN. ENABLE PULSE WIDTH)


D
t_{PW}
t_{PW}
Ē
1.5 V
Q RESPONSE

Other Conditions: $\overline{S}$ = L, $\overline{MR}$ = H

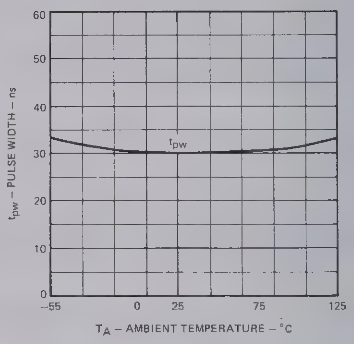
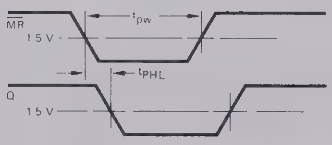


Fig. 4

t_{pw} (MIN. MASTER RESET PULSE WIDTH)
t_{PHL} (MASTER RESET TO OUTPUT)


$\overline{MR}$
1.5 V
t_{pw}
t_{PHL}
Q
1.5 V

Other Conditions: $\overline{S}$ & Ē = L

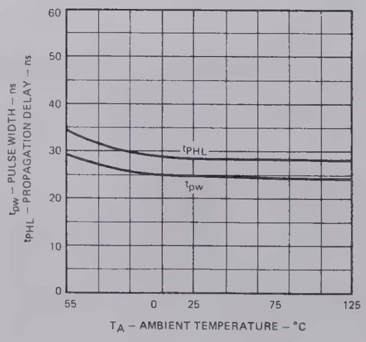
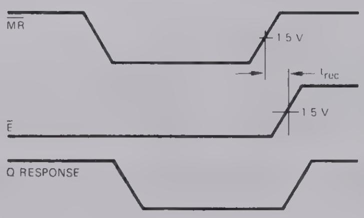


Fig. 5

t_{rec} (MASTER RESET RECOVERY TIME)


$\overline{MR}$
1.5 V
t_{ruc}
Ē
1.5 V
Q RESPONSE

Other Conditions: $\overline{S}$ = L, D = H

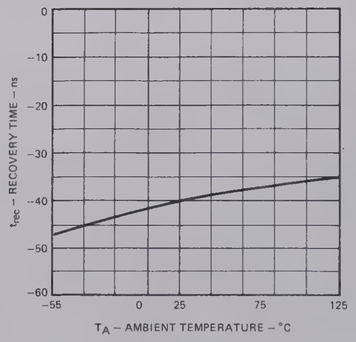
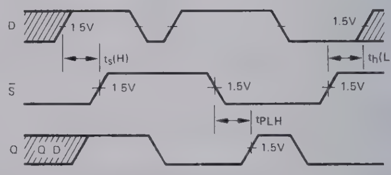


Fig. 6

SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO SET INPUT, AND SET TO OUTPUT DELAY.


D
1.5V
1.5V
$t_s(H)$
$t_h(L)$
$\overline{S}$
1.5V
1.5V
1.5V
t_{PLH}
Q
Q D
1.5V

OTHER CONDITIONS: $\overline{MR}$ = H, Ē = L

The shaded area indicates when the Data input is permitted to change for predictable output performance.

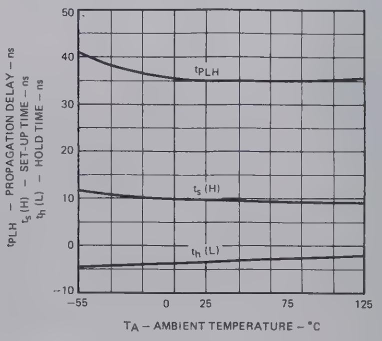


Fig. 7

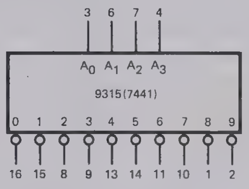
TTL/MSI 9315 (7441)

1-OF-10 DECODER/DRIVER

DESCRIPTION — The TTL/MSI 9315 accepts 1-2-4-8 binary coded decimal inputs and provides ten mutually exclusive outputs to directly control the ionizing potentials of many gas filled cold cathode indicator tubes. The 9315 is similar in operation to the CμL9960, but the 9315 can be driven from any TTL or DTL product.

- **STABLE HIGH VOLTAGE OUTPUT CHARACTERISTICS**
- **DIRECT DISPLAY DRIVE CAPABILITY**
- **BCD ACTIVE LEVEL HIGH INPUTS**
- **BLANKING TEST MODE**
- **–55°C TO +125°C TEMPERATURE CAPABILITY**

LOGIC SYMBOL


3 6 7 4
A_0 A_1 A_2 A_3
9315(7441)
0 1 2 3 4 5 6 7 8 9
16 15 8 9 13 14 11 10 1 2

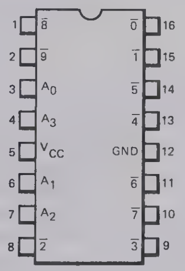
V_{CC} = PIN 5
GND = PIN 12

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

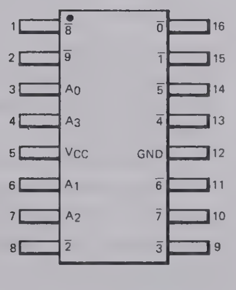
Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7 V
Input Voltage (dc) (See Note 1)	–1.5 V to +5.5 V
Input Current (dc) (See Note 1)	–10 mA to +1.0 mA
Current into output when output is LOW	10 mA
Current into each output when output is HIGH (See Note 2)	+1.5 mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
2: Total current through all 10 outputs in the HIGH state shall not exceed 2.0 mA.

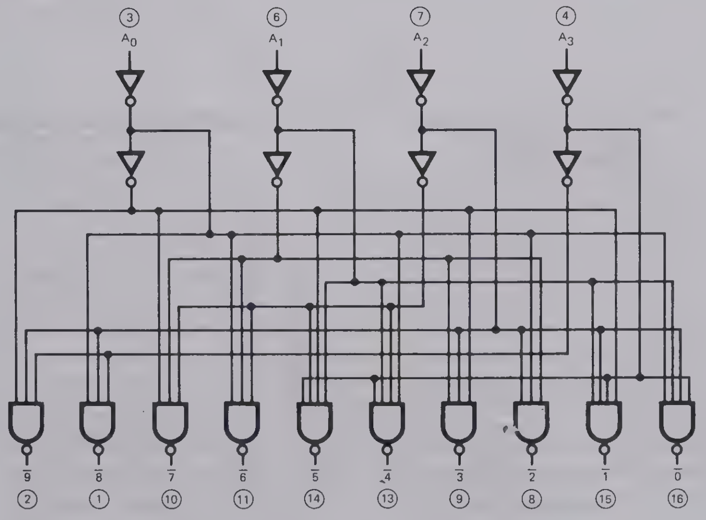
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 $\overline{8}$
2 $\overline{9}$
3 A_0
4 A_3
5 V_{CC}
6 A_1
7 A_2
8 $\overline{2}$
16 $\overline{0}$
15 $\overline{1}$
14 $\overline{5}$
13 $\overline{4}$
12 GND
11 $\overline{6}$
10 $\overline{7}$
9 $\overline{3}$

FLATPAK (TOP VIEW)


1 $\overline{8}$
2 $\overline{9}$
3 A_0
4 A_3
5 V_{CC}
6 A_1
7 A_2
8 $\overline{2}$
16 $\overline{0}$
15 $\overline{1}$
14 $\overline{5}$
13 $\overline{4}$
12 GND
11 $\overline{6}$
10 $\overline{7}$
9 $\overline{3}$

LOGIC DIAGRAM


③ A_0
⑥ A_1
⑦ A_2
④ A_3
$\overline{9}$ ②
$\overline{8}$ ①
$\overline{7}$ ⑩
$\overline{6}$ ⑪
$\overline{5}$ ⑭
$\overline{4}$ ⑬
$\overline{3}$ ⑨
$\overline{2}$ ⑧
$\overline{1}$ ⑮
$\overline{0}$ ⑯

○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The one-of-ten decoder/driver accepts BCD inputs from all TTL circuits and produces the correct output selection to directly drive gas filled cold cathode indicator tubes. The outputs are selected as shown in the Truth Table. It is capable of driving all known available cold cathode indicator tubes having 7 mA or less cathode current.

Unused input codes 12 and 13 cause all the outputs to remain HIGH, no cathode will be selected. This results in the indicator tube being blanked. Using this feature for blanking may cause a slight glow to appear in the tube.

TRUTH TABLE

	A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	H	L	L	L	H	L	H	H	H	H	H	H	H	H
2	L	H	L	L	H	H	L	H	H	H	H	H	H	H
3	H	H	L	L	H	H	H	L	H	H	H	H	H	H
4	L	L	H	L	H	H	H	H	L	H	H	H	H	H
5	H	L	H	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	H	H	H	L	H	H	H	H	H	H	H	L	H	H
8	L	L	L	H	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	L	H	L	H	H	H	L	H	H	H	H	H	L	H
11	H	H	L	H	H	H	H	L	H	H	H	H	H	L
12	L	L	H	H	H	H	H	H	H	H	H	H	H	H
13	H	L	H	H	H	H	H	H	H	H	H	H	H	H
14	L	H	H	H	H	H	H	H	H	H	L	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	L	H	H

H = HIGH voltage level
L = LOW voltage level

LOADING RULES

INPUTS	LOADING
All Inputs	1 U.L.

TTL INPUT LOAD

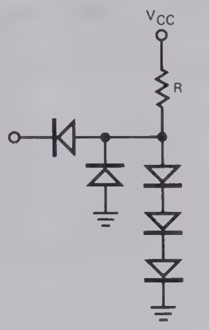
GRADE	INPUTS	LOADING
IND	All Inputs	1/9.4
MIL	All Inputs	2/9.4

OUTPUTS are designed to drive gas filled cold Cathode Indicator tubes

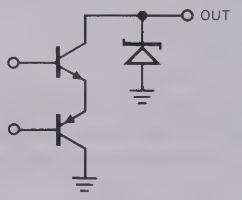
1 U.L. = 1 DTL Unit Load
1 U.L. is defined by the entries
I_{IH} and I_{IL} in the table on following page.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

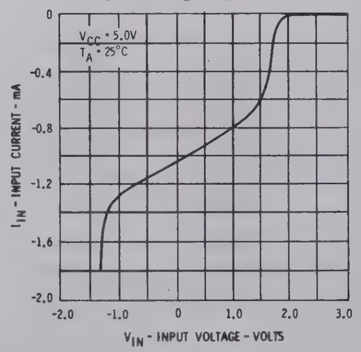
EQUIVALENT INPUT CIRCUIT



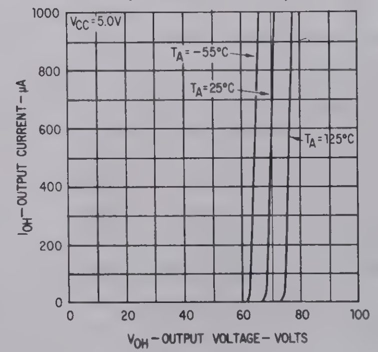
EQUIVALENT OUTPUT CIRCUIT



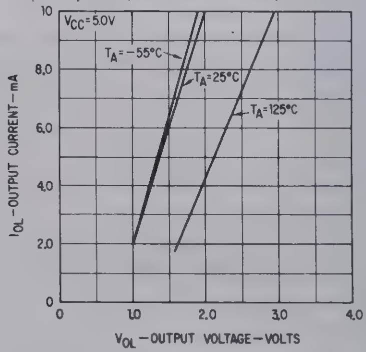
INPUT CURRENT VERSUS INPUT VOLTAGE A_0, A_1, A_2, A_3 INPUTS



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



ELECTRICAL CHARACTERISTICS (T_A = –55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part No. 9315XM, see note)

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS
		–55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	61		70	75		70		Volts	V_{CC} = 5.5 V, Force 2.0 mA into HIGH Output
I_{OH}	Output HIGH Leakage Current					20		50	μA	V_{CC} = 5.5 V, V_{OUT} = 55 V Inputs at Threshold Voltages (V_{IL} = Gnd, V_{IH} = 4.5 V) as per Truth Table
V_{OL}	Output LOW Voltage		3.0			2.5		3.7	Volts	V_{CC} = 4.5 V, I_{OL} = 7.0 mA Inputs at Threshold Voltages (V_{IL} or V_{IH}) as per Truth Table
V_{IH}	Input HIGH Voltage	2.1		1.9			1.7		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		1.4			1.1		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		–1.5		–1.3	–1.5		–1.5	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V Other Inputs Open
I_{IH}	Input HIGH Current				0.02	2.0		5.0	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V Other Inputs Open
I_{CC}	Supply Current		29			29		29	mA	V_{CC} = 5.0 V, No Connection to Input or Output Pins

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9315XC, see note)

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS
		0°C		+25°C			+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	67		70	75		70		Volts	V_{CC} = 5.25 V, Force 2.0 mA into HIGH Output
I_{OH}	Output HIGH Leakage Current					40		50	μA	V_{CC} = 5.25 V, V_{OUT} = 55 V Inputs at Threshold Voltages (V_{IL} = Gnd, V_{IH} = 4.5 V) as per Truth Table
V_{OL}	Output LOW Voltage		3.2			3.0		3.6	Volts	V_{CC} = 4.75 V, I_{OL} = 7.0 mA Inputs at Threshold Voltages (V_{IL} or V_{IH}) as per Truth Table
V_{IH}	Input HIGH Voltage	2.0		2.0			2.0		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		–1.5			–1.5		–1.5	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V Other Inputs Open
I_{IH}	Input HIGH Current					5.0		10	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V Other Inputs Open
I_{CC}	Supply Current		31			31		31	mA	V_{CC} = 5.0 V, No Connection to Input or Output Pins

NOTE:
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

TTL/MSI 9317B • 9317C

SEVEN SEGMENT DECODER/DRIVER

DESCRIPTION — The 9317 is a TTL/MSI Seven Segment Decoder/Driver designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used to directly drive seven segment incandescent lamp displays and light emitting diode indicators (or indirectly drive neon, electro-luminescent, numeric displays). The 9317 is compatible with all members of the Fairchild TTL family.

The 9317 is available in two output current and latch voltage versions, the 9317B and C.

- **TTL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE LOW OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE**
- **DRIVE LAMPS DIRECTLY**
- **CODES IN EXCESS OF BINARY 9 DISABLE OUTPUTS**
- **ENHANCED RELIABILITY WITH UNIQUE NUMERIC ONE DISPLAY POSITION**

PIN NAMES

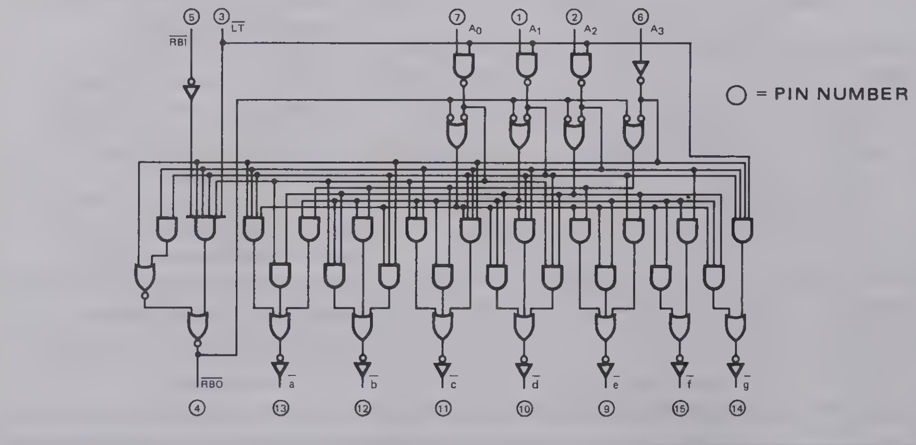
		LOADING	
		HIGH	LOW
A_0, A_1, A_2, A_3	Address Inputs	1.0 U.L.	1.0 U.L.
$\overline{LT}$	Lamp Test (Active LOW) Input	5.0 U.L.	4.0 U.L.
$\overline{RBI}$	Ripple Blanking (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{RBO}$	Ripple Blanking (Active LOW) Output	1.5 U.L.	1.5 U.L.
$\overline{a}$, $\overline{b}$, $\overline{c}$, $\overline{d}$, $\overline{e}$, $\overline{f}$, $\overline{g}$	(Active LOW) Outputs	See Options	

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

OPTIONS

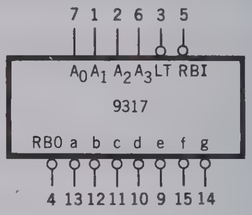
PARAMETER	9317B	9317C
Latch Voltage Output Current (Pins 9 through 15)	20 Volts 40 mA	30 Volts 20 mA

LOGIC DIAGRAM



5
RBI
3
LT
7
A0
1
A1
2
A2
6
A3
○ = PIN NUMBER
RBO
a
b
c
d
e
f
g
4
13
12
11
10
9
15
14

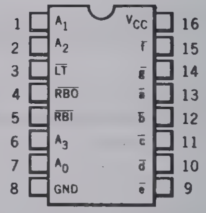
LOGIC SYMBOL



7 1 2 6 3 5
A0 A1 A2 A3 LT RBI
9317
RBO a b c d e f g
4 13 12 11 10 9 15 14

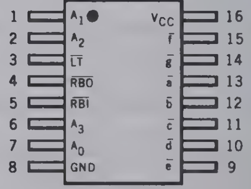
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1
2
3
4
5
6
7
8
A1
A2
LT
RBO
RBI
A3
A0
GND
VCC
f
g
a
b
c
d
e
16
15
14
13
12
11
10
9

FLATPAK (TOP VIEW)



1
2
3
4
5
6
7
8
A1
A2
LT
RBO
RBI
A3
A0
GND
VCC
f
g
a
b
c
d
e
16
15
14
13
12
11
10
9

FUNCTIONAL DESCRIPTION – The 9317 seven segment decoder/driver accepts a 4-bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0–9. The seven outputs ($\overline{a}$,$\overline{b}$,$\overline{c}$,$\overline{d}$, $\overline{e}$,$\overline{f}$,$\overline{g}$,) of the decoder select the corresponding segments in the matrix shown in Figure 1. The numeric designations chosen to represent the decimal numbers are shown in Figure 3. Code configurations in excess of binary nine disable the outputs.

The decoder has active LOW outputs so that it may be used directly to drive incandescent displays or light emitting diode indicators.

The device has provision for automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed interger fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeros.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and allows checking on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

TRUTH TABLE

$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	DECIMAL OR FUNCTION
L	X	X	X	X	X	L	L	L	L	L	L	L	H	
H	L	L	L	L	L	H	H	H	H	H	H	H	L	0
H	H	L	L	L	L	L	L	L	L	L	L	H	H	0
	X	H	L	L	L	H	H	H	H	L	L	H	H	1
		L	H	L	L	L	L	H	L	L	H	L	H	2
		H	H	L	L	L	L	L	L	H	H	L	H	3
		L	L	H	L	H	L	L	H	H	L	L	H	4
		H	L	H	L	L	H	L	L	H	L	L	H	5
		L	H	H	L	H	H	L	L	L	L	L	H	6
		H	H	H	L	L	L	L	H	H	H	H	H	7
		L	L	L	H	L	L	L	L	L	L	L	H	8
		H	L	L	H	L	L	L	H	H	L	L	H	9
		L	H	L	H	H	H	H	H	H	H	H	L	10
		H	H	L	H	H	H	H	H	H	H	H	L	11
		L	L	H	H	H	H	H	H	H	H	H	L	12
		H	L	H	H	H	H	H	H	H	H	H	L	13
		L	H	H	H	H	H	H	H	H	H	H	L	14
H	X	H	H	H	H	H	H	H	H	H	H	H	L	15

H – HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care Condition

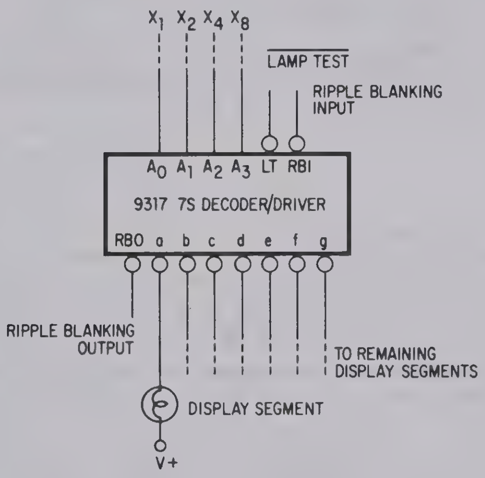


Fig. 2
SEVEN SEGMENT DECODER DRIVING INCANDESCENT LAMP DISPLAY

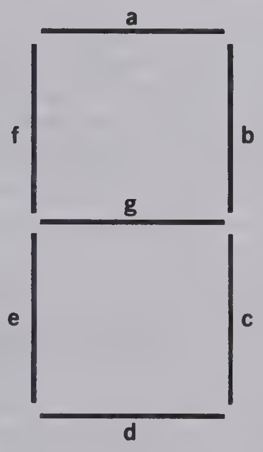


Fig. 1
SEGMENT DESIGNATION

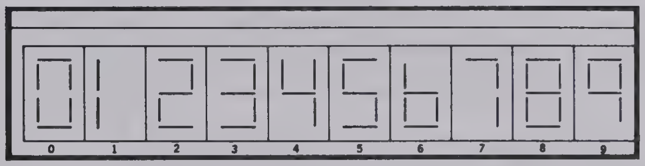


Fig. 3
NUMERICAL DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature		–65°C to +150°C
Temperature (Ambient) Under Bias		–55°C to +125°C
V_{CC} Pin Potential to Ground Pin		–0.5 V to +7.0 V
Voltage Applied to Outputs for HIGH Output State		–0.5 V to +30 V
Input Voltage (dc)		–0.5 V to +5.5 V
Current Into Outputs		80 mA
Power Dissipation per Output	9317B	50 mW
	9317C	30 mW

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part No. 9317BXM • 9317CXM)*

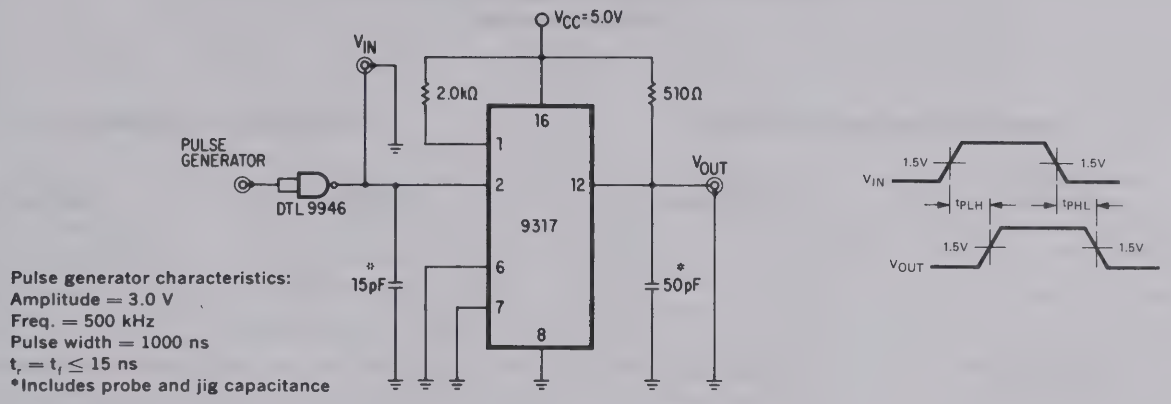
SYMBOL	PARAMETER		LIMITS							UNITS	CONDITIONS	
			−55°C		+25°C			+125°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OH}	Output HIGH Voltage on $\overline{RBO}$ Only		3.0		3.0	4.0		3.0		Volts	V_{CC} = 4.5 V, I_{OH} = −70 μA Pin 5 = V_{IH}, Pins 1, 2, 6, 7 = 0 V	
I_{CEX}	Output HIGH Leakage Current					100	200		250	μA	V_{CC} = 5.5 V, V_{CEX} = 30 V (CXM), 20 V (BXM) Inputs at V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage on $\overline{RBO}$ Only			0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 3.1 mA	Inputs at V_{IH} or V_{IL} per Truth Table
				0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 2.4 mA	
V_{OL}	Output LOW Voltage	9317BXM		0.8		0.50	0.8		0.8	Volts	V_{CC} = 4.5 V, I_{OL} = 40 mA Pin 3 = 0 V	
		9317CXM		0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 20 mA Pin 3 = 0 V	
V_{LATCH}	Output Latch Voltage	9317BXM	20		20			20		Volts	V_{CC} = 5.0 V, I_{OUT} = 10 mA	
		9317CXM	30		30			30		Volts	Inputs = Open	
V_{IH}	Input HIGH Voltage		2.1		1.9			1.7		Volts	Guaranteed Input HIGH Threshold for All Inputs	
V_{IL}	Input LOW Voltage			1.4			1.1		0.8	Volts	Guaranteed Input LOW Threshold for All Inputs	
I_{IL}	Input LOW Current											
	$\overline{LT}$			−6.4			−6.4		−6.4	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V	
	A_0, A_1, A_2, A_3			−1.5			−1.5		−1.5	mA	V_{IN} = 5.5 V on Other Inputs	
	$\overline{RBI}$			−0.75			−0.75		−0.75	mA		
I_{IH}	Input HIGH Current											
	$\overline{LT}$						200		200	μA	V_{CC} = 5.5 V, V_{IN} = 2.4 V	
	$\overline{RBI}$, A_0, A_1, A_2, A_3						40		40	μA	GND on Other Inputs	
t_{PLH}	Turn Off Delay						500			ns	V_{CC} = 5.0 V, See Figure 4	
t_{PHL}	Turn On Delay						500			ns		

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9317BXC • 9317CXC)*

SYMBOL	PARAMETER		LIMITS							UNITS	CONDITIONS	
			0°C		+25°C			+75°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OH}	Output HIGH Voltage on $\overline{RBO}$ Only		3.0		3.0	4.0		3.0		Volts	V_{CC} = 4.75 V, I_{OH} = −70 μA Pin 5 = V_{IH}, Pins 1, 2, 6, 7 = 0 V	
I_{CEX}	Output HIGH Leakage Current					100	200		250	μA	V_{CC} = 5.25 V, V_{CEX} = 30 V (CXC), 20 V (BXC) Inputs at V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage on $\overline{RBO}$ Only			0.45		0.25	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 2.75 mA	Inputs at V_{IH} or V_{IL} per Truth Table
				0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 2.4 mA	
V_{OL}	Output LOW Voltage	9317BXC		0.9		0.65	0.9		0.9	Volts	V_{CC} = 4.75 V, I_{OL} = 40 mA Pin 3 = 0 V	
		9317CXC		0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 20 mA Pin 3 = 0 V	
V_{LATCH}	Output Latch Voltage	9317BXC	20		20			20		Volts	V_{CC} = 5.0 V, I_{OUT} = 10 mA	
		9317CXC	30		30			30		Volts	Inputs = Open	
V_{IH}	Input HIGH Voltage		2.0		2.0			2.0		Volts	Guaranteed Input HIGH Threshold for All Inputs	
V_{IL}	Input LOW Voltage			0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold for All Inputs	
I_{IL}	Input LOW Current											
	$\overline{LT}$			−6.4			−6.4		−6.4	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V	
	A_0, A_1, A_2, A_3			−1.5			−1.5		−1.5	mA	V_{IN} = 5.25 V on Other Inputs	
	$\overline{RBI}$			−0.75			−0.75		−0.75	mA		
I_{IH}	Input HIGH Current											
	$\overline{LT}$						200		200	μA	V_{CC} = 5.25 V, V_{IN} = 2.4 V	
	$\overline{RBI}$, A_0, A_1, A_2, A_3						40		40	μA	GND on Other Inputs	
t_{PLH}	Turn Off Delay						500			ns	V_{CC} = 5.0 V, See Figure 4	
t_{PHL}	Turn On Delay						500			ns		

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

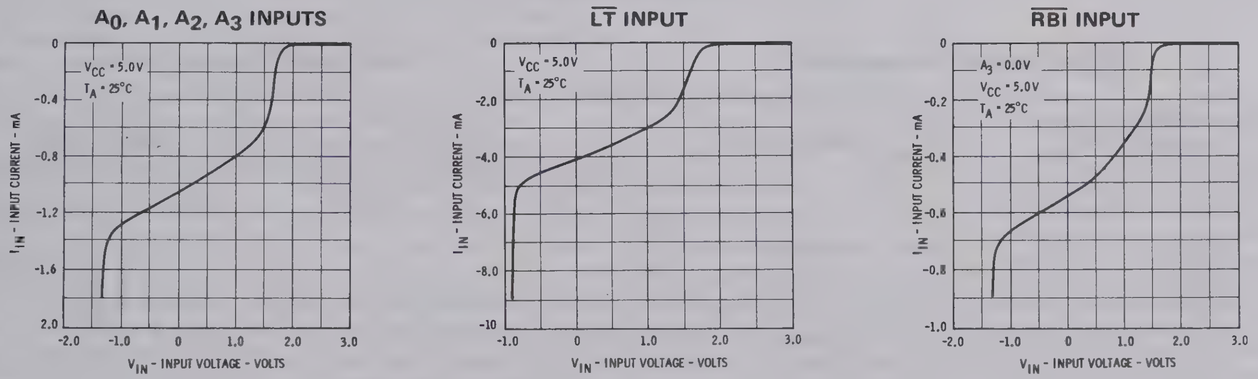
Fig. 4 – SWITCHING CIRCUIT AND WAVEFORMS


VCC = 5.0V
VIN
2.0kΩ
510Ω
16
1
PULSE GENERATOR
DTL 9946
2
12
VOUT
9317
* 15pF
6
7
8
* 50pF
1.5V
VIN
1.5V
tPLH
tPHL
1.5V
VOUT
1.5V

Pulse generator characteristics:
Amplitude = 3.0 V
Freq. = 500 kHz
Pulse width = 1000 ns
$t_r = t_f \leq 15$ ns
*Includes probe and jig capacitance

TYPICAL INPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE

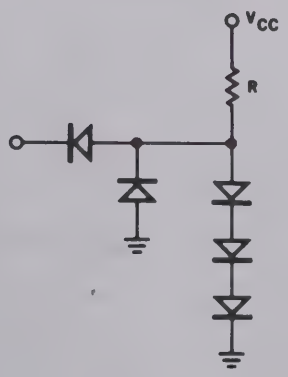

A_0, A_1, A_2, A_3 INPUTS

$\overline{LT}$ INPUT

$\overline{RBI}$ INPUT

INPUTS

EQUIVALENT CIRCUIT

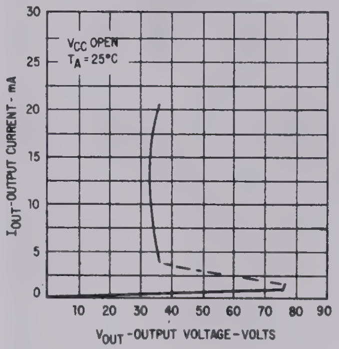


OUTPUT CHARACTERISTICS

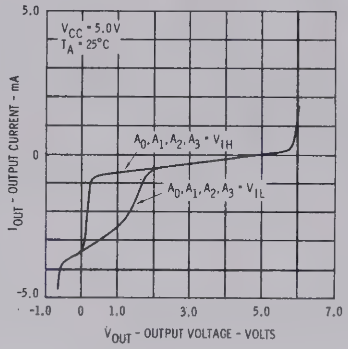
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE
9317BXM, 9317BXC

TYPICAL OUTPUT IN HIGH STATE

$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$ OUTPUTS

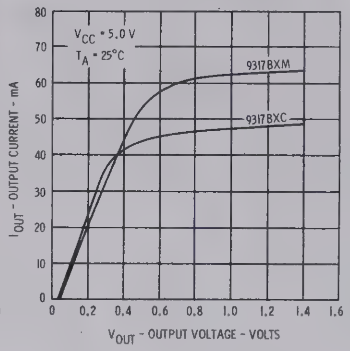


$\overline{\text{RBO}}$ OUTPUT

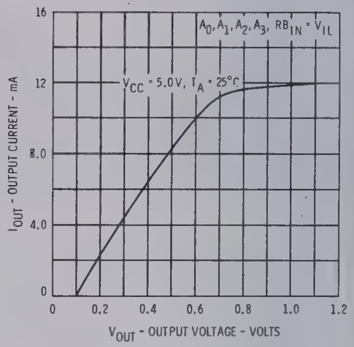


TYPICAL OUTPUT IN LOW STATE

$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$ OUTPUTS



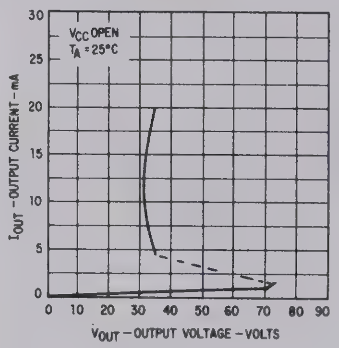
$\overline{\text{RBO}}$ OUTPUT



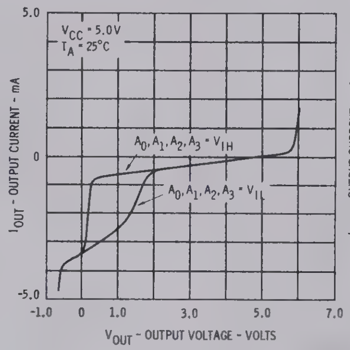
9317CXM, 9317CXC

TYPICAL OUTPUT IN HIGH STATE

$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$ OUTPUTS

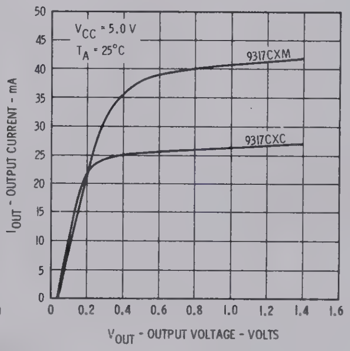


$\overline{\text{RBO}}$ OUTPUT

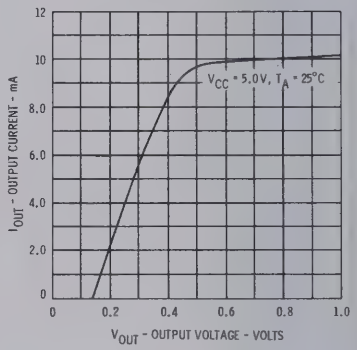


TYPICAL OUTPUT IN LOW STATE

$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$ OUTPUTS

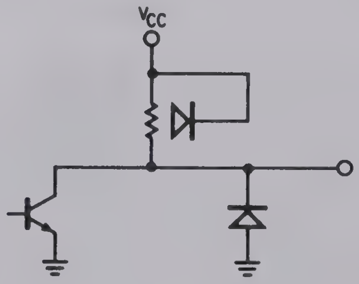


$\overline{\text{RBO}}$ OUTPUT

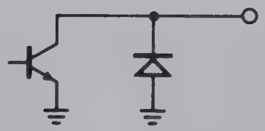


OUTPUTS

EQUIVALENT CIRCUIT (PIN 4)



EQUIVALENT CIRCUIT
(Pins 9 thru 15)



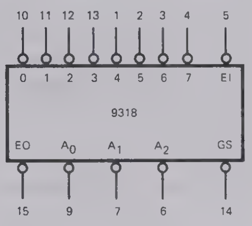
TTL/MSI 9318

EIGHT-INPUT PRIORITY ENCODER

DESCRIPTION — The TTL/MSI 9318 is a Multipurpose Encoder designed to accept eight inputs and produce a binary weighted code of the highest order input. The circuit uses TTL for high speed and high fanout capability, and is compatible with all members of the Fairchild TTL family.

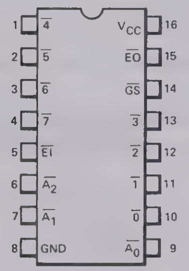
- **MULTI-FUNCTION CAPABILITY**
  - **CODE CONVERSIONS**
  - **MULTI-CHANNEL D/A CONVERTER**
  - **DECIMAL TO BCD CONVERTER**
  - **CASCADING FOR PRIORITY ENCODING OF N BITS**
- **INPUT ENABLE CAPABILITY**
- **PRIORITY ENCODING — AUTOMATIC SELECTION OF HIGHEST PRIORITY INPUT LINE**
- **OUTPUT ENABLE — ACTIVE LOW WHEN ALL INPUTS HIGH**
- **GROUP SIGNAL OUTPUT — ACTIVE WHEN ANY INPUT IS LOW**
- **TYPICAL POWER DISSIPATION OF 250 mW**
- **INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**
- **ALL CERAMIC HERMETIC 16-LEAD DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL

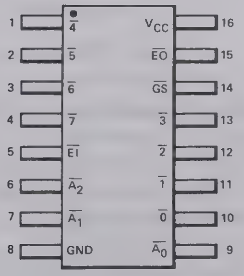

10
11
12
13
1
2
3
4
5
0
1
2
3
4
5
6
7
EI
9318
EO
A0
A1
A2
GS
15
9
7
6
14

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 4
2 5
3 6
4 7
5 EI
6 A2
7 A1
8 GND
16 VCC
15 EO
14 GS
13 3
12 2
11 1
10 0
9 A0

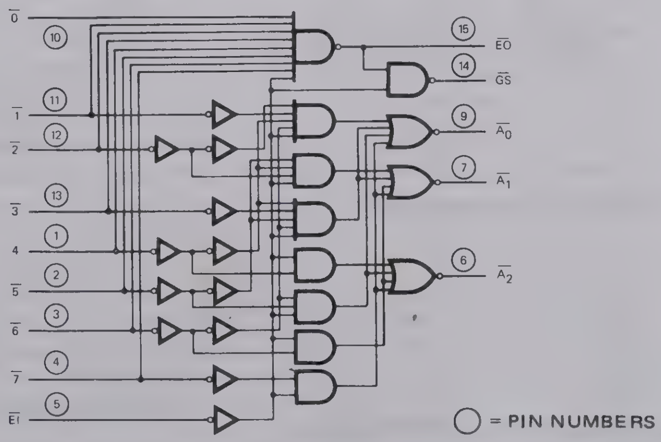
FLATPAK (TOP VIEW)


1 4
2 5
3 6
4 7
5 EI
6 A2
7 A1
8 GND
16 VCC
15 EO
14 GS
13 3
12 2
11 1
10 0
9 A0

PIN NAMES		**LOADING** (Note a)
$\overline{0}$	Priority (Active LOW) Input	1 U.L.
$\overline{1}$ to $\overline{7}$	Priority (Active LOW) Inputs	2 U.L.
$\overline{EI}$	Enable (Active LOW) Input	2 U.L.
$\overline{EO}$	Enable (Active LOW) Output	10 U.L.*
$\overline{GS}$	Group Select (Active LOW) Output	10 U.L.*
$\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$	Address (Active LOW) Outputs	10 U.L.*

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM


0
10
1
11
2
12
3
13
4
1
5
2
6
3
7
4
EI
5
15
EO
14
GS
9
A0
7
A1
6
A2
○ = PIN NUMBERS

FUNCTIONAL DESCRIPTION — The 9318 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority.

A HIGH on the Input Enable ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

A Group Signal output ($\overline{GS}$) and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active level LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active level LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are inactive HIGH when the input enable is HIGH.

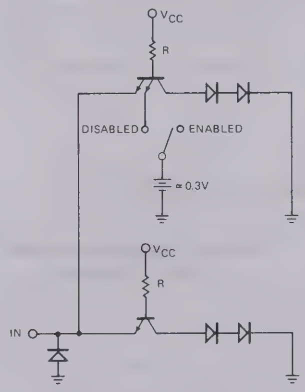
TABLE I — TRUTH TABLE

$\overline{EI}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{GS}$	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

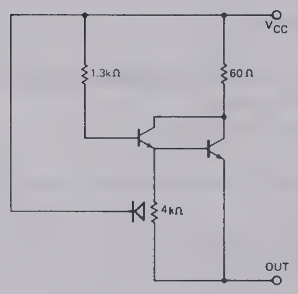
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

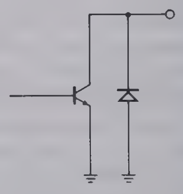
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

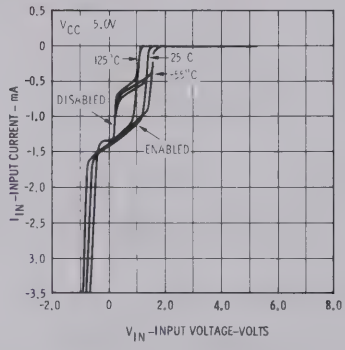


Fig. 1.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH STATE

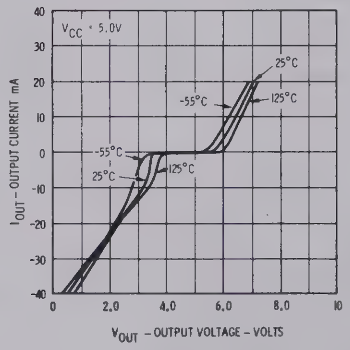


Fig. 2.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW STATE

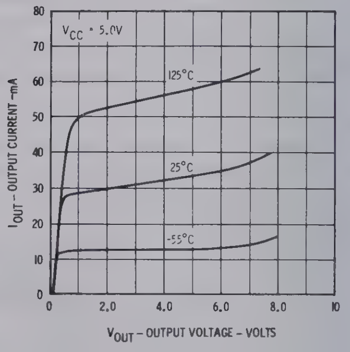


Fig. 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	SUPPLY VOLTAGE (V_{CC}) TYP.	SUPPLY VOLTAGE (V_{CC}) MAX.	TEMPERATURE
9318XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9318XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., $I_{IN} = -12$mA, $T_A = 25°C$
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., $I_{OH} = -800\ \mu A$ $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{I_0}$ (Pin 10) $\overline{EI}$, $\overline{I_1}-\overline{I_7}$		 10 20	 40 80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current $\overline{I_0}$ (Pin 10) $\overline{EI}$, $\overline{I_1}-\overline{I_7}$		 −0.96 −1.92	 −1.6 −3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−30	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		50	77	mA	V_{CC} = MAX.

NOTES:

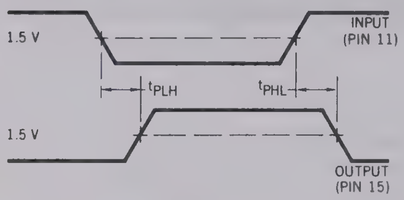
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	9318XM(MIL) MIN.	9318XM(MIL) MAX.	9318XC(IND) MIN.	9318XC(IND) MAX.	UNITS	CONDITIONS	
t_{PLH} t_{PHL}	Data Input to Enable Output		10 30		15 40	ns ns	See Figure 4	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Enable Input to Group Signal		16 25		20 31	ns ns	See Figure 5	
t_{PLH} t_{PHL}	Enable Input to Enable Output		15 40		21 45	ns ns	See Figure 6	
t_{PLH} t_{PHL}	Enable Input to Data Output		20 25		25 30	ns ns	See Figure 7	
t_{PLH} t_{PHL}	Data Input to Group Signal		40 25		45 30	ns ns	See Figure 8	
t_{PLH} t_{PHL}	Data Input to Data Output		30 30		38 38	ns ns	See Figure 9	

SWITCHING CHARACTERISTICS

DATA INPUT TO ENABLE OUTPUT


1.5 V
INPUT (PIN 11)
tPLH
tPHL
1.5 V
OUTPUT (PIN 15)

Other Conditions: Pin 5 = GND
Pins 1, 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

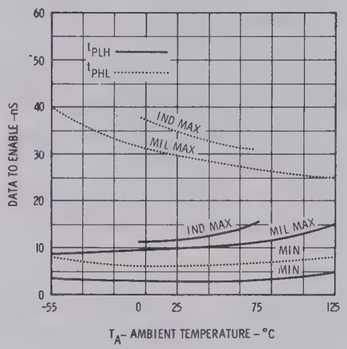
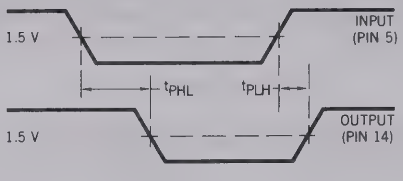


Fig. 4.

ENABLE INPUT TO GROUP SIGNAL


1.5 V
INPUT (PIN 5)
tPHL
tPLH
1.5 V
OUTPUT (PIN 14)

Other Conditions: Pin 10 - GND
Pins 1, 2, 3, 4, 11, 12, 13 =
V_{CC} through 750 Ω

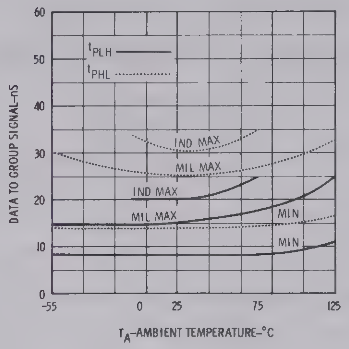
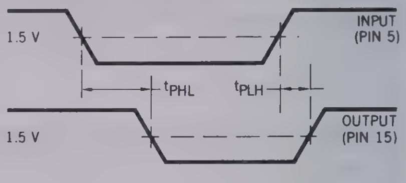


Fig. 5.

ENABLE INPUT TO ENABLE OUTPUT


1.5 V
INPUT (PIN 5)
tPHL
tPLH
1.5 V
OUTPUT (PIN 15)

Other Conditions:
Pins 1, 2, 3, 4, 10, 11, 12, 13 =
V_{CC} through 750 Ω

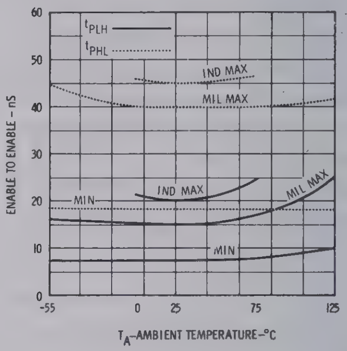
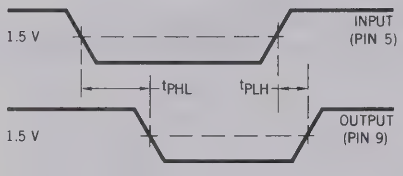


Fig. 6.

ENABLE INPUT TO DATA OUTPUT


1.5 V
INPUT (PIN 5)
tPHL
tPLH
1.5 V
OUTPUT (PIN 9)

Other Conditions: Pin 4 = GND
Pins 1, 2, 3, 10, 11, 12, 13 =
V_{CC} through 750 Ω

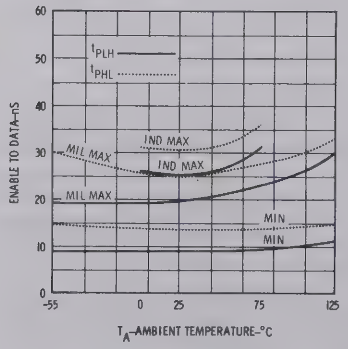
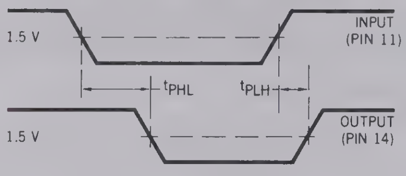


Fig. 7.

DATA INPUT TO GROUP SIGNAL


1.5 V
INPUT (PIN 11)
tPHL
tPLH
1.5 V
OUTPUT (PIN 14)

Other Conditions: Pin 5 = GND
Pins 1, 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

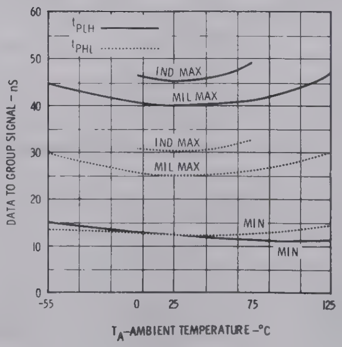
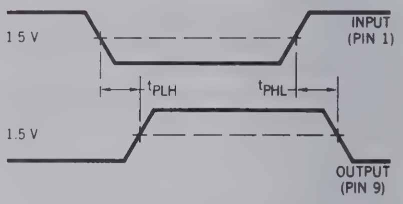


Fig. 8.

DATA INPUT TO DATA OUTPUT


1.5 V
INPUT (PIN 1)
tPLH
tPHL
1.5 V
OUTPUT (PIN 9)

Other Conditions: Pins 5, 11 = GND
Pins 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

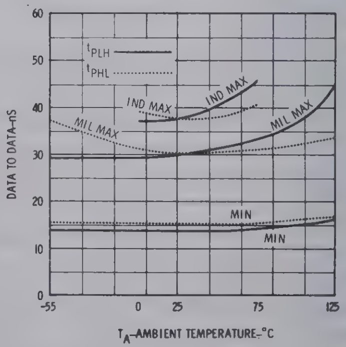


Fig. 9.

LPTTL/MSI 93L18

LOW POWER EIGHT-INPUT PRIORITY ENCODER

DESCRIPTION — The LPTTL/MSI 93L18 is a Multipurpose Encoder designed to accept eight inputs and produce a binary weighted code of the highest order input. The circuit uses TTL technology for high speed and high fanout capability, and is compatible with all Fairchild TTL families.

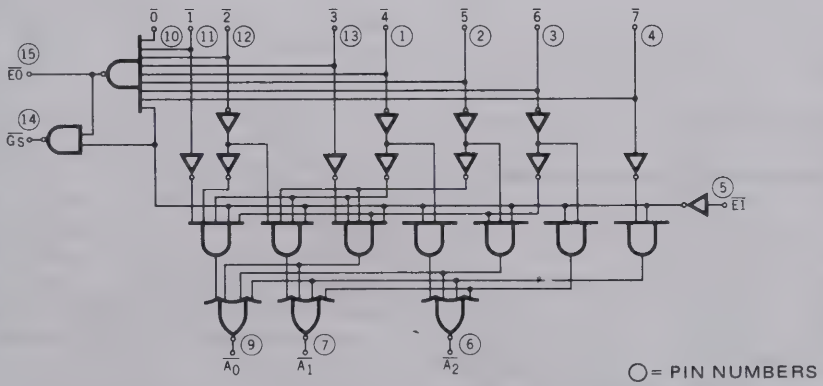
- MULTI-FUNCTION CAPABILITY
  - CODE CONVERSIONS
  - MULTI-CHANNEL D/A CONVERTER
  - DECIMAL TO BCD CONVERTER
  - CASCADING FOR PRIORITY ENCODING OF N BITS
- INPUT ENABLE CAPABILITY
- PRIORITY ENCODING — AUTOMATIC SELECTION OF HIGHEST PRIORITY INPUT LINE
- OUTPUT ENABLE — ACTIVE LOW WHEN ALL INPUTS HIGH
- GROUP SIGNAL OUTPUT — ACTIVE WHEN ANY INPUT IS LOW
- TYPICAL PROPAGATION DELAY OF 55 ns
- TYPICAL POWER DISSIPATION OF 75 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC HERMETIC 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

PIN NAMES

		LOADING	
		HIGH	LOW
$\overline{0}$	Priority (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{1}$ to $\overline{7}$	Priority (Active LOW) Inputs	1.0 U.L.	0.5 U.L.
$\overline{EI}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{EO}$	Enable (Active LOW) Output	10 U.L.	1.25 U.L.
$\overline{GS}$	Group Select (Active LOW) Output	10 U.L.	1.5 U.L.
$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$	Address (Active LOW) Outputs	10 U.L.	2.5 U.L.

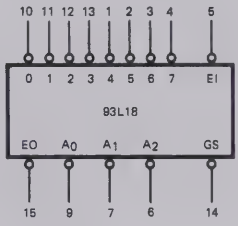
1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW

LOGIC DIAGRAM



0̄ 10
1̄ 11
2̄ 12
3̄ 13
4̄ 1
5̄ 2
6̄ 3
7̄ 4
15 E̅O̅
14 G̅S̅
5 E̅I̅
9 A̅0
7 A̅1
6 A̅2
○= PIN NUMBERS

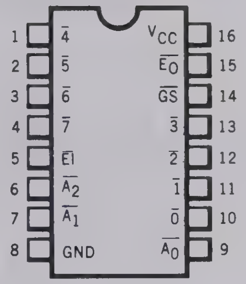
LOGIC SYMBOL



10 11 12 13 1 2 3 4 5
0 1 2 3 4 5 6 7 EI
93L18
EO A0 A1 A2 GS
15 9 7 6 14

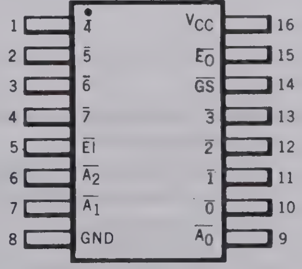
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 4̄
2 5̄
3 6̄
4 7̄
5 E̅I̅
6 A̅2
7 A̅1
8 GND
16 VCC
15 E̅O̅
14 G̅S̅
13 3̄
12 2̄
11 1̄
10 0̄
9 A̅0

FLATPAK (TOP VIEW)



1 4̄
2 5̄
3 6̄
4 7̄
5 E̅I̅
6 A̅2
7 A̅1
8 GND
16 VCC
15 E̅O̅
14 G̅S̅
13 3̄
12 2̄
11 1̄
10 0̄
9 A̅0

FUNCTIONAL DESCRIPTION – The LPTTL/MSI 93L18 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority.

A HIGH on the input enable ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

Provided with the three data outputs are a group signal output ($\overline{GS}$) and an enable output ($\overline{EO}$). The $\overline{GS}$ is active level LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active level LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are inactive when the input enable is HIGH.

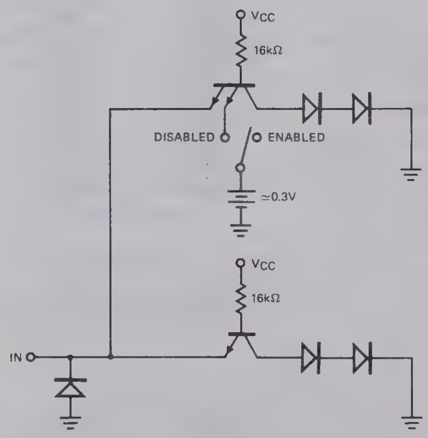
TRUTH TABLE

$\overline{EI}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TYPICAL INPUT AND OUTPUT CIRCUITS

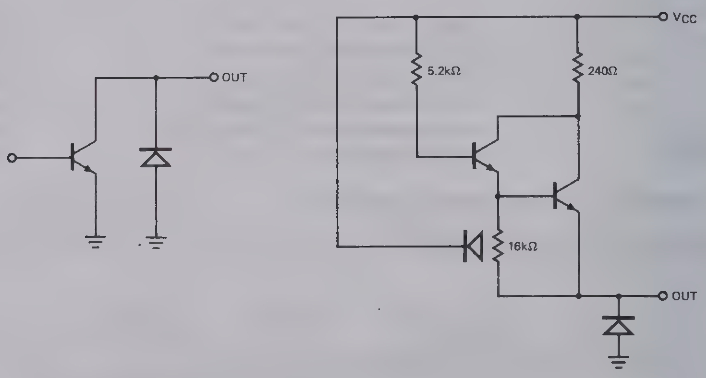
INPUTS
EQUIVALENT CIRCUIT



OUTPUTS
EQUIVALENT CIRCUIT

OUTPUT LOW

OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L18XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L18XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pins 6, 7, 9) I_{OL} = 2.4 mA (Pin 14) I_{OL} = 2.0 mA (Pin 15) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.3 V
	Input $\overline{0}$ (Pin 10)		−0.25	−0.4		
	Inputs $\overline{1}$ thru $\overline{7}$ & $\overline{EI}$		−0.50	−0.8		
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input $\overline{0}$ (Pin 10)		2.0	20		
	Inputs $\overline{1}$ thru $\overline{7}$ & $\overline{EI}$		4.0	40		
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		15	22	mA	V_{CC} = MAX., Pins 4 & 5 at GND

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

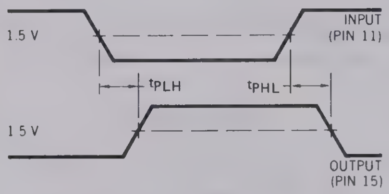
SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, Pin 8 = GND)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Data Input to Enable Output		10	15	ns	See Figure 1
t_{PHL}	Data Input to Enable Output		68	100		
t_{PLH}	Enable Input to Group Signal		16	27	ns	See Figure 2
t_{PHL}	Enable Input to Group Signal		38	57		
t_{PLH}	Enable Input to Enable Output		16	27	ns	See Figure 3
t_{PHL}	Enable Input to Enable Output		68	100		
t_{PLH}	Enable Input to Data Output		23	35	ns	See Figure 4
t_{PHL}	Enable Input to Data Output		38	57		
t_{PLH}	Data Input to Group Signal		59	89	ns	See Figure 5
t_{PHL}	Data Input to Group Signal		38	57		
t_{PLH}	Data Input to Data Output		33	50	ns	See Figure 6
t_{PHL}	Data Input to Data Output		51	77		

TYPICAL SWITCHING CHARACTERISTICS

All measurements are made with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. The active input is driven by a 9002 TTL gate. The input and output pins under test are loaded with 15 pF of capacitance. (This includes probe & jig capacitance.)

Fig. 1. Data Input to Enable Output


1.5 V
INPUT (PIN 11)
tPLH
tPHL
1.5 V
OUTPUT (PIN 15)

Other Conditions: Pin 5 = GND
Pins 1, 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

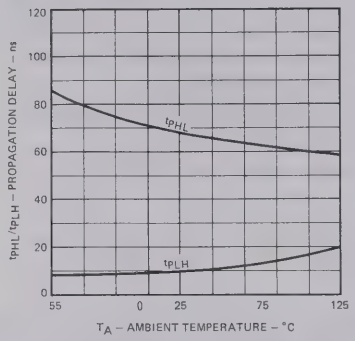
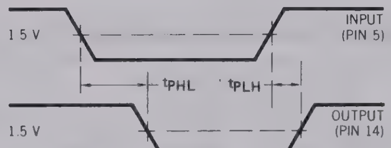


Fig. 2. Enable Input to Group Signal


1.5 V
INPUT (PIN 5)
tPHL
tPLH
1.5 V
OUTPUT (PIN 14)

Other Conditions: Pin 10 = GND
Pins 1, 2, 3, 4, 11, 12, 13 =
V_{CC} through 750 Ω

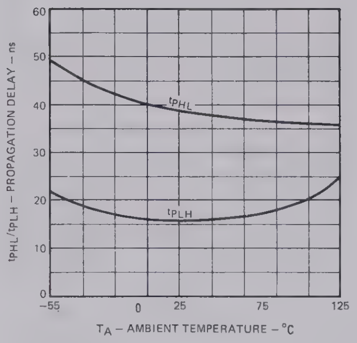
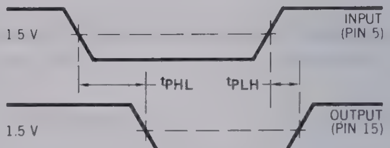


Fig. 3. Enable Input to Enable Output


1.5 V
INPUT (PIN 5)
tPHL
tPLH
1.5 V
OUTPUT (PIN 15)

Other Conditions:
Pins 1, 2, 3, 4, 10, 11, 12, 13 =
V_{CC} through 750 Ω

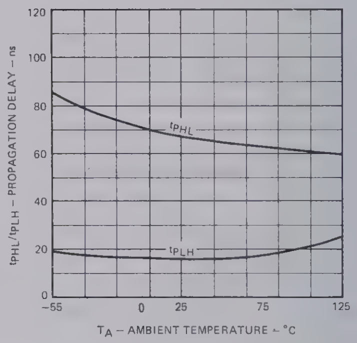
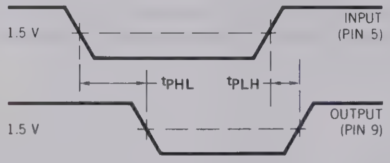


Fig. 4. Enable Input to Data Output


1.5 V
INPUT (PIN 5)
tPHL
tPLH
1.5 V
OUTPUT (PIN 9)

Other Conditions: Pin 4 = GND
Pins 1, 2, 3, 10, 11, 12, 13 =
V_{CC} through 750 Ω

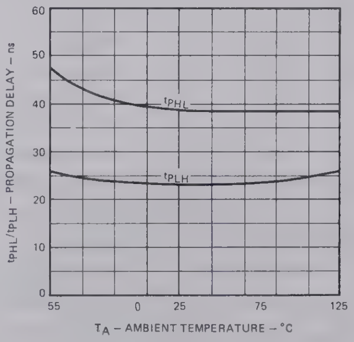
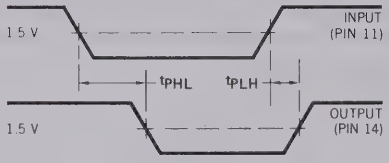


Fig. 5. Data Input to Group Signal


1.5 V
INPUT (PIN 11)
tPHL
tPLH
1.5 V
OUTPUT (PIN 14)

Other Conditions: Pin 5 = GND
Pins 1, 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

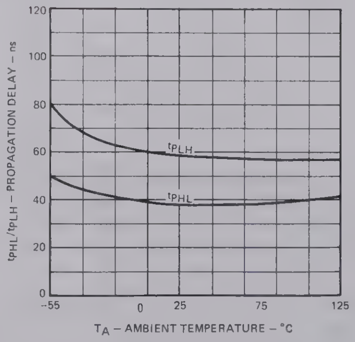
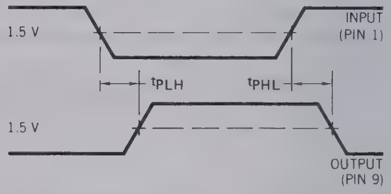
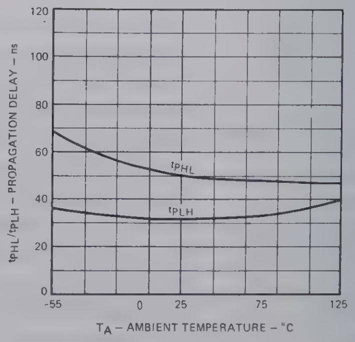


Fig. 6. Data Input to Data Output


1.5 V
INPUT (PIN 1)
tPLH
tPHL
1.5 V
OUTPUT (PIN 9)

Other Conditions: Pins 5, 11 = GND
Pins 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω



TTL/MSI 9321

DUAL ONE-OF-FOUR DECODER

DESCRIPTION — The TTL/MSI 9321 consists of two Independent Multipurpose Decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition, an active LOW enable input is provided for each decoder which gives demultiplexing capability. The circuit uses TTL for high speed and high fanout capability, and is compatible with all members of the Fairchild TTL family.

- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **GUARANTEED FANOUT OF 10 TTL LOADS OVER THE FULL TEMPERATURE RANGE AND SUPPLY VOLTAGE RANGES**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 150 mW**
- **THE INPUT / OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD MSI, DTL, LPDTL AND TTL FAMILIES**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**
- **ACTIVE LOW ENABLE FOR EACH DECODER**

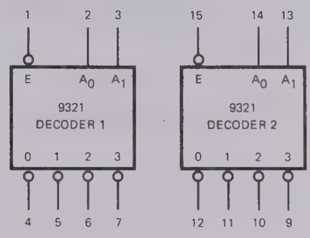
PIN NAMES		**LOADING** (Note a)
Decoder 1 and 2		
$\overline{E}$	Enable (Active LOW) Input	1 U.L.
A_0, A_1	Address Inputs	1 U.L.
$\overline{0}, \overline{1}, \overline{2}, \overline{3}$	(Active LOW) Outputs (Note b)	10 U.L.

Notes:

a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

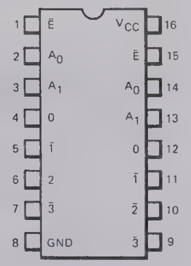
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC SYMBOL

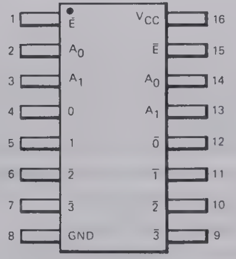

1
2
3
15
14
13
E
A_0
A_1
9321
DECODER 1
9321
DECODER 2
0
1
2
3
4
5
6
7
12
11
10
9

V_{CC} = Pin 16
GND = Pin 8

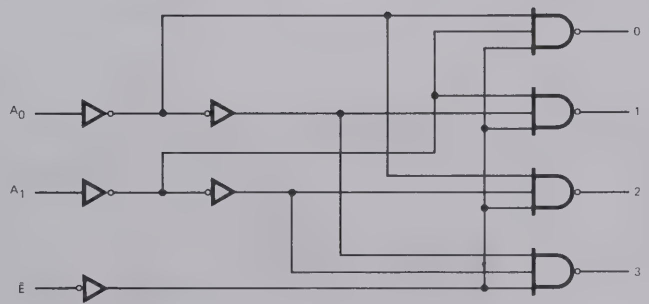
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 Ē
2 A_0
3 A_1
4 0
5 1̄
6 2
7 3̄
8 GND
V_{CC} 16
Ē 15
A_0 14
A_1 13
0 12
1̄ 11
2̄ 10
3̄ 9

FLATPAK (TOP VIEW)


1 Ē
2 A_0
3 A_1
4 0
5 1
6 2̄
7 3̄
8 GND
V_{CC} 16
Ē 15
A_0 14
A_1 13
0̄ 12
1̄ 11
2̄ 10
3̄ 9

LOGIC DIAGRAM



Note: Only one Decoder shown.

FUNCTIONAL DESCRIPTION – The 9321 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

The active LOW outputs facilitate memory addressing for units such as the 93402 associative memory. The active LOW outputs are also compatible with the active LOW enables of other MSI elements making the 9321 useful in logic selection schemes.

TRUTH TABLE
DECODER 1 & 2

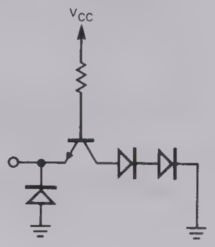
$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

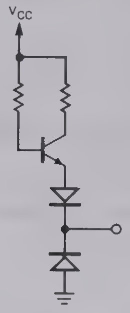
INPUTS

EQUIVALENT CIRCUIT

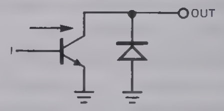


OUTPUTS

EQUIVALENT CIRCUIT OUTPUT HIGH



EQUIVALENT CIRCUIT OUTPUT LOW



INPUT CURRENT VERSUS INPUT VOLTAGE

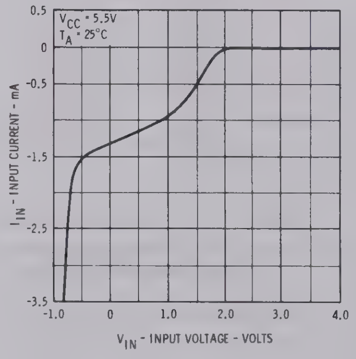


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH

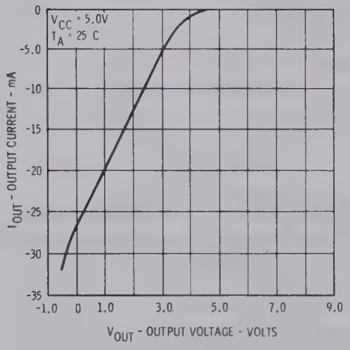


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

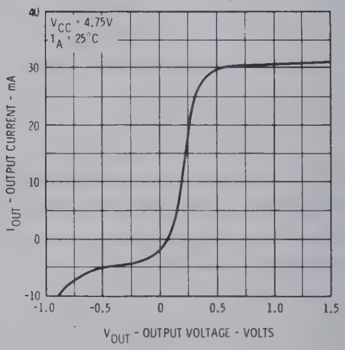


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9321XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9321XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA., T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−40	−70	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		30	50	mA	V_{CC} = MAX.

NOTES:

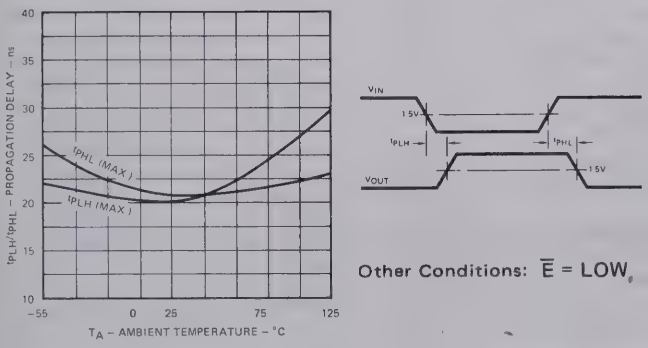
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay A Input to Output		13	20	ns	See Figure 4	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay A Input to Output		14	21	ns		
t_{PLH}	Turn Off Delay E Input to Output		9	14	ns	See Figure 5	
t_{PHL}	Turn On Delay E Input to Output		12	18	ns		

SWITCHING CHARACTERISTICS

ADDRESS INPUT TO OUTPUT



Other Conditions: $\overline{E}$ = LOW

Fig. 4.

ENABLE INPUT TO OUTPUT

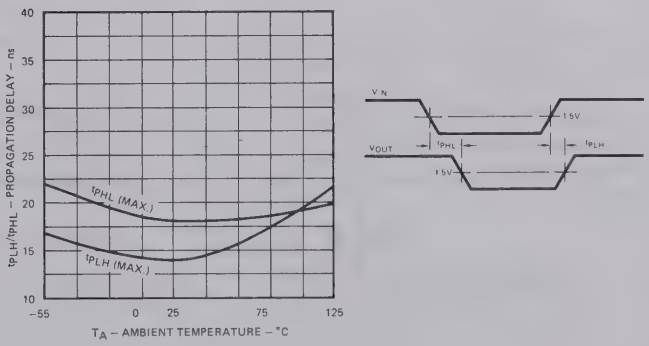


Fig. 5.

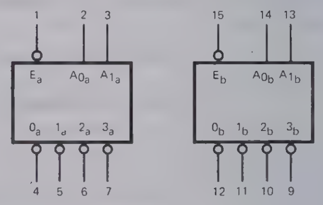
LPTTL/MSI 93L21

LOW POWER DUAL ONE-OF-FOUR DECODER

DESCRIPTION – The LPTTL/MSI 93L21 consists of two independent multipurpose decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition an active LOW enable input is provided for each decoder which gives demultiplexing capability. The circuit uses TTL technology and is compatible with the Fairchild TTL family.

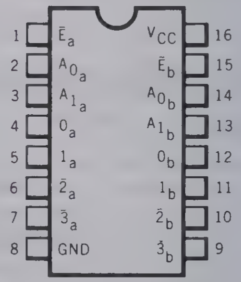
- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **ACTIVE LOW ENABLE FOR EACH DECODER**
- **TYPICAL PROPAGATION DELAY OF 50 ns**
- **TYPICAL POWER DISSIPATION OF 45 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

LOGIC SYMBOL

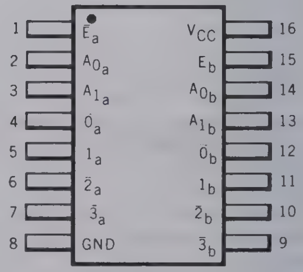

1
2
3
15
14
13
Ea
A0a
A1a
Eb
A0b
A1b
0a
1a
2a
3a
0b
1b
2b
3b
4
5
6
7
12
11
10
9

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1
2
3
4
5
6
7
8
Ēa
A0a
A1a
0̄a
1̄a
2̄a
3̄a
GND
VCC
Ēb
A0b
A1b
0̄b
1̄b
2̄b
3̄b
16
15
14
13
12
11
10
9

FLATPAK (TOP VIEW)

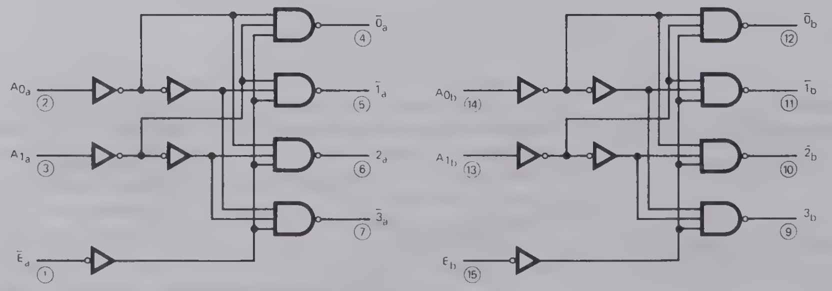

1
2
3
4
5
6
7
8
Ēa
A0a
A1a
0̄a
1a
2̄a
3̄a
GND
VCC
Eb
A0b
A1b
0̄b
1b
2̄b
3̄b
16
15
14
13
12
11
10
9

PIN NAMES
Decoder 1 and 2

		LOADING HIGH	LOADING LOW
$\bar{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\bar{0}$, $\bar{1}$, $\bar{2}$, $\bar{3}$	(Active LOW) Outputs	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM


A0a ②
A1a ③
Ēa ①
0̄a ④
1̄a ⑤
2̄a ⑥
3̄a ⑦
A0b ⑭
A1b ⑬
Eb ⑮
0̄b ⑫
1̄b ⑪
2̄b ⑩
3̄b ⑨

○= PIN NUMBERS

FUNCTIONAL DESCRIPTION — The 93L21 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in logic symbol. Each decoder can be used as a four output demultiplexer by using the enable as a data input.

The active LOW outputs facilitate memory addressing for units such as the 93402 associative memory. The active LOW outputs are also compatible with the active LOW enables of other LPTTL/MSI elements making the 93L21 useful in logic selection schemes.

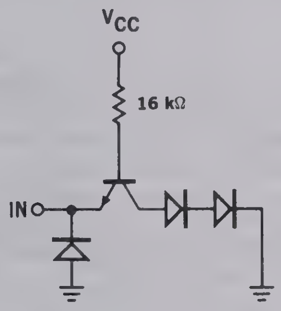
TRUTH TABLE
DECODER I & II

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

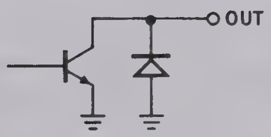
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

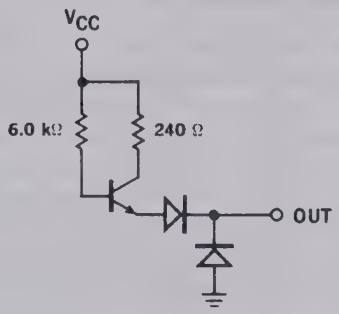


OUTPUTS EQUIVALENT CIRCUITS

OUTPUT LOW



OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L21XM	4.5 V	5.0 V	5.5 V	–55°C to 125°C
93L21XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		–0.25	–0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	–2.5	–16	–25	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		9.0	13.2	mA	V_{CC} = MAX., All Inputs at GND

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

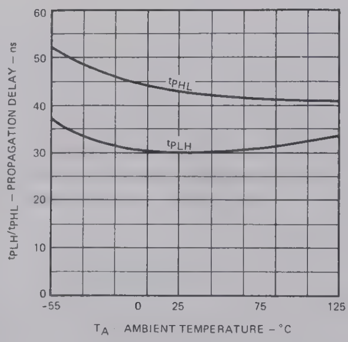
SWITCHING CHARACTERISTICS (T_A = 25°C)

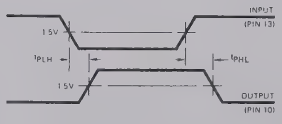
SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay A Input to Output		30	50	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay A Input to Output		43	65	ns	C_L = 15 pF, (See Fig. 1)
t_{PLH}	Turn Off Delay E Input to Output		23	40	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay E Input to Output		34	52	ns	C_L = 15 pF, (See Fig. 2)

SWITCHING TIME AND WAVEFORMS

All measurements are made with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. The active input is driven by a 9002 TTL gate. The input and output pins under test are loaded with 15 pF of capacitance (this includes probe and jig capacitance).

ADDRESS INPUT TO OUTPUT

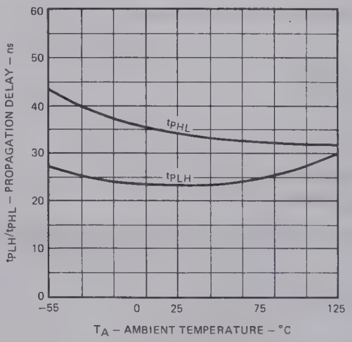


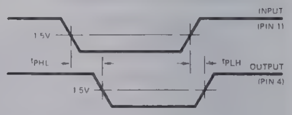


Other Conditions:
Pins 15, 14 = GND

Fig. 1.

ENABLE INPUT TO OUTPUT





Other Conditions:
Pins 2, 3 = GND

Fig. 2.

TTL/MSI 9322
QUAD TWO-INPUT MULTIPLEXER

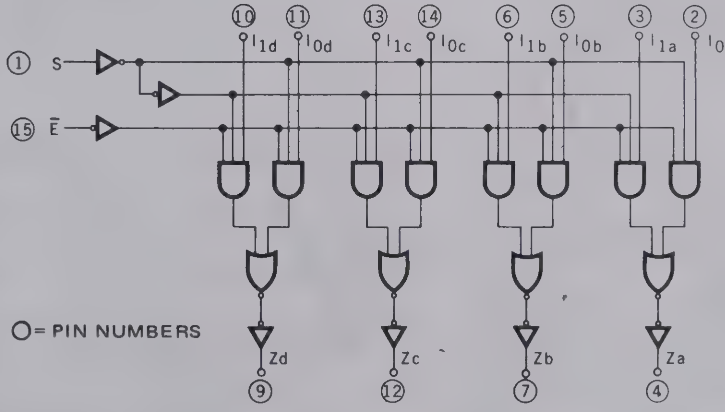
DESCRIPTION — The TTL/MSI 9322 is a Monolithic, High Speed, Quad Two-Input Digital Multiplexer Circuit, constructed with the Fairchild Planar* epitaxial process. It consists of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output. The circuit uses TTL for high speed, high fan out operation and is compatible with all other members of the Fairchild TTL family.

- **MULTIFUNCTION CAPABILITY***
- **20 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATIONS EFFECTS**

PIN NAMES		**LOADING** (Note a)
S	Common Selected Input	1 U.L.
$\overline{E}$	Enable (Active LOW) Inputs	1 U.L.
$I_{0a}, I_{1a}, I_{0b}, I_{1b}$, $I_{0c}, I_{1c}, I_{0d}, I_{1d}$	Multiplexer Inputs	1 U.L.
Z_a, Z_b, Z_c, Z_d	Multiplexer Output (Note b)	10 U.L.

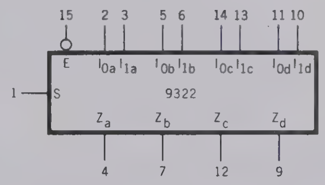
Notes:
a. 1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



⑩ I_{1d}
⑪ I_{0d}
⑬ I_{1c}
⑭ I_{0c}
⑥ I_{1b}
⑤ I_{0b}
③ I_{1a}
② I_{0a}
① S
⑮ $\overline{E}$
○= PIN NUMBERS
Zd ⑨
Zc ⑫
Zb ⑦
Za ④

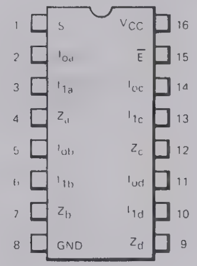
LOGIC SYMBOL



15 2 3 5 6 14 13 11 10
E
I_{0a} I_{1a} I_{0b} I_{1b} I_{0c} I_{1c} I_{0d} I_{1d}
1 S
9322
Z_a Z_b Z_c Z_d
4 7 12 9

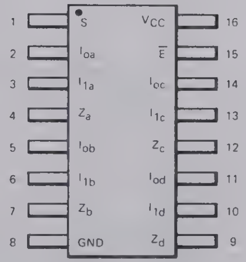
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 S
2 I_{0a}
3 I_{1a}
4 Z_a
5 I_{0b}
6 I_{1b}
7 Z_b
8 GND
16 V_{CC}
15 $\overline{E}$
14 I_{0c}
13 I_{1c}
12 Z_c
11 I_{0d}
10 I_{1d}
9 Z_d

FLATPAK (TOP VIEW)



1 S
2 I_{0a}
3 I_{1a}
4 Z_a
5 I_{0b}
6 I_{1b}
7 Z_b
8 GND
16 V_{CC}
15 $\overline{E}$
14 I_{0c}
13 I_{1c}
12 Z_c
11 I_{0d}
10 I_{1d}
9 Z_d

*Planar is a patented Fairchild process.

FUNCTIONAL DESCRIPTION — The 9322 quad 2-input multiplexer is a member of the Fairchild family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select four bits of either data or control from two sources, in one package. The Enable input ($\overline{E}$) is active LOW. When not activated all outputs (Z) are LOW regardless of all other inputs.

The 9322 quad 2-input multiplexer is the logical implementation of a four-pole, two position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

$$Z_a = E \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = E \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = E \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = E \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

A common use of the 9322 is the moving of data from a group of registers to four common output busses. The particular register from which the data comes is determined by the state of the select input. A less obvious use is as a function generator. The 9322 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

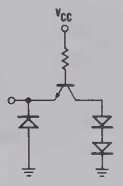
TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

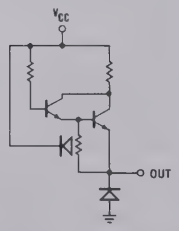
H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Logic Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

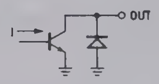
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE

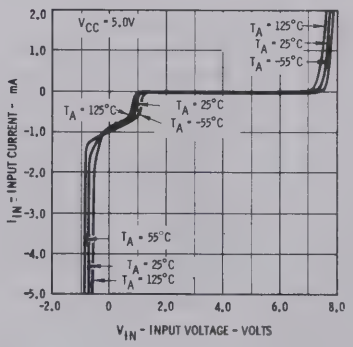


Fig. 1.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

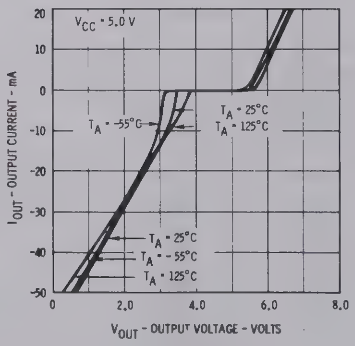


Fig. 2.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

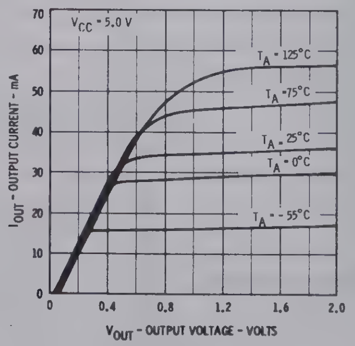


Fig. 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9322XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9322XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., $I_{IN} = -12$ mA, $T_A = 25°C$
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., $I_{OH} = -800\ \mu A$ $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-30	-60	-100	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		30	47	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

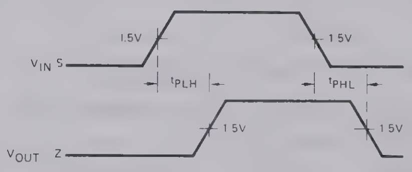
SYMBOL	PARAMETER	9322XM(MIL)			9322XC(IND)			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output (S to Z)		17	25		17	30	ns	V_{CC} = 5.0 V C_L = 15 pF	See Figure 4
t_{PHL}	Turn On Delay Input to Output (S to Z)		20	27		20	31	ns		

SWITCHING CHARACTERISTICS

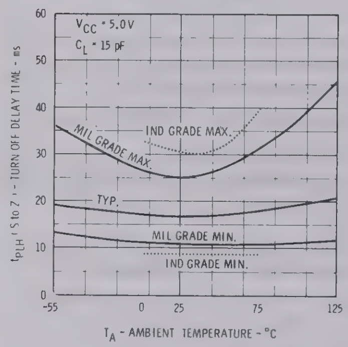
Fig. 4.

t_{PLH}/t_{PHL} — S to Z

Other Conditions: $\overline{E}$ = L, I_0 = L, I_1 = H


1.5V
1.5V
VIN S
tPLH
tPHL
1.5V
1.5V
VOUT Z

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z)

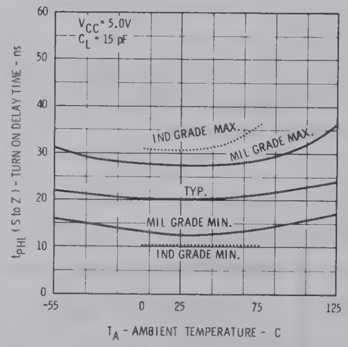
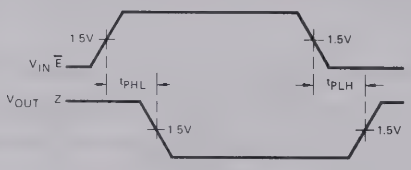


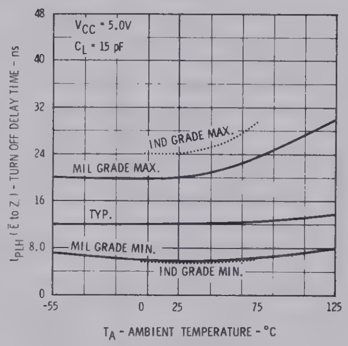
Fig. 5.

t_{PLH}/t_{PHL} — $\overline{E}$ to Z

Other Conditions: All Other Inputs HIGH


1.5V
1.5V
VIN E
tPHL
tPLH
VOUT Z
1.5V
1.5V

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z)

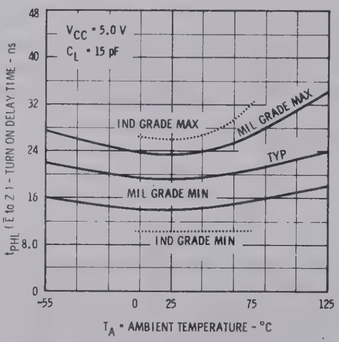
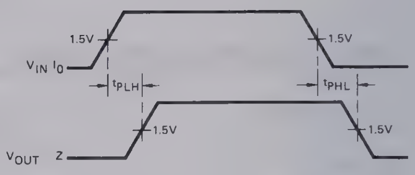


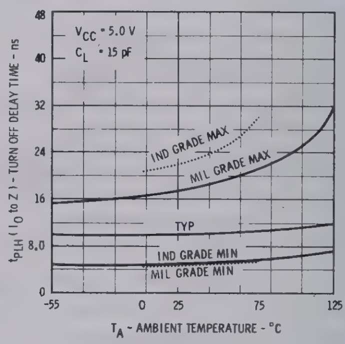
Fig. 6.

t_{PLH}/t_{PHL} — I_0 to Z

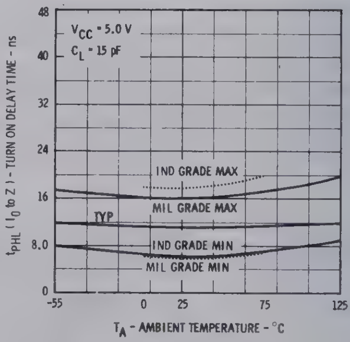
Other Conditions: $\overline{E}$ = L, S = L


1.5V
1.5V
VIN I0
tPLH
tPHL
1.5V
1.5V
VOUT Z

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_0 to Z)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_0 to Z)



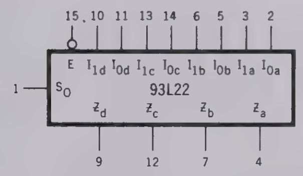
LPTTL/MSI 93L22

LOW POWER QUAD TWO-INPUT MULTIPLEXER

DESCRIPTION — The LPTTL/MSI 93L22 is a monolithic, medium speed, Quad Two-Input Digital Multiplexer, constructed with the Fairchild Planar* epitaxial process. It consists of four multiplexing circuits with common select and enable logic. Each circuit contains two inputs and one output. The circuit uses TTL technology and is compatible with the Fairchild TTL family.

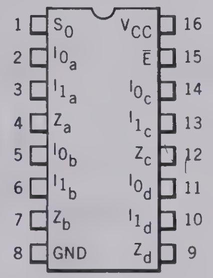
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **TYPICAL PROPAGATION DELAY OF 44 ns**
- **TYPICAL POWER DISSIPATION OF 45 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

LOGIC SYMBOL


15
10
11
13
14
6
5
3
2
E
I_{1d}
I_{0d}
I_{1c}
I_{0c}
I_{1b}
I_{0b}
I_{1a}
I_{0a}
1
S_0
93L22
Z_d
Z_c
Z_b
Z_a
9
12
7
4

V_{CC} = Pin 16
GND = Pin 8

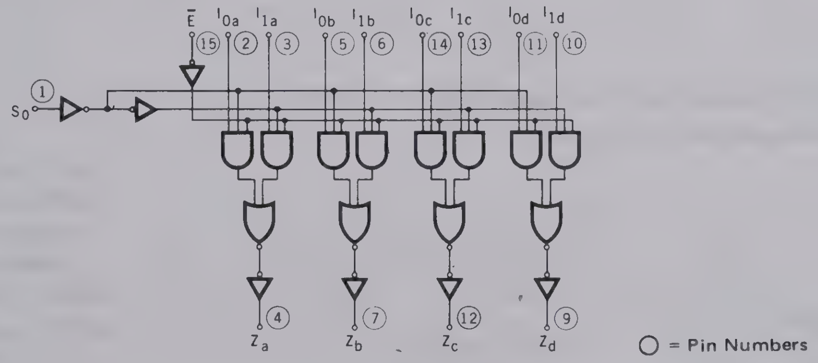
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1
S_0
V_{CC}
16
2
I_{0a}
$\overline{E}$
15
3
I_{1a}
I_{0c}
14
4
Z_a
I_{1c}
13
5
I_{0b}
Z_c
12
6
I_{1b}
I_{0d}
11
7
Z_b
I_{1d}
10
8
GND
Z_d
9

PIN NAMES		LOADING HIGH	LOADING LOW
S_0	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1	Multiplexers Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output	10 U.L.	2.5 U.L.

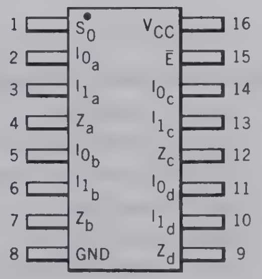
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM


$\overline{E}$
I_{0a}
I_{1a}
I_{0b}
I_{1b}
I_{0c}
I_{1c}
I_{0d}
I_{1d}
(15)
(2)
(3)
(5)
(6)
(14)
(13)
(11)
(10)
(1)
S_0
(4)
(7)
(12)
(9)
Z_a
Z_b
Z_c
Z_d

○ = Pin Numbers

FLATPAK (TOP VIEW)


1
S_0
V_{CC}
16
2
I_{0a}
$\overline{E}$
15
3
I_{1a}
I_{0c}
14
4
Z_a
I_{1c}
13
5
I_{0b}
Z_c
12
6
I_{1b}
I_{0d}
11
7
Z_b
I_{1d}
10
8
GND
Z_d
9

*Planar is a patented Fairchild process.

FUNCTIONAL DESCRIPTION — The 93L22 quad two-input multiplexer is a member of the Fairchild family of low power medium scale integrated digital building blocks. It provides, in one package, the ability to select four bits of either data or control from four 2-bit sources. The enable input ($\overline{E}$) is active LOW. When not activated all outputs (Z) are LOW regardless of all other inputs. The 93L22 quad two input multiplexer is the logical implementation of a four-pole two position switch, with the position of the switch being set by the logic level supplied to the one select input. The logic equations for the outputs are shown below:

$$Z_a = E \cdot (I_{1a} \cdot S_0 + I_{0a} \cdot \overline{S_0}) \quad Z_b = E \cdot (I_{1b} \cdot S_0 + I_{0b} \cdot \overline{S_0}) \quad Z_c = E \cdot (I_{1c} \cdot S_0 + I_{0c} \cdot \overline{S_0}) \quad Z_d = E \cdot (I_{1d} \cdot S_0 + I_{0d} \cdot \overline{S_0})$$

A common use of the 93L22 is the moving of data from two registers to common output busses. The particular register from which the data came would be determined by the state of the select input. A less obvious use is a function generator. The 93L22 can generate four functions of two variables with one variable common. This is useful implementing gating functions.

TRUTH TABLE

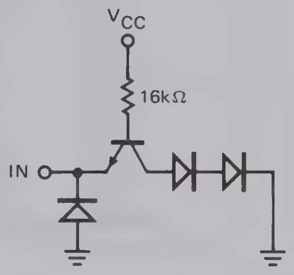
Identical for Each Multiplexer

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S_0	I_{0Y}	I_{1Y}	Z_Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

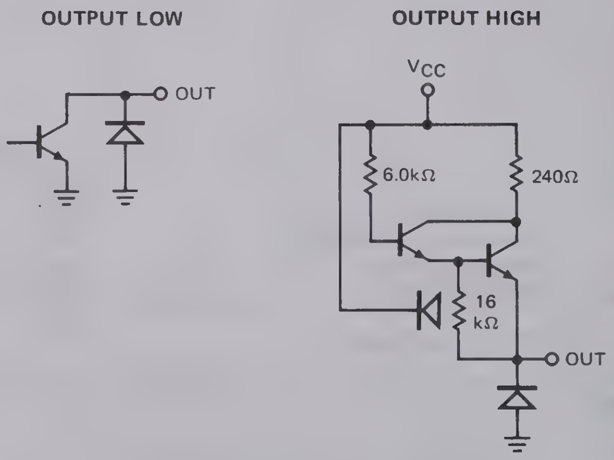
H = HIGH voltage level
L = LOW voltage level
X = Level does not affect output
Y = a, b, c, d

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS
EQUIVALENT CIRCUIT



OUTPUTS
EQUIVALENT CIRCUITS


OUTPUT LOW

OUTPUT HIGH

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
*Input Voltage (dc)	–0.5V to +5.5V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
93L22XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L22XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3V
I_{IH}	Input HIGH Current		2.0	20	µA	V_{CC} = MAX., V_{IN} = 2.4V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{SC} (Note 5)	Output Short Circuit Current	−10	−21	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0V
I_{CC}	Power Supply Current		9.0	13.2	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

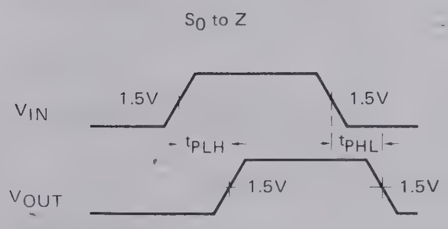
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{PLH} (S_0 to Z)	Turn Off Delay Input to Output		26	36	ns	V_{CC} = 5.0 V
t_{PHL} (S_0 to Z)	Turn On Delay Input to Output		36	49	ns	C_L = 15 pF

SWITCHING TIME WAVEFORMS



TTL/MSI 9324
5-BIT COMPARATOR

DESCRIPTION — The TTL/MSI 9324 is a High Speed Expandable Comparator which provides comparison between two 5-bit words and gives three outputs, "less than", "greater than" and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

- **THREE SEPARATE OUTPUTS . . . $A < B$, $A > B$, $A = B$**
- **EASILY EXPANDABLE**
- **ACTIVE LOW LEVEL ENABLE INPUT**
- **HIGH DRIVE OUTPUT CIRCUITRY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED**
- **TERMINATION EFFECTS**
- **COMPATIBLE WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**

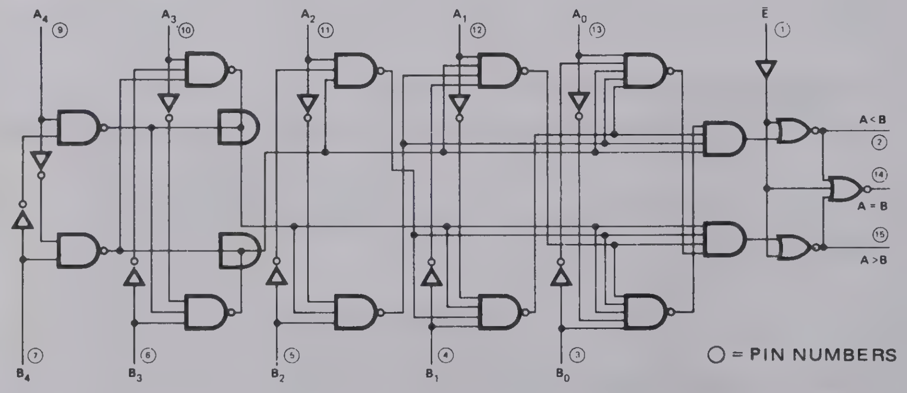
PIN NAMES		**LOADING** (Note a)
$\overline{E}$	Enable (Active LOW) Input	2 U.L.
A_0, A_1, A_2, A_3, A_4	Word A Parallel Inputs	2 U.L.
B_0, B_1, B_2, B_3, B_4	Word B Parallel Inputs	2 U.L.
$A < B$	A Less Than B Output (Note b)	10 U.L.
$A > B$	A Greater Than B Output (Note b)	10 U.L.
$A = B$	A Equal to B Output (Note b)	10 U.L.

Notes:

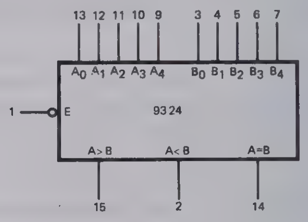
a. 1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW

b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor

LOGIC DIAGRAM

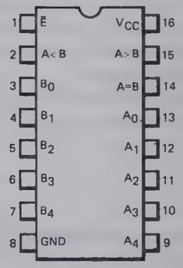

A4 ⑨
A3 ⑩
A2 ⑪
A1 ⑫
A0 ⑬
$\overline{E}$ ①
A<B ②
⑭ A = B
⑮ A>B
⑦ B4
⑥ B3
⑤ B2
④ B1
③ B0
○ = PIN NUMBERS

LOGIC SYMBOL

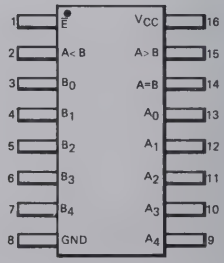

13 12 11 10 9
3 4 5 6 7
A0 A1 A2 A3 A4
B0 B1 B2 B3 B4
1
E
9324
A>B
A<B
A=B
15
2
14

V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 $\overline{E}$
2 A<B
3 B0
4 B1
5 B2
6 B3
7 B4
8 GND
16 VCC
15 A>B
14 A=B
13 A0
12 A1
11 A2
10 A3
9 A4

FLATPAK (TOP VIEW)


1 $\overline{E}$
2 A<B
3 B0
4 B1
5 B2
6 B3
7 B4
8 GND
16 VCC
15 A>B
14 A=B
13 A0
12 A1
11 A2
10 A3
9 A4

FUNCTIONAL DESCRIPTION — The 9324 5-bit comparator uses combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable input ($\overline{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is HIGH and B_4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\overline{E}$.

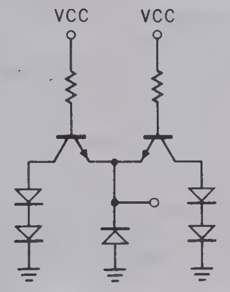
TRUTH TABLE

$\overline{E}$	Ay	By	A < B	A > B	A = B
H	X	X	L	L	L
L	Word A =	Word B	L	L	H
L	Word A >	Word B	L	H	L
L	Word B >	Word A	H	L	L

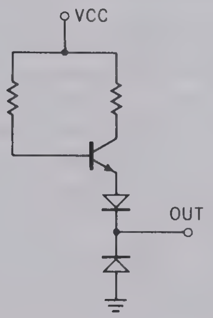
H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Voltage Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

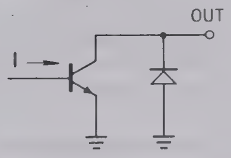
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE

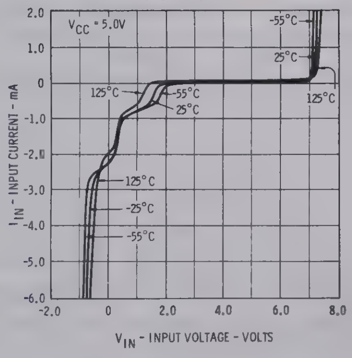


Fig. 1.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

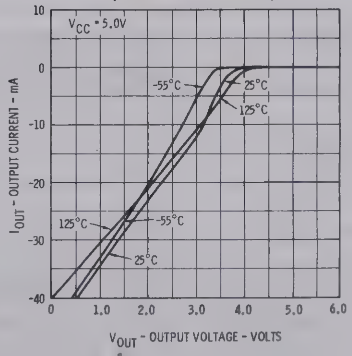


Fig. 2.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

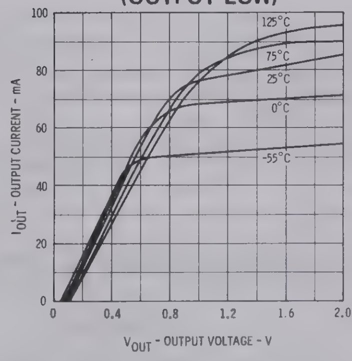


Fig. 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
9324XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9324XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., $I_{IN} = -12\text{mA}, T_A = 25°\text{C}$
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., $I_{OH} = -800\ \mu A$ $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		20	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current		−1.92	−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−50	−70	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		40	81	mA	V_{CC} = MAX.

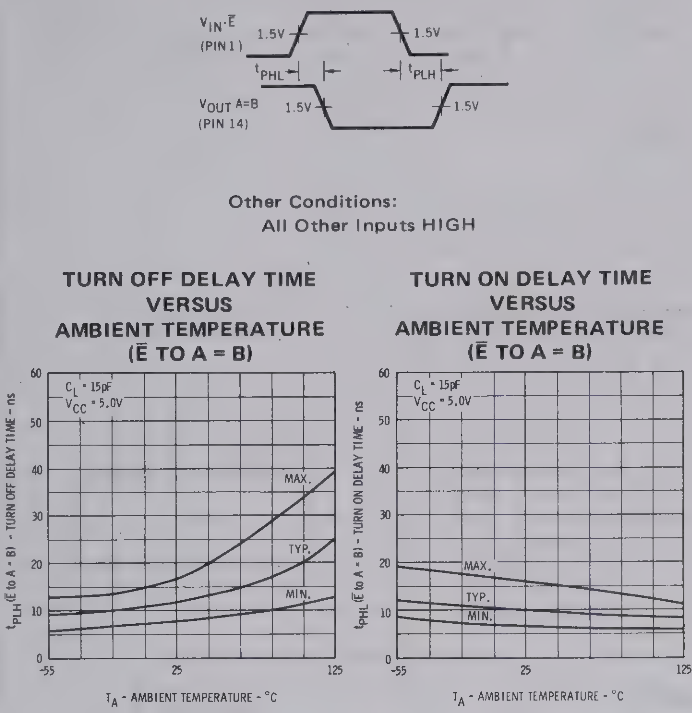
NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°\text{C}$)

SYMBOL	PARAMETER	9324XM MIN.	TYP.	MAX.	9324XC MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{PLH}	Turn Off Delay Input to Output (A_2 to A = B)		40	45		40	48	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay Input to Output (A_2 to A = B)		35	42		35	45	ns	

SWITCHING CHARACTERISTICS

t_{PLH}/t_{PHL} – $\overline{E}$ to A = B



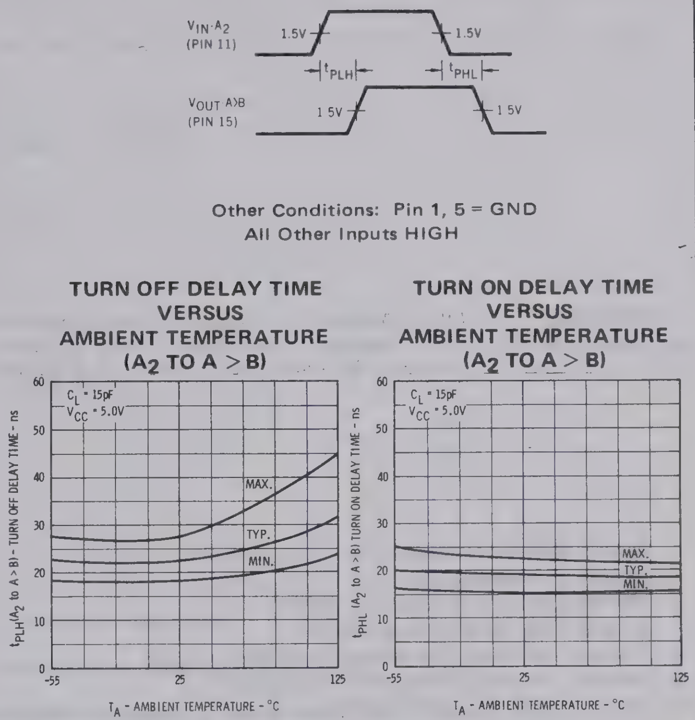
Other Conditions:
All Other Inputs HIGH

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ TO A = B)

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ TO A = B)

Fig. 4.

t_{PLH}/t_{PHL} – A_2 to A > B



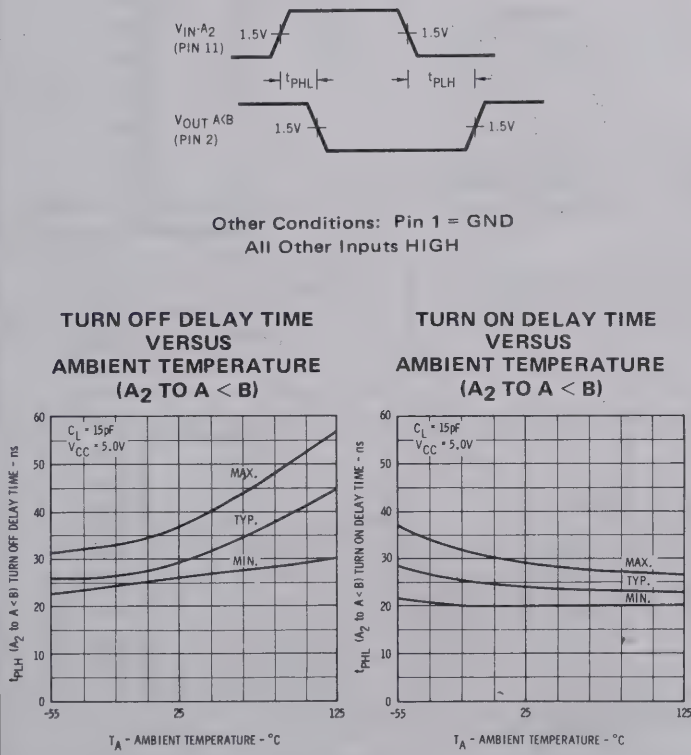
Other Conditions: Pin 1, 5 = GND
All Other Inputs HIGH

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A > B)

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A > B)

Fig. 5.

t_{PLH}/t_{PHL} – A_2 to A < B



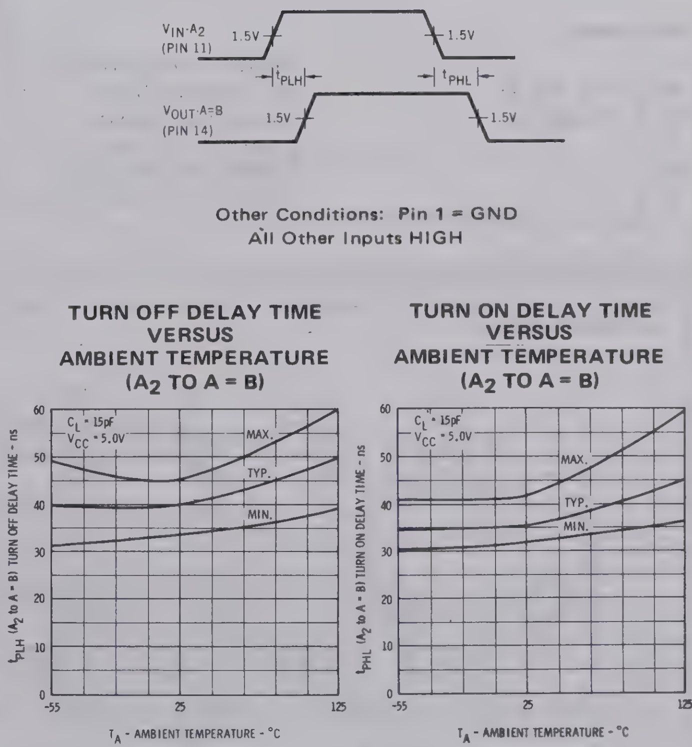
Other Conditions: Pin 1 = GND
All Other Inputs HIGH

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A < B)

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A < B)

Fig. 6

t_{PLH}/t_{PHL} – A_2 to A = B



Other Conditions: Pin 1 = GND
All Other Inputs HIGH

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A = B)

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A = B)

Fig. 7.

LPTTL/MSI 93L24

LOW POWER 5-BIT COMPARATOR

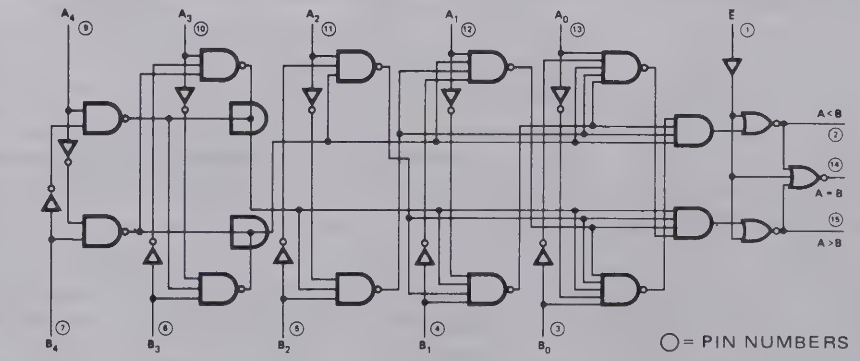
DESCRIPTION — The LPTTL/MSI 93L24 is a Medium Speed Expandable Comparator which provides comparison between two 5-bit words and gives three outputs, "less than", "greater than", and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

- THREE SEPARATE OUTPUTS . . . A < B, A > B, A = B
- EASILY EXPANDABLE
- ACTIVE LOW-LEVEL ENABLE INPUT
- HIGH DRIVE OUTPUT CIRCUITRY
- TYPICAL PROPAGATION DELAY OF 55 ns (A > B)
- TYPICAL POWER DISSIPATION OF 52 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

PIN NAMES		LOADING	
		HIGH	LOW
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
A_0, A_1, A_2, A_3, A_4	Word A Parallel Inputs	1.0 U.L.	0.5 U.L.
B_0, B_1, B_2, B_3, B_4	Word B Parallel Inputs	1.0 U.L.	0.5 U.L.
A < B	A Less than B Output	9 U.L.	2.25 U.L.
A > B	A Greater than B Output	9 U.L.	2.25 U.L.
A = B	A Equal to B Output	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

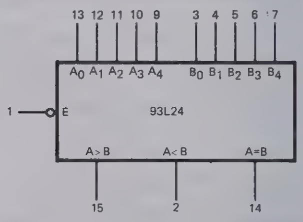
LOGIC DIAGRAM



A4 ⑨
A3 ⑩
A2 ⑪
A1 ⑫
A0 ⑬
E ①
A<B ②
A=B ⑭
A>B ⑮
B4 ⑦
B3 ⑥
B2 ⑤
B1 ④
B0 ③

○= PIN NUMBERS

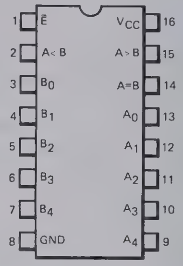
LOGIC SYMBOL



13 12 11 10 9
3 4 5 6 7
A0 A1 A2 A3 A4
B0 B1 B2 B3 B4
1
E
93L24
A>B
A<B
A=B
15
2
14

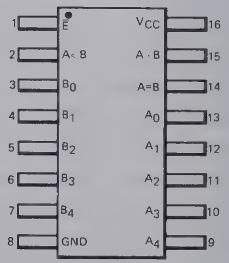
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 E
2 A<B
3 B0
4 B1
5 B2
6 B3
7 B4
8 GND
16 VCC
15 A>B
14 A=B
13 A0
12 A1
11 A2
10 A3
9 A4

FLATPAK(TOP VIEW)



1 E
2 A<B
3 B0
4 B1
5 B2
6 B3
7 B4
8 GND
16 VCC
15 A>B
14 A=B
13 A0
12 A1
11 A2
10 A3
9 A4

FUNCTIONAL DESCRIPTION – The 93L24 5-bit comparator uses combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW enable input ($\bar{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion as shown in Figure 1.

The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is HIGH and B_4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\bar{E}$.

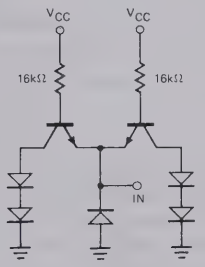
TRUTH TABLE

$\bar{E}$	A	B	A < B	A > B	A = B
H	X	X	L	L	L
L	Word A = Word B		L	L	H
L	Word A > Word B		L	H	L
L	Word A < Word B		H	L	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Either HIGH or LOW Voltage Level

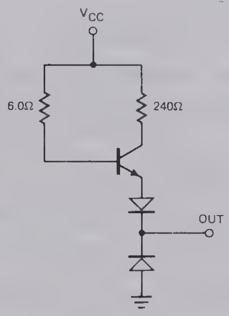
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

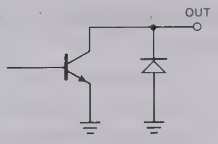


OUTPUTS EQUIVALENT CIRCUITS

OUTPUT HIGH



OUTPUT LOW



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L24XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L24XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC}=MIN.,I_{OH}= −0.4mA(Pin 14), I_{OH}= −0.36mA(Pin 2&15), V_{IN}=V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pin 14) I_{OL} = 3.6 mA (Pins 2 & 15) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.5	−0.8	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		4.0	40	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 5)	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		10.4	21	mA	V_{CC} = MAX.

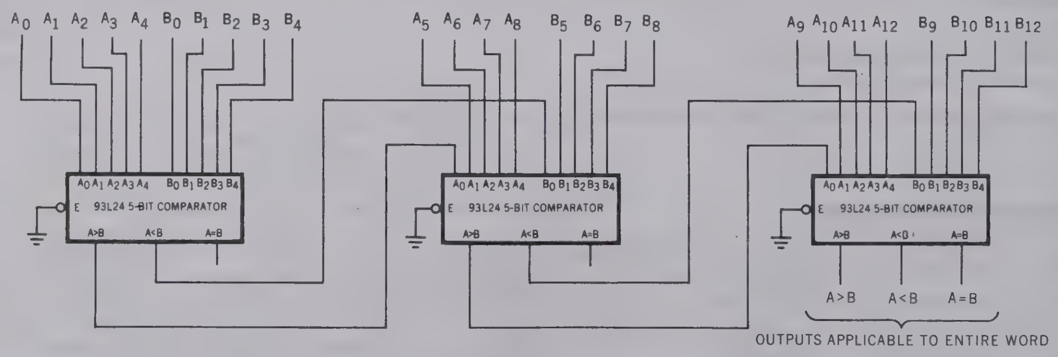
NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Enable to Output ($\overline{E}$ to A = B)		21 22	32 35	ns ns	C_L = 15 pF V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Data to Output (A_2 to A > B)		35 50	54 75	ns ns	
t_{PLH} t_{PHL}	Data to Output (A_2 to A < B)		46 51	70 77	ns ns	
t_{PLH} t_{PHL}	Data to Output (A_2 to A = B)		65 68	100 102	ns ns	

SERIAL EXPANSION OF 93L24 FOR LONGER WORD LENGTHS


A0 A1 A2 A3 A4 B0 B1 B2 B3 B4
A5 A6 A7 A8 B5 B6 B7 B8
A9 A10 A11 A12 B9 B10 B11 B12
A0 A1 A2 A3 A4 B0 B1 B2 B3 B4
E
93L24 5-BIT COMPARATOR
A>B A<B A=B
A>B A<B A=B
OUTPUTS APPLICABLE TO ENTIRE WORD

For each additional 93L24 added four extra bits can be accommodated.

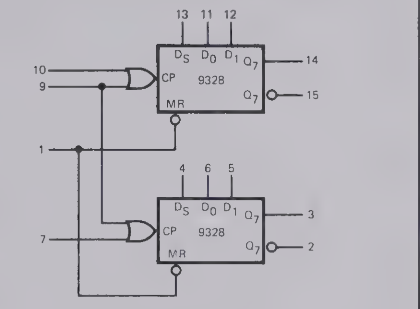
Fig. 1.

TTL/MSI 9328
DUAL 8-BIT SHIFT REGISTER

DESCRIPTION — The 9328 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers that will shift at greater than 20 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

- **20 MHz SHIFT FREQUENCY**
- **TWO INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**
- **TYPICAL POWER DISSIPATION OF 300 mW**
- **TTL COMPATIBLE**
- **INPUT DIODE CLAMPING**

LOGIC SYMBOL


13
11
12
D_S
D_0
D_1
Q_7
14
10
9
CP
9328
$\overline{Q_7}$
15
MR
1
4
6
5
D_S
D_0
D_1
Q_7
3
7
CP
9328
$\overline{Q_7}$
2
MR

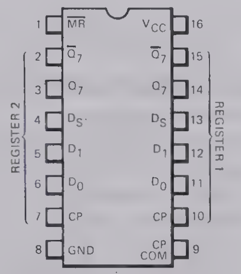
V_{CC} = Pin 16
Gnd = Pin 8

PIN NAMES

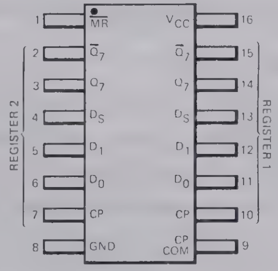
PIN NAMES		LOADING (Note a)
D_S	Data Select Input	2 U.L.
D_0, D_1	Data Inputs	1 U.L.
CP	Clock (Active HIGH) Going Edge Input	
	Common (Pin 9)	3 U.L.
	Separate (Pins 7 and 10)	1.5 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_7	Last Stage Output (Note b)	10 U.L.
$\overline{Q_7}$	Complementary Output (Note b)	10 U.L.

NOTES
a. 1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor

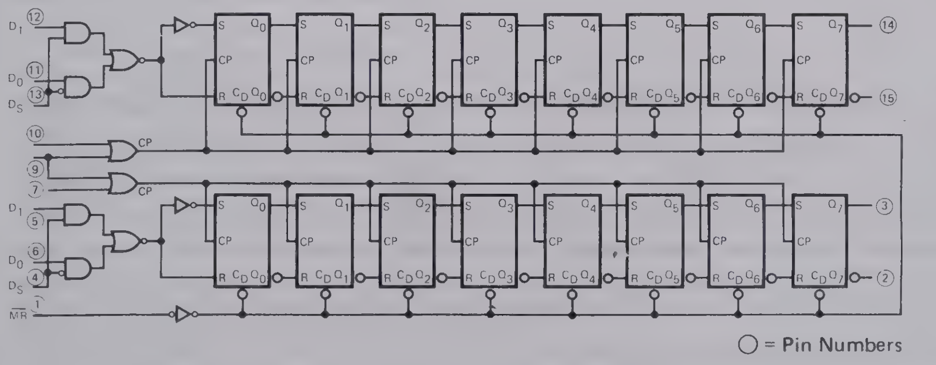
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1
$\overline{MR}$
V_{CC}
16
2
$\overline{Q}_7$
$\overline{Q}_7$
15
3
Q_7
Q_7
14
4
D_S
D_S
13
5
D_1
D_1
12
6
D_0
D_0
11
7
CP
CP
10
8
GND
CP COM
9
REGISTER 2
REGISTER 1

FLATPAK (TOP VIEW)


1
$\overline{MR}$
V_{CC}
16
2
$\overline{Q}_7$
$\overline{Q}_7$
15
3
Q_7
Q_7
14
4
D_S
D_S
13
5
D_1
D_1
12
6
D_0
D_0
11
7
CP
CP
10
8
GND
CP COM
9
REGISTER 2
REGISTER 1

LOGIC DIAGRAM


D_1 ⑫
D_0 ⑪
D_S ⑬
⑩
⑨
⑦
CP
CP
D_1 ⑤
D_0 ⑥
D_S ④
$\overline{MR}$ ①
S
CP
R
C_D
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
⑭
⑮
③
②

○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW to HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH to LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a two input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input (D_S) following the Boolean expression:

Serial data in: $S_D = \overline{D}_S D_0 + D_S D_1$

An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all sixteen stages independently of any other input signal.

TRUTH TABLE

SHIFT SELECTION

D_S	D_0	D_1	Q_7 (t_{n+8})
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

n+8 = Indicates state after eight clock pulse
L = LOW voltage level
H = HIGH voltage level
X = Either HIGH or LOW voltage level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9328XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9328XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 µA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{MR}$, D_0, D_1 CP (Pins 7 & 10) D_S CP (Pin 9)		 10 15 20 30	 40 60 80 120	µA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current all inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current $\overline{MR}$, D_0, D_1 CP (Pins 7 & 10) D_S CP (Pin 9)		 −0.96 −1.44 −1.92 −2.88	 −1.6 −2.4 −3.2 −4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−50	−70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		60	77	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Clock to Output		13	20	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay Clock to Output		22	35	ns		
t_{PHL}	Turn On Delay Master Reset to Q Output		35	50	ns	Fig. 2	
f_{sr}	Shift Right Frequency	20	30		MHz	Fig. 1	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
t_{pw} (CP)	Clock Pulse Width	25	17		ns	Fig. 1	V_{CC} = 5.0 V
t_{pw} ($\overline{MR}$) (CPH)	Master Reset Pulse Width with Clock HIGH	30	20		ns	Fig. 2	
t_{pw} ($\overline{MR}$) (CPL)	Master Reset Pulse Width with Clock LOW	40	24		ns		
t_s (Data)	Set-up Time Data to Clock	20	10		ns	Fig. 3	
t_h (Data)	Hold Time Data to Clock	0			ns		
t_{rec} ($\overline{MR}$)	Recovery Time Master Reset to Clock	33	19		ns	Fig. 2	

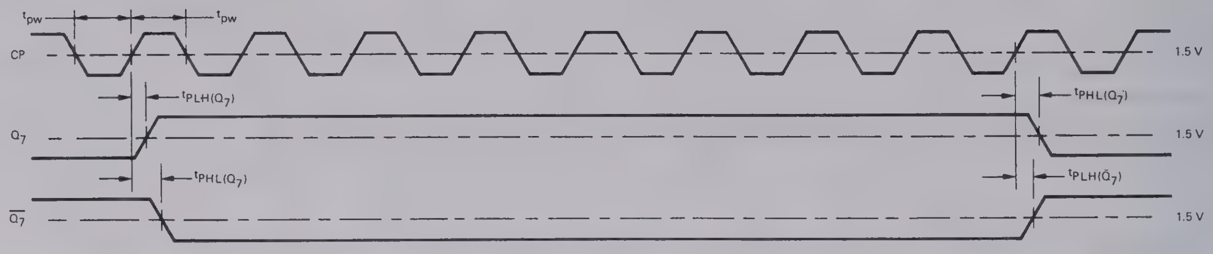
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SWITCHING WAVEFORMS

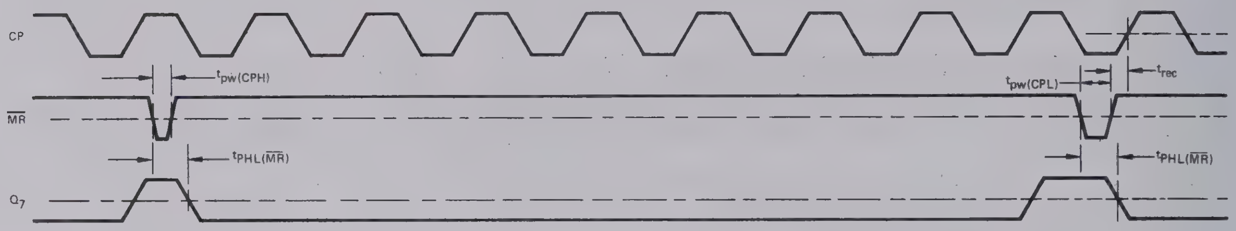
CLOCK TO OUTPUT DELAYS AND MINIMUM CLOCK PULSE WIDTH


t_{pw}
t_{pw}
CP
1.5 V
$t_{PLH(Q_7)}$
$t_{PHL(Q_7)}$
Q_7
1.5 V
$t_{PHL(Q_7)}$
$t_{PLH(\overline{Q}_7)}$
$\overline{Q_7}$
1.5 V

OTHER CONDITIONS: $\overline{Q}_7$ is connected to D_1. Other clock is LOW.

Fig. 1

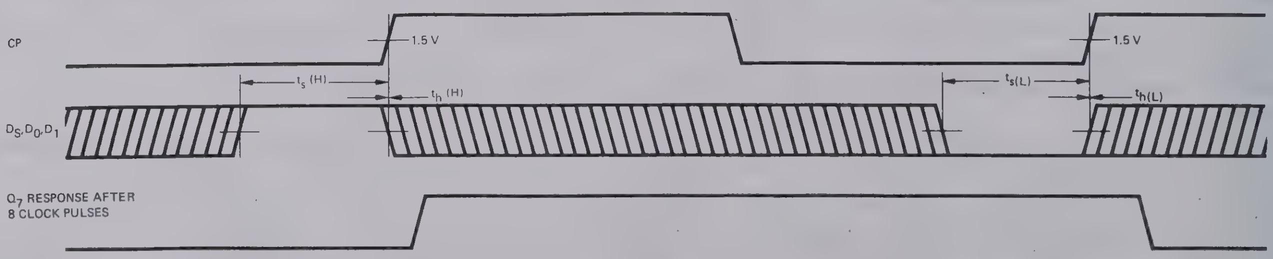
MASTER RESET TO OUTPUT TURN ON DELAY AND MINIMUM MASTER RESET PULSE WIDTHS


CP
$t_{pw(CPH)}$
$t_{pw(CPL)}$
t_{rec}
$\overline{MR}$
$t_{PHL(\overline{MR})}$
$t_{PHL(\overline{MR})}$
Q_7

OTHER CONDITIONS: D_S, D_1, D_0 are HIGH. Other clock input is LOW.

Fig. 2

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR DATA INPUTS


CP
1.5 V
1.5 V
t_s (H)
t_h (H)
$t_{s(L)}$
$t_{h(L)}$
D_S, D_0, D_1
Q_7 RESPONSE AFTER 8 CLOCK PULSES

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

OTHER CONDITIONS: $\overline{MR}$ = HIGH, other clock input is LOW.

Fig. 3

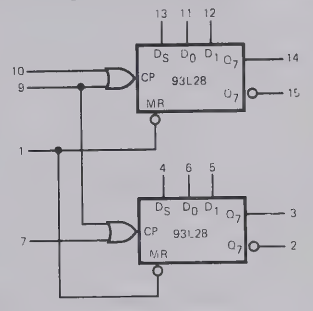
LPTTL/MSI 93L28

LOW POWER DUAL 8-BIT SHIFT REGISTER

DESCRIPTION — The LPTTL/MSI 93L28 is a medium speed Serial Storage Element providing sixteen bits of storage in the form of two 8-bit registers that will shift at greater than 5 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each 8-bit register, and both registers may be master reset from a common input.

- **10 MHz TYPICAL SHIFT FREQUENCY**
- **TWO-INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**
- **TYPICAL POWER DISSIPATION OF 80 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

LOGIC SYMBOL

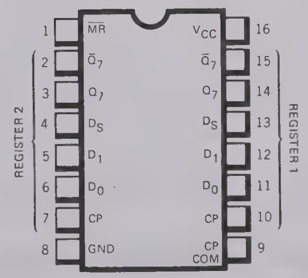

13 11 12
D_S D_0 D_1 Q_7
CP 93L28
$\overline{Q}_7$
MR
14
15
10
9
1
4 6 5
D_S D_0 D_1 Q_7
CP 93L28
$\overline{Q}_7$
MR
3
2
7

V_{CC} = PIN 16
GND = PIN 8

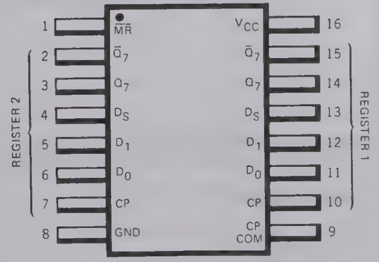
PIN NAMES		LOADING HIGH	LOADING LOW
D_S	Data Select Input	1.0 U.L.	0.5 U.L.
D_0, D_1	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input		
	Common	1.5 U.L.	0.75 U.L.
	Separate	0.75 U.L.	0.375 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_7	Last Stage Output	8.0 U.L.	2.0 U.L.
$\overline{Q}_7$	Complementary Output	8.0 U.L.	2.0 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

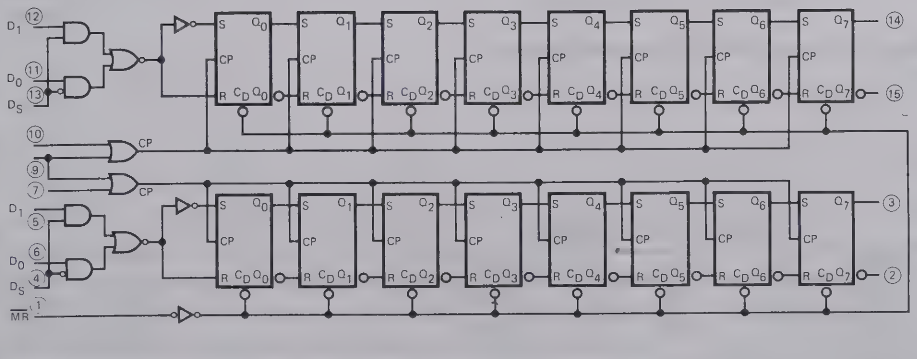
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 $\overline{MR}$
2 $\overline{Q}_7$
3 Q_7
4 D_S
5 D_1
6 D_0
7 CP
8 GND
16 V_{CC}
15 $\overline{Q}_7$
14 Q_7
13 D_S
12 D_1
11 D_0
10 CP
9 CP COM
REGISTER 2
REGISTER 1

FLATPAK (TOP VIEW)


1 $\overline{MR}$
2 $\overline{Q}_7$
3 Q_7
4 D_S
5 D_1
6 D_0
7 CP
8 GND
16 V_{CC}
15 $\overline{Q}_7$
14 Q_7
13 D_S
12 D_1
11 D_0
10 CP
9 CP COM
REGISTER 2
REGISTER 1

LOGIC DIAGRAM


D_1 12
D_0 11
D_S 13
10
9
7
CP
D_1 5
D_0 6
D_S 4
$\overline{MR}$ 1
S Q_0 CP R C_D $\overline{Q}_0$
S Q_1 CP R C_D $\overline{Q}_1$
S Q_2 CP R C_D $\overline{Q}_2$
S Q_3 CP R C_D $\overline{Q}_3$
S Q_4 CP R C_D $\overline{Q}_4$
S Q_5 CP R C_D $\overline{Q}_5$
S Q_6 CP R C_D $\overline{Q}_6$
S Q_7 CP R C_D $\overline{Q}_7$
14
15
3
2

○ = PIN NUMBERS

FUNCTIONAL DESCRIPTION — The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 & 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW to HIGH transition of either or both of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master. The now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH to LOW transition of the last remaining high clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a two-input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input D_S following the Boolean expression:

Serial data in: $S_D = \overline{D}_S D_0 + D_S D_1$.

An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all sixteen stages independently of any other input signal.

TRUTH TABLE

SHIFT SELECTION

D_S	D_0	D_1	$Q_7(t_{n+8})$
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

n+8 = indicates state after eight clock pulse
L = LOW voltage level
H = HIGH voltage level
X = Either HIGH or LOW voltage level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L28XM	4.5V	5.0V	5.5V	-55°C to 125°C
93L28XC	4.75V	5.0V	5.25V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage For All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Voltage For All Inputs
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.3 V
	$\overline{MR}$, D_0 & D_1		−0.25	−0.4		
	CP (Pins 7 & 10)		−0.38	−0.6		
	D_S		−0.50	−0.8		
	CP (Pin 9)		−0.75	−1.2		
I_{IH}	Input HIGH Current				µA	V_{CC} = MAX., V_{IN} = 2.4 V
	$\overline{MR}$, D_0 & D_1		2.0	20		
	CP (Pins 7 & 10)		3.0	30		
	D_S		4.0	40		
	CP (Pin 9)		6.0	60		
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		16	25.3	mA	V_{CC} = MAX.

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

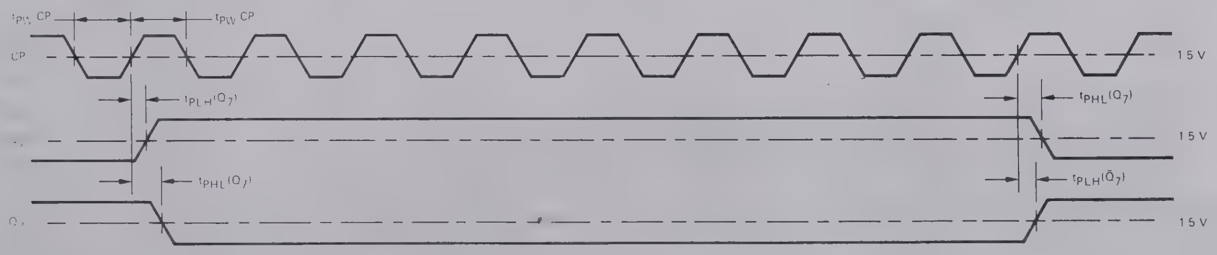
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{PLH} (Q_7 & $\overline{Q}_7$)	Turn-Off Delay (clock to output)		30	45	ns	V_{CC} = 5.0V, C_L = 15pF Fig. 1
t_{PHL} (Q_7 & $\overline{Q}_7$)	Turn-On Delay (clock to output)		55	80	ns	
t_{PHL} ($\overline{MR}$)	Turn-On Delay (Master reset to output)		72	110	ns	V_{CC} = 5.0V, C_L = 15pF,

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{PW} CP	Min. Clock Pulse Width	55	30		ns	V_{CC} = 5.0V, C_L = 15pF Fig. 1
t_{PW} $\overline{MR}$ (CPH)	Min. Master Reset Pulse Width with Clock HIGH	60	28		ns	V_{CC} = 5.0V, C_L = 15pF
t_{PW} $\overline{MR}$ (CPL)	Min. Master Reset Pulse Width with Clock LOW	70	38		ns	V_{CC} = 5.0V, C_L = 15pF

SWITCHING WAVEFORMS



NOTE: $\overline{Q}_7$ is connected to D_1. Other clock is grounded.

Fig. 1

TTL/MSI 9334

8-BIT ADDRESSABLE LATCH

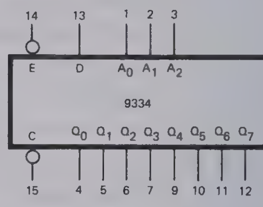
DESCRIPTION — The TTL/MSI 9334 is a high speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active level LOW common clear for resetting all latches, as well as, an active level LOW enable. The 9334 is compatible with all members of Fairchild's TTL family.

- SERIAL TO PARALLEL CAPABILITY
- 8-BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE
- RANDOM (ADDRESSABLE) DATA ENTRY
- ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY
- EASILY EXPANDABLE
- COMMON CLEAR
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- TTL COMPATIBLE

PIN NAMES		LOADING (Note a)
A_0, A_1, A_2	Address Inputs	1 U.L.
D	Data Input	1 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.5 U.L.
$\overline{C}$	Clear (Active LOW) Input	1 U.L.
Q_0 to Q_7	Parallel Latch Outputs (Note b)	6 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW
b. 6 U.L. is the output LOW drive factor and 18 U.L. is the output HIGH drive factor.

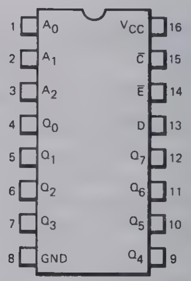
LOGIC SYMBOL



14
13
1
2
3
E
D
A0
A1
A2
9334
C
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
15
4
5
6
7
9
10
11
12

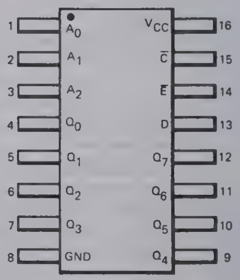
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



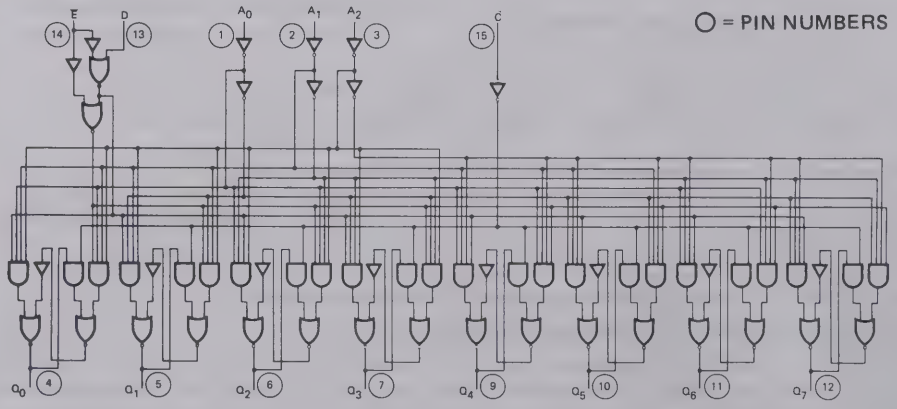
1 A0
2 A1
3 A2
4 Q0
5 Q1
6 Q2
7 Q3
8 GND
16 VCC
15 C̄
14 Ē
13 D
12 Q7
11 Q6
10 Q5
9 Q4

FLATPAK (TOP VIEW)



1 A0
2 A1
3 A2
4 Q0
5 Q1
6 Q2
7 Q3
8 GND
16 VCC
15 C̄
14 Ē
13 D
12 Q7
11 Q6
10 Q5
9 Q4

LOGIC DIAGRAM



○ = PIN NUMBERS
Ē
D
14
13
A0
1
A1
2
A2
3
C̄
15
Q0 4
Q1 5
Q2 6
Q3 7
Q4 9
Q5 10
Q6 11
Q7 12

FUNCTIONAL DESCRIPTION — The TTL/MSI 9334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the 9334 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations of the 9334.

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

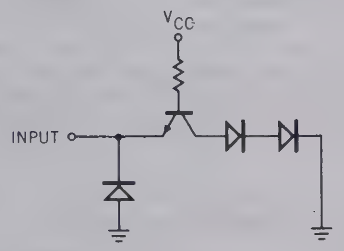
TRUTH TABLE

						PRESENT OUTPUT STATES								
$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
⋮	⋮	⋮		⋮					⋮					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	→	→	→	→	ADDRESSABLE
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}	→	→	→	→	→	LATCH
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}	→	→	→	→	→	
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}	→	→	→	→	→	
⋮	⋮	⋮		⋮				⋮						
H	L	L	H	H	H	Q_{N-1}	→	→	→	→	→	Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}	→	→	→	→	→	Q_{N-1}	H	

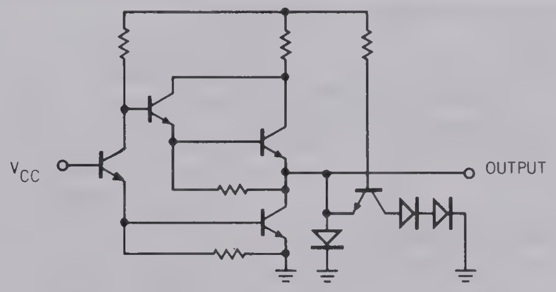
X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{n-1} = Previous Output State

TYPICAL INPUT AND OUTPUT CIRCUITS

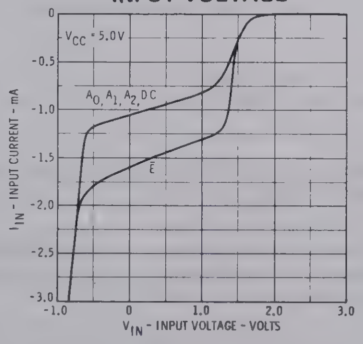
INPUTS EQUIVALENT CIRCUIT



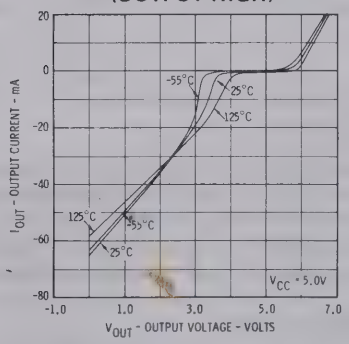
OUTPUTS EQUIVALENT CIRCUIT



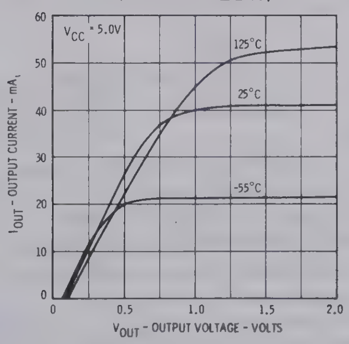
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to + 150°C
Temperature (Ambient) Under Bias	−55°C to + 125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to + 7.0 V
*Input Voltage (dc)	−0.5 V to + 5.5 V
*Input Current (dc)	−30 mA to + 5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to + V_{CC} value
Output Current (dc) (Output LOW)	+ 30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9334XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9334XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −720 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 9.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed Input Logical HIGH Voltage for all Inputs
V_{IL}	Input LOW Level			0.8	Volts	Guaranteed Input Logical LOW Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
I_{IL}	Input LOW Current A_0, A_1, A_2, D, $\overline{C}$ $\overline{E}$		 −0.96 −1.44	 −1.6 −2.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input HIGH Current A_0, A_1, A_2, D, $\overline{C}$ $\overline{E}$		 10 15	 40 60	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 5)	−30	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		56	86	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Turn-Off Delay Enable to Output Turn-On Delay Enable to Output		19 16	23 24	ns ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 1
t_{PLH} t_{PHL}	Turn-Off Delay Data to Output Turn-On Delay Data to Output		28 16	35 24	ns ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 2
t_{PLH} t_{PHL}	Turn-Off Delay Address to Output Turn-On Delay Address to Output			35 35	ns ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 3
t_{PHL}	Turn-On Delay Clear to Output		21	25	ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 5

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

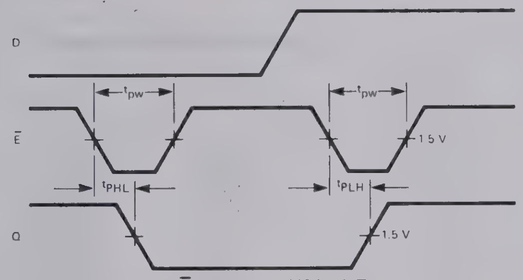
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_s (H) t_h (H)	Set-up Time HIGH Data to Enable Hold Time HIGH Data to Enable	20 0	13 −10		ns ns	V_{CC} = 5.0 V Fig. 4
t_s (L) t_h (L)	Set-up Time LOW Data to Enable Hold Time LOW Data to Enable	17 0	10 −13		ns ns	
t_s (A–$\overline{E}$)	Set-up Time Address to Enable (See Note 6)	5	0		ns	V_{CC} = 5.0 V Fig. 6
t_{pw} ($\overline{E}$)	Enable Pulse Width	17	11		ns	V_{CC} = 5.0 V Fig. 1

NOTES:

(6) The Address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

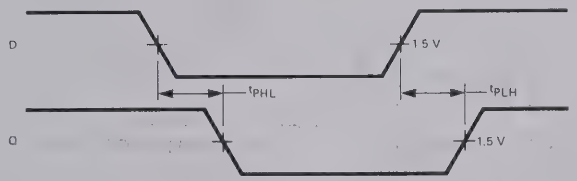
(7) The shaded areas indicate when the inputs are permitted to change for predictable output performance.

Fig. 1 TURN-ON & TURN-OFF DELAYS ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



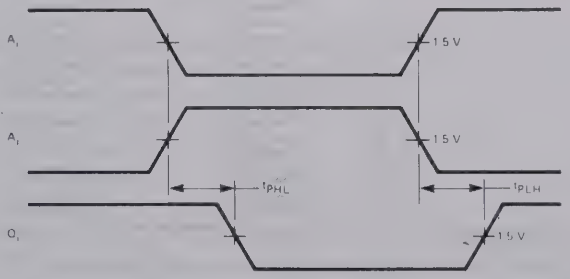
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 2 TURN-ON & TURN-OFF DELAYS DATA TO OUTPUT



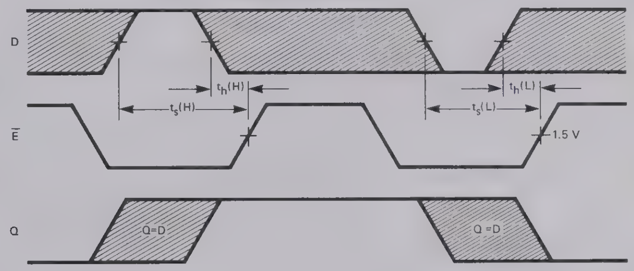
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

Fig. 3 TURN-ON & TURN-OFF DELAYS ADDRESS TO OUTPUT



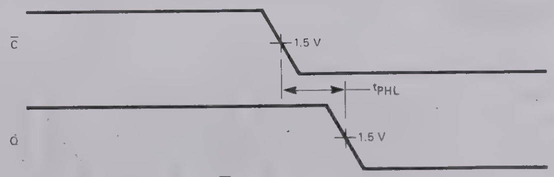
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Fig. 4 SET-UP AND HOLD TIME DATA TO ENABLE



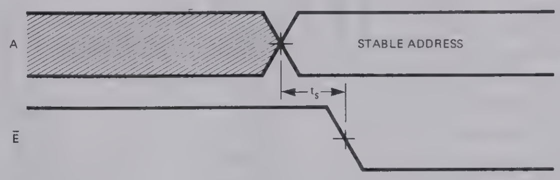
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 5 TURN-ON DELAY CLEAR TO OUTPUT



OTHER CONDITIONS: $\overline{E}$ = H

Fig. 6 SET-UP TIME ADDRESS TO ENABLE (SEE NOTES 6 & 7)



OTHER CONDITIONS: $\overline{C}$ = H

TTL/MSI 9338
8-BIT MULTIPLE PORT REGISTER

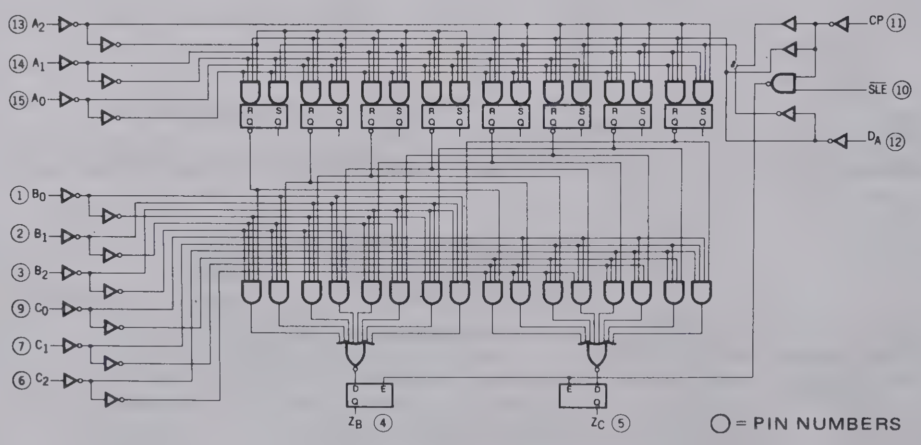
DESCRIPTION — The TTL/MSI 9338 is an 8-Bit Multiple Port Register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously. The circuit uses TTL technology and is compatible with all members of Fairchild's TTL family.

- MASTER/SLAVE OPERATION PERMITTING SIMULTANEOUS WRITE/READ WITHOUT RACE PROBLEMS
- SIMULTANEOUSLY READ TWO BITS AND WRITE ONE BIT IN ANY ONE OF EIGHT BIT POSITIONS
- READILY EXPANDABLE TO ALLOW FOR LARGER WORD SIZES
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16 LEAD DUAL IN-LINE AND FLATPAKS
- TTL COMPATIBLE

PIN NAMES		LOADING (Note a)
A_0, A_1, A_2	Write Address Inputs	2/3 U.L.
D_A	Data Input	2/3 U.L.
B_0, B_1, B_2	B Read Address Inputs	2/3 U.L.
Z_B	B Output (Note b)	10 U.L.
C_0, C_1, C_2	C Read Address Inputs	2/3 U.L.
Z_C	C Output (Note b)	10 U.L.
CP	Clock Pulse Input	2/3 U.L.
$\overline{SLE}$	Slave Enable (Active LOW) Input	2/3 U.L.

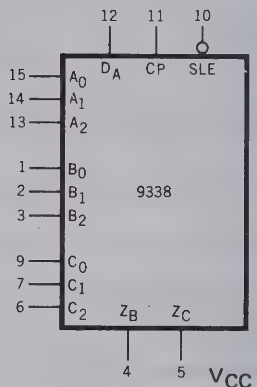
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



⑬ A2
⑭ A1
⑮ A0
① B0
② B1
③ B2
⑨ C0
⑦ C1
⑥ C2
CP ⑪
SLE ⑩
DA ⑫
R S Q Q
D E Q
ZB ④
ZC ⑤
○ = PIN NUMBERS

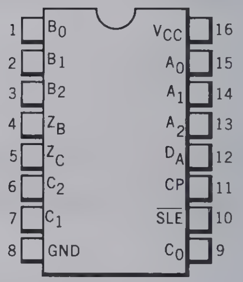
LOGIC SYMBOL



12
11
10
DA
CP
SLE
15 A0
14 A1
13 A2
1 B0
2 B1
3 B2
9338
9 C0
7 C1
6 C2
ZB
ZC
4
5

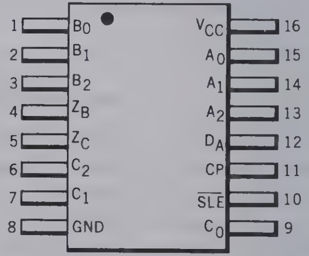
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 B0
2 B1
3 B2
4 ZB
5 ZC
6 C2
7 C1
8 GND
VCC 16
A0 15
A1 14
A2 13
DA 12
CP 11
SLE 10
C0 9

FLATPAK (TOP VIEW)



1 B0
2 B1
3 B2
4 ZB
5 ZC
6 C2
7 C1
8 GND
VCC 16
A0 15
A1 14
A2 13
DA 12
CP 11
SLE 10
C0 9

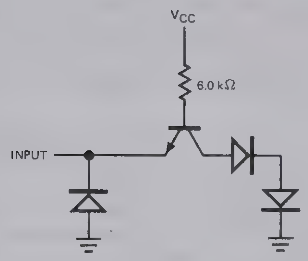
FUNCTIONAL DESCRIPTION – The 9338 8-bit multiple port register may be considered as a 1-bit slice of eight high speed working registers. Data may be written into any one of eight storage locations and read out from any two of the eight storage locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous writing in and reading from the same location.

The timing of this data transfer is similar to that of a standard master/slave flip-flop. While the clock is LOW the slaves are held steady, but the information on the D (data) input is permitted to enter the selected master. The next clock transition from LOW to HIGH locks the masters in their present states making them insensitive to the D input and write address inputs. This rising clock edge also connects each of the two slaves to the selected masters causing their contents to be reflected on the outputs. Outputs change, therefore, following the LOW to HIGH transition of the clock as on almost all Fairchild TTL/MSI devices and TTL flip-flops.

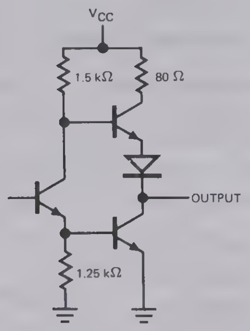
The Slave Enable ($\overline{SLE}$) input may be used to defeat the master/slave operation. If the Slave Enable ($\overline{SLE}$) line is held LOW, the slaves are continuously enabled allowing immediate transfer of information from the selected masters to the outputs.

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE D_A A_2 A_1 A_0 C_2 C_1 C_0 B_2 B_1 B_0 CP

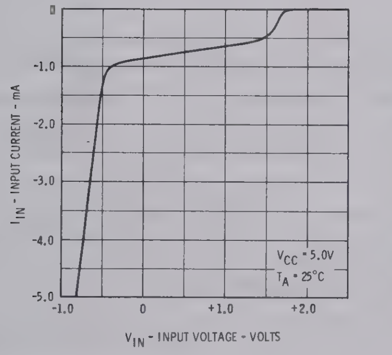


Fig. 1

INPUT CURRENT VERSUS INPUT VOLTAGE $\overline{SLE}$

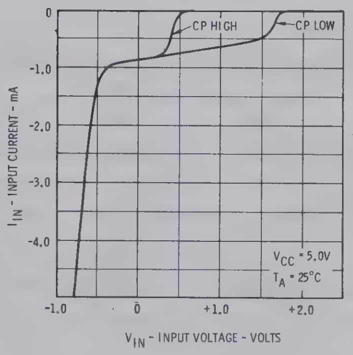


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE Z_B AND Z_C (LOW STATE)

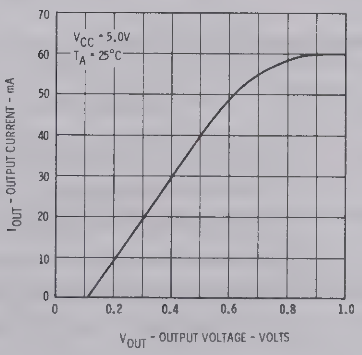


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to $+V_{CC}$
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9338XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C
9338XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			27	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.64	−1.1	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 5)	−10	−50	−70	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		85	135	mA	V_{CC} = MAX.

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
(5) Not more than one output should be shorted at a time.

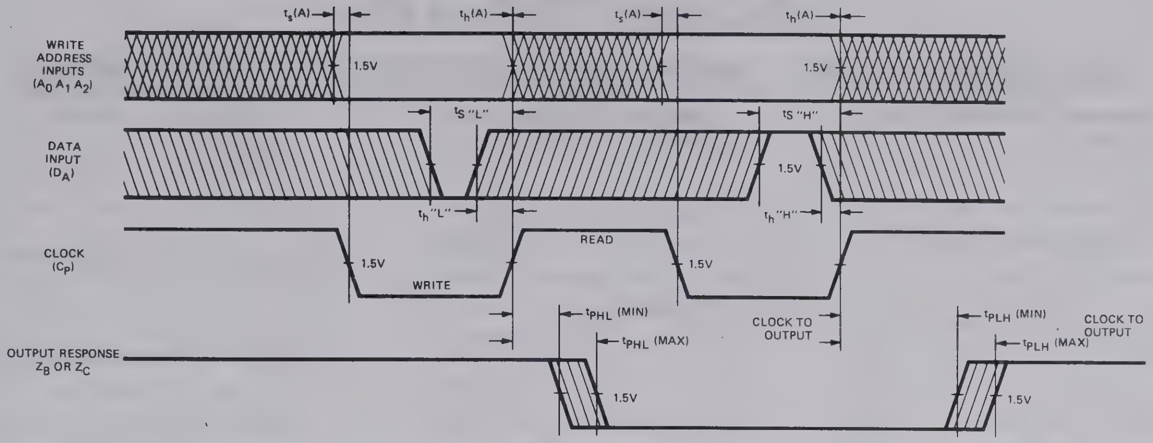
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{PLH}	Turn-Off Delay Address to Output	13	25	40	ns	See Fig. 6	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn-On Delay Address to Output	18	27	35	ns		
t_{PLH}	Turn-Off Delay Data to Output	25	33	45	ns	See Fig. 5	
t_{PHL}	Turn-On Delay Data to Output	25	37	50	ns		
t_{PLH}	Turn-Off Delay Clock to Output	18	26	35	ns	See Fig. 4	
t_{PHL}	Turn-On Delay Clock to Output	13	21	30	ns		

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

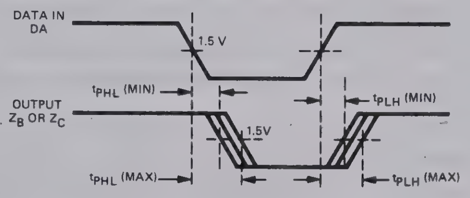
SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_s"H"	Set-up Time HIGH Data to Clock	20	14		ns	See Fig. 4	V_{CC} = 5.0 V
t_h"H"	Hold Time HIGH Data to Clock	0	−7		ns		
t_s"L"	Set-up Time LOW Data to Clock	12	7		ns		
t_h"L"	Hold Time LOW Data to Clock	−8	−14		ns		
t_s(A)	Set-up Time (A) Address to Clock	10	5		ns		
t_h(A)	Hold Time (A) Address to Clock	0			ns		
t_{CP}"L"	Clock LOW Time Required to Write	13	7.0		ns	See Fig. 7	
t_{CP}"H"	Clock HIGH Time Required to Read	23	15		ns	See Fig. 8	

SWITCHING WAVEFORMS


$t_s(A)$
$t_h(A)$
$t_s(A)$
$t_h(A)$
WRITE ADDRESS INPUTS (A_0 A_1 A_2)
1.5V
1.5V
t_S "L"
t_S "H"
DATA INPUT (D_A)
1.5V
t_h "L"
t_h "H"
CLOCK (C_P)
READ
1.5V
WRITE
1.5V
t_{PHL} (MIN)
t_{PHL} (MAX)
CLOCK TO OUTPUT
t_{PLH} (MIN)
t_{PLH} (MAX)
CLOCK TO OUTPUT
OUTPUT RESPONSE Z_B OR Z_C
1.5V
1.5V

The crosshatched areas of the input waveforms indicate when inputs are permitted to change. The crosshatched areas on the output response waveforms indicate minimum and maximum propagation delays.

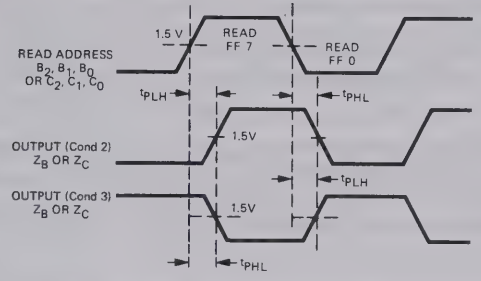
Fig. 4 DATA AND WRITE ADDRESS SETUP TIMES; READ TIME (CLOCK PULSE TO OUTPUT)


DATA IN DA
1.5 V
t_{PHL} (MIN)
t_{PLH} (MIN)
OUTPUT Z_B OR Z_C
1.5V
t_{PHL} (MAX)
t_{PLH} (MAX)

OTHER CONDITIONS

1. CP = LOW
2. $\overline{SLE}$ = LOW
3. $A_2, A_1, A_0 = B_2, B_1, B_0 = C_2, C_1, C_0$

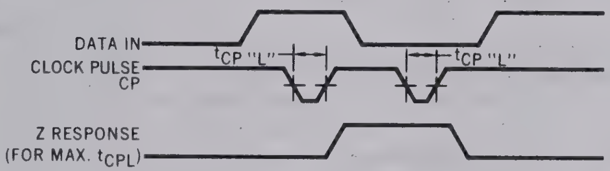
Fig. 5 t_{PLH}/t_{PHL} (DATA INPUT TO OUTPUT)


1.5 V
READ FF 7
READ FF 0
READ ADDRESS B_2, B_1, B_0 OR C_2, C_1, C_0
t_{PLH}
t_{PHL}
1.5V
OUTPUT (Cond 2) Z_B OR Z_C
t_{PLH}
OUTPUT (Cond 3) Z_B OR Z_C
1.5V
t_{PHL}

OTHER CONDITIONS

1. CP = HIGH
2. Master FF 7 = H
3. Master FF 0 = L
   Master FF 7 = L
   Master FF 0 = H

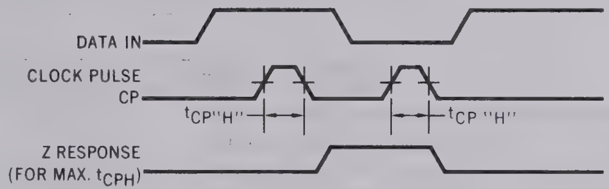
Fig. 6 t_{PLH}/t_{PHL} (READ ADDRESS TO OUTPUT)


DATA IN
CLOCK PULSE CP
t_{CP} "L"
t_{CP} "L"
Z RESPONSE (FOR MAX. t_{CPL})

OTHER CONDITIONS

1. $\overline{SLE}$ = LOW
2. $A_2, A_1, A_0 = B_2, B_1, B_0 = C_2, C_1, C_0$

Fig. 7 t_{CP}"L" (CLOCK LOW TIME REQUIRED TO WRITE)


DATA IN
CLOCK PULSE CP
t_{CP}"H"
t_{CP} "H"
Z RESPONSE (FOR MAX. t_{CPH})

OTHER CONDITIONS

1. $\overline{SLE}$ = HIGH
2. $A_2, A_1, A_0 = B_2, B_1, B_0 = C_0, C_1, C_2$

Fig. 8 t_{CP}"H" (CLOCK HIGH TIME REQUIRED TO READ)

DEFINITION OF TERMS

DATA SET UP TIME (t_s) — Is defined as the time required for a HIGH (t_s "H") or a LOW (t_s "L") logic level to be present at the data input prior to the clock transition from LOW to HIGH, in order for the master to recognize and store the new data.

t_{CP} "L" (CLOCK LOW TIME REQUIRED TO WRITE) — This parameter is defined as the minimum LOW clock pulse width required to write information into the master.

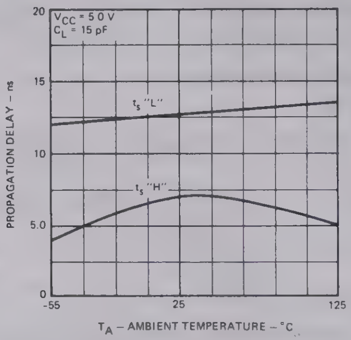
t_{CP} "H" (CLOCK HIGH TIME REQUIRED TO READ) — This parameter is defined as the minimum HIGH clock pulse width required to store information in the slaves.

WRITE ADDRESS SET-UP TIME $t_s(A)$ — Is the time required for the write address to be present before the HIGH to LOW clock transition so that the correct master is addressed and other masters are not disturbed. When writing data into the 9338, the write address inputs should be stable at $t_s(A)$ before the HIGH to LOW transition of the clock and while the clock is LOW but they may change simultaneously with the LOW to HIGH clock transition.

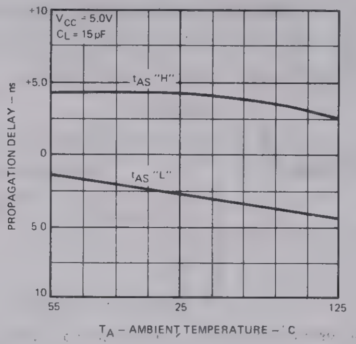
HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

TYPICAL SWITCHING CHARACTERISTICS

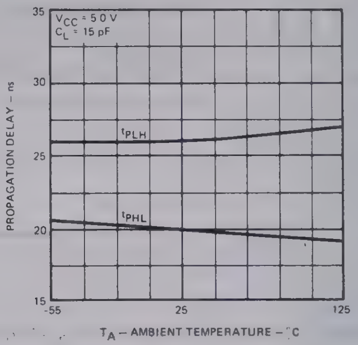
DATA SETUP TIME VERSUS AMBIENT TEMPERATURE



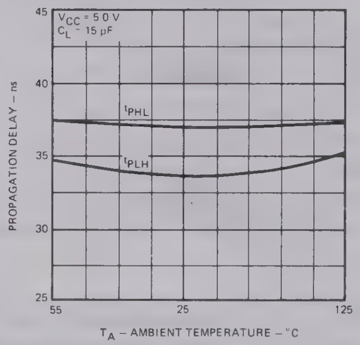
WRITE ADDRESS SETUP TIME VERSUS AMBIENT TEMPERATURE



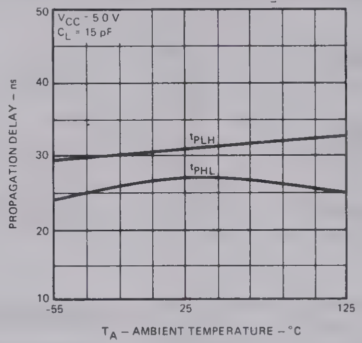
READ TIME VERSUS AMBIENT TEMPERATURE (CLOCK TO OUTPUT)



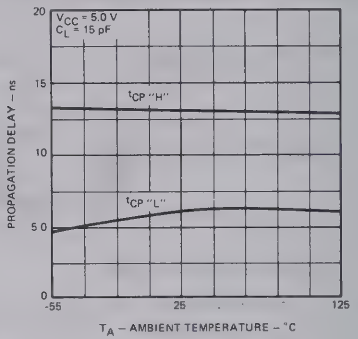
DELAY TIME VERSUS AMBIENT TEMPERATURE (D_A TO Z_B OR Z_C)



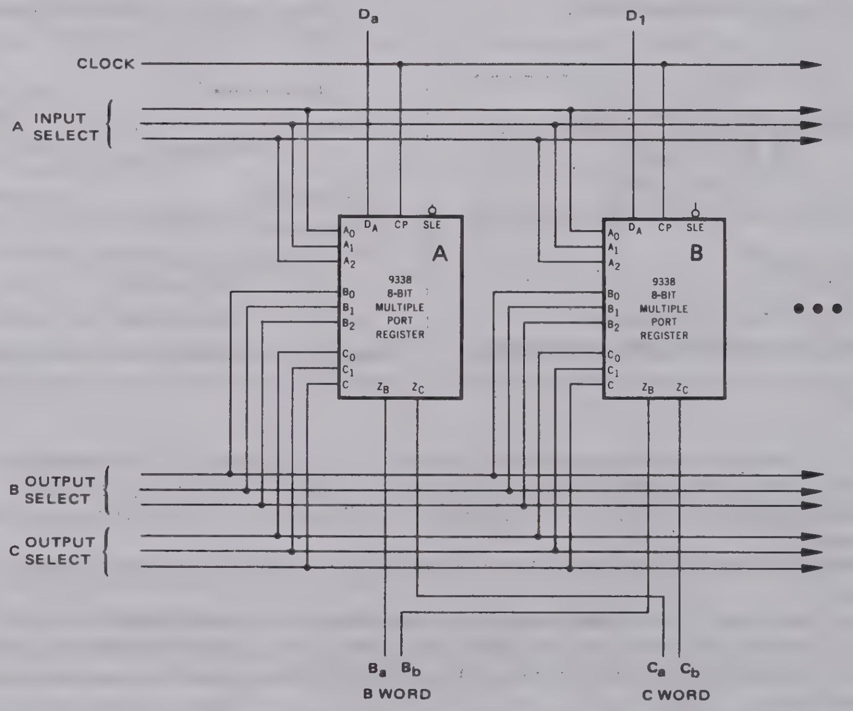
READ TIME VERSUS AMBIENT TEMPERATURE (B OR C TO OUTPUT)



CLOCK TIME REQUIRED TO READ OR WRITE VERSUS AMBIENT TEMPERATURE



APPLICATIONS



Da
D1
CLOCK
A INPUT SELECT
A0
A1
A2
DA
CP
SLE
A
B0
B1
B2
C0
C1
C
ZB
ZC
9338 8-BIT MULTIPLE PORT REGISTER
B
B OUTPUT SELECT
C OUTPUT SELECT
Ba
Bb
B WORD
Ca
Cb
C WORD

Fig. 9 PARALLEL EXPANSION

One 9338 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time as is illustrated above, where n devices are connected in parallel.

TTL/MSI 93S39

8-BIT EDGE TRIGGERED MULTIPLE PORT REGISTER

TO BE ANNOUNCED

DESCRIPTION — The TTL/MSI 93S39 is an 8-bit, edge triggered, multiple port register designed with the super high speed Schottky-barrier diode clamp circuit. It is organized as a 1-bit slice of eight storage registers for use as accumulators, data registers, or scratch pad memory. It is primarily intended to be used with an arithmetic logic unit (ALU) such as the 93S41/74S181 to provide very high speed arithmetic operations.

The 93S39 is essentially an 8-bit register having one input data line and three output ports. Data can be written into any one of eight locations, selected by address lines A_0 thru A_2. Because of the master/slave design, the previous data can be read out of that same location simultaneously on output Z_A. In addition data can be read out from any other location on output Z_B, under control of the second output multiplexer, addressed by B_0 thru B_2. Individual multiplexer enable controls to the Z_A and Z_B outputs allow for easy expansion to more than eight registers. A separate Z_0 output is provided which continuously displays the contents of location 0, which can be used as a P register.

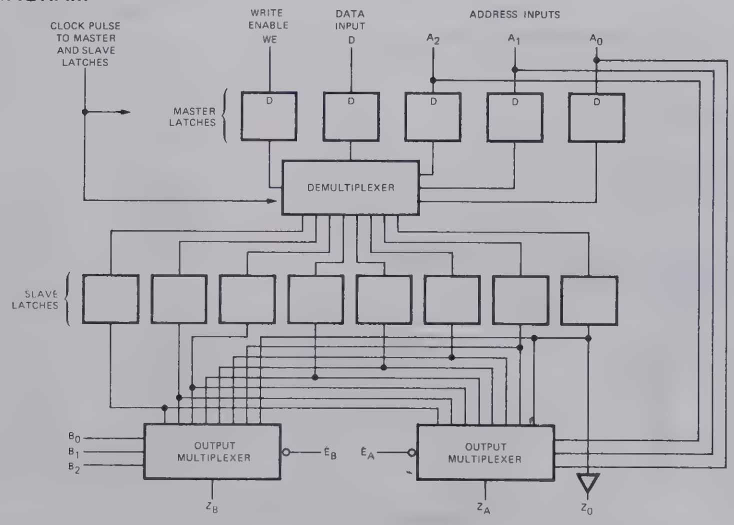
The 93S39 features edge triggered inputs on the write enable, data, and write address lines, which respond only to the LOW to HIGH transition of the clock. This insures the longest possible time for propagation of signals through external combinatorial logic, as the stability of the input address, the new data, and the write enable must be controlled only within the set-up time requirements of the rising edge of the clock. The outputs Z_A and Z_B are asynchronous, depending only on the delay of the multiplexer address and enable controls. The output enables are designed to permit OR-tying the outputs for easy expansion to more than eight registers.

- **THE WRITE CONTROLS (WRITE ENABLE, WRITE ADDRESS, AND DATA) ARE EDGE TRIGGERED—RESPONDING ONLY TO THE POSITIVE TRANSITION OF THE CLOCK PULSE**
- **SCHOTTKY-BARRIER DIODE DESIGN FOR SUPER HIGH SPEED OPERATION**
- **ASYCHRONOUS CONTROL OF OUTPUT DATA MULTIPLEXERS**
- **OUTPUT MULTIPLEXER DESIGN PROVIDES FOR EASY REGISTER EXPANSION**
- **CONTINUOUS OUTPUT FROM BIT LOCATION "000" FOR MEMORY ADDRESS REGISTER APPLICATIONS**

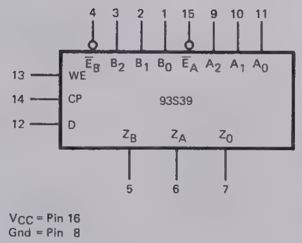
PIN NAMES

A_0, A_1, A_2	Write Address and "A" Multiplexer Address Inputs	WE	Write Enable Input
$\overline{E}_A$	"A" Multiplexer Enable (Active LOW) Input	CP	Clock Pulse (Active HIGH going edge) Input
B_0, B_1, B_2	"B" Multiplexer Address Inputs	Z_0	Output from Bit Location "000"
$\overline{E}_B$	"B" Multiplexer Enable (Active LOW) Input	Z_A	Output from "A" Multiplexer
D	Data Input	Z_B	Output from "B" Multiplexer

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

TTL/MSI 9340

4-BIT ARITHMETIC LOGIC UNIT WITH CARRY LOOKAHEAD

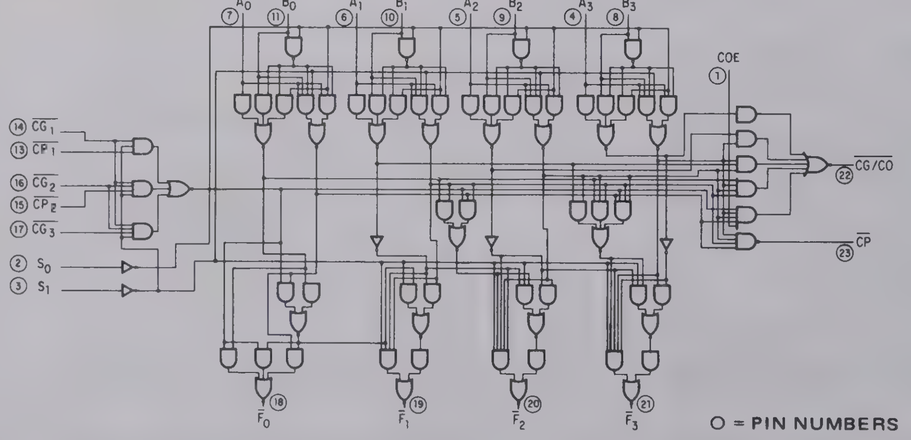
DESCRIPTION — The 9340 is a TTL/MSI high speed Arithmetic Logic Unit with full on chip carry lookahead circuitry. It can perform the arithmetic operations add or subtract in parallel, or either of six logic functions on two 4-bit binary words. The internal carry lookahead provides either a ripple carry output or carry lookahead outputs. An internal carry input network accepts carry lookahead outputs from up to three other packages producing a 16-bit full carry lookahead ALU without additional gates. Ripple carries can be used between additional blocks of 12 bits to further expand the word length. A low power version of the 9340 is available as the 93L40, dissipating only 110 mW.

- **MULTIFUNCTION CAPABILITY**
  Two Arithmetic Operations — Add, Subtract
  Six Logic Functions — A Ex or B, A and B, Plus Four Others
- **ADD TWO 4-BIT WORDS IN 23 ns TYPICAL**
- **SUBTRACT TWO 4-BIT WORDS IN 28 ns**
- **LOOKAHEAD CARRY INPUT AND OUTPUT NETWORKS ON CHIP**
- **EASILY EXPANDABLE TO LONGER WORD LENGTHS**
- **TYPICAL POWER DISSIPATION OF 425 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL COMPATIBLE**

PIN NAMES		**LOADING** (Note a)
$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$	Operand Active LOW Inputs	3 U.L.
S_0, S_1	Mode Select Inputs	1 U.L.
$\overline{CG}_1$	Active LOW Carry Generate Input from immediately preceding stage	3 U.L.
$\overline{CP}_1$	Active LOW Carry Propagate Input from immediately preceding stage	1 U.L.
$\overline{CG}_2$	Active LOW Carry Generate Input from second preceding stage	2 U.L.
$\overline{CP}_2$	Active LOW Carry Propagate Input from second preceding stage	1 U.L.
$\overline{CG}_3$	Active LOW Carry Generate Input from third preceding stage	1 U.L.
COE	Carry Out Enable Input	1.5 U.L.
$\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$	Function (Active LOW) Outputs (Note b)	10 U.L.
$\overline{CO/CG}$	Carry Out/Carry Generate (Active LOW) Output (Note b)	10 U.L.
$\overline{CP}$	Carry Propagate (Active LOW) Output (Note b)	10 U.L.

Notes: a. 1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

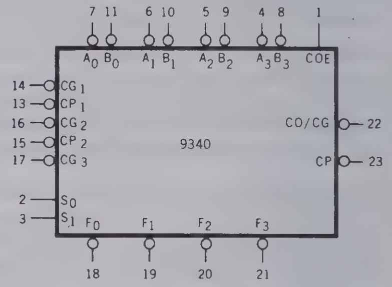
LOGIC DIAGRAM



$\overline{A}_0$ ⑦
$\overline{B}_0$ ⑪
$\overline{A}_1$ ⑥
$\overline{B}_1$ ⑩
$\overline{A}_2$ ⑤
$\overline{B}_2$ ⑨
$\overline{A}_3$ ④
$\overline{B}_3$ ⑧
COE ①
⑭ $\overline{CG}_1$
⑬ $\overline{CP}_1$
⑯ $\overline{CG}_2$
⑮ $\overline{CP}_2$
⑰ $\overline{CG}_3$
② S_0
③ S_1
㉒ $\overline{CG/CO}$
㉓ $\overline{CP}$
⑱ $\overline{F}_0$
⑲ $\overline{F}_1$
⑳ $\overline{F}_2$
㉑ $\overline{F}_3$

O = PIN NUMBERS

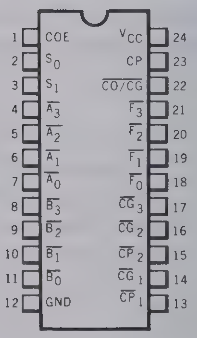
LOGIC SYMBOL



7 11 6 10 5 9 4 8 1
A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3 COE
14 CG 1
13 CP 1
16 CG 2
15 CP 2
17 CG 3
9340
CO/CG 22
CP 23
2 S_0
3 S_1
F_0 F_1 F_2 F_3
18 19 20 21

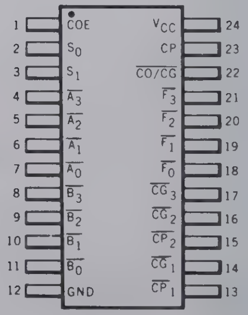
V_{CC} = Pin 24
Gnd = Pin 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 COE
2 S_0
3 S_1
4 $\overline{A}_3$
5 $\overline{A}_2$
6 $\overline{A}_1$
7 $\overline{A}_0$
8 $\overline{B}_3$
9 $\overline{B}_2$
10 $\overline{B}_1$
11 $\overline{B}_0$
12 GND
24 V_{CC}
23 CP
22 $\overline{CO/CG}$
21 $\overline{F}_3$
20 $\overline{F}_2$
19 $\overline{F}_1$
18 $\overline{F}_0$
17 $\overline{CG}_3$
16 $\overline{CG}_2$
15 $\overline{CP}_2$
14 $\overline{CG}_1$
13 $\overline{CP}_1$

FLATPAK (TOP VIEW)



1 COE
2 S_0
3 S_1
4 $\overline{A}_3$
5 $\overline{A}_2$
6 $\overline{A}_1$
7 $\overline{A}_0$
8 $\overline{B}_3$
9 $\overline{B}_2$
10 $\overline{B}_1$
11 $\overline{B}_0$
12 GND
24 V_{CC}
23 CP
22 $\overline{CO/CG}$
21 $\overline{F}_3$
20 $\overline{F}_2$
19 $\overline{F}_1$
18 $\overline{F}_0$
17 $\overline{CG}_3$
16 $\overline{CG}_2$
15 $\overline{CP}_2$
14 $\overline{CG}_1$
13 $\overline{CP}_1$

FUNCTIONAL DESCRIPTION – The 9340 accepts two 4-bit words, A_0, A_1, A_2, A_3 ($A_{0\text{-}3}$) and B_0, B_1, B_2, B_3 ($B_{0\text{-}3}$), and produces a 4-bit output, F_0, F_1, F_2, F_3 ($F_{0\text{-}3}$). The output function is determined by the states on the control lines S_0 and S_1. The inputs and outputs of the 9340 may be considered to be active level LOW or active level HIGH. Logic equivalents for four representations of the 9340 are shown in Figure 1a, b, c, and d.

The add and subtract operations are performed on the entire word, with carries or borrows propagated between bits of different weight. The arithmetic may be performed in 1's complement, 2's complement, or sign-magnitude notation. In the logic modes, carries are inhibited and the device acts like four gates of the type shown in Figure 1.

To achieve high speed operation, the 9340 is designed to be used in a carry lookahead system. Full carry lookahead is used inside the device to propagate carries between bits. Carry lookahead functions over the 4-bit block are available as outputs. These outputs are labeled $\overline{CO/CG}$ (Carry Out/Carry Generate) and $\overline{CP}$ (Carry Propagate) on the logic symbol. The carry in to the device is formed from a set of Carry Generate and Carry Propagate inputs (equation 1) so that three 9340's can be interconnected without any additional gates to form a 12-bit full carry lookahead ALU with a carry in. The pin labeled COE (Carry Out Enable) controls the $\overline{CO/CG}$ output according to equation 2. When COE is HIGH, $\overline{CO/CG}$ becomes a Carry Out which can be used to ripple carries between blocks of 12 bits. The $\overline{CG_1}$ input can be used for a ripple carry input, since this signal is sufficient to produce a carry in.

EQUATION:

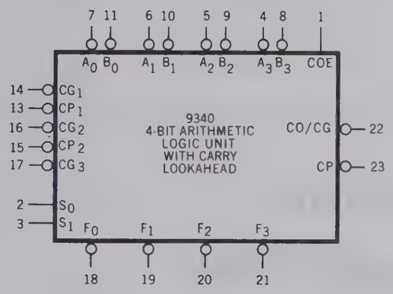
(1) $(\overline{CG_1}) + (\overline{CP_1})\ (\overline{CG_2}) + (\overline{CP_1})\ (\overline{CP_2})\ (\overline{CG_3}) = C_{in}$ (internal)

(2) $\overline{CO/CG} = (\overline{CG}) + (\overline{CP})\ (C_{in})\ (COE)$

Fig. 1—FUNCTION TABLES FOR LOGIC EQUIVALENTS OF THE 9340

Note that when the input operants are defined as active HIGH, the carry lookahead inputs and outputs are not formally carry generate and carry propagate. Consequently, these pins have been relabeled CX and CY in the active HIGH cases. However, the signals are connected in the same manner as $\overline{CG}$ and $\overline{CP}$.

ACTIVE LOW OPERANDS


7 11
6 10
5 9
4 8
1
A0 B0
A1 B1
A2 B2
A3 B3
COE
14 CG1
13 CP1
16 CG2
15 CP2
17 CG3
2 S0
3 S1
9340
4-BIT ARITHMETIC
LOGIC UNIT
WITH CARRY
LOOKAHEAD
CO/CG 22
CP 23
F0 F1 F2 F3
18 19 20 21

V_{CC} = Pin 24
Gnd = Pin 12

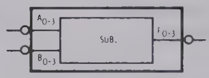
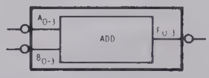
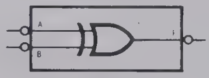
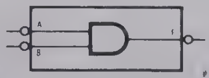
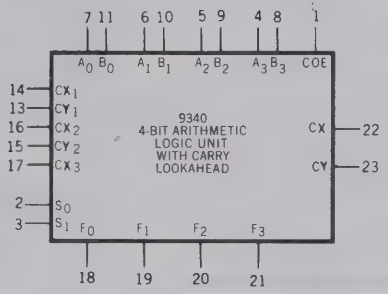
CONTROL INPUTS S_0 S_1	OPERATION	EQUIVALENT LOGIC
L L	A SUBTRACT B	
H L	A ADD B	
L H	A EX OR B	
H H	A AND B	

Fig.1a

ACTIVE HIGH OPERANDS


7 11
6 10
5 9
4 8
1
A0 B0
A1 B1
A2 B2
A3 B3
COE
14 CX1
13 CY1
16 CX2
15 CY2
17 CX3
2 S0
3 S1
9340
4-BIT ARITHMETIC
LOGIC UNIT
WITH CARRY
LOOKAHEAD
CX 22
CY 23
F0 F1 F2 F3
18 19 20 21

V_{CC} = Pin 24
Gnd = Pin 12

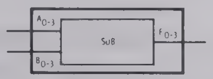
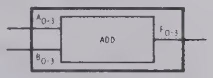
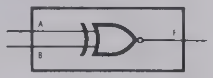
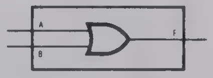
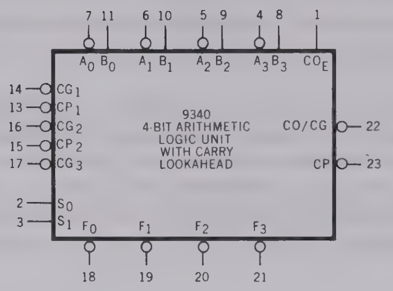
CONTROL INPUTS S_0 S_1	OPERATION	EQUIVALENT LOGIC
L L	A SUBTRACT B	
H L	A ADD B	
L H	A EQUIV B	
H H	A OR B	

Fig.1b

ACTIVE LOW OPERANDS WITH INVERTED B


7 11
6 10
5 9
4 8
1
A0 B0
A1 B1
A2 B2
A3 B3
COE
14 CG1
13 CP1
16 CG2
15 CP2
17 CG3
9340
4-BIT ARITHMETIC
LOGIC UNIT
WITH CARRY
LOOKAHEAD
CO/CG 22
CP 23
2 S0
3 S1
F0
F1
F2
F3
18
19
20
21

V_{CC} = Pin 24
Gnd = Pin 12

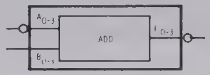
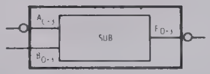
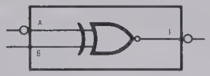
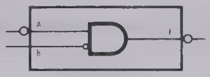
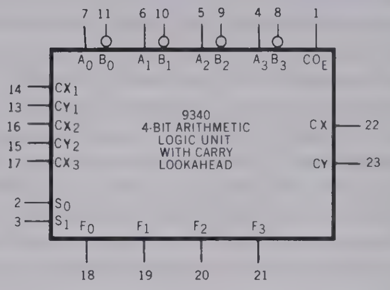
CONTROL INPUTS		OPERATION	EQUIVALENT LOGIC
S_0	S_1		
L	L	A ADD B	 A0-3 B0-3 ADD F0-3
H	L	A SUBTRACT B	 A0-3 B0-3 SUB F0-3
L	H	A EQUIV B	
H	H	A AND $\overline{B}$	

Fig.1c

ACTIVE HIGH OPERANDS WITH INVERTED B


7 11
6 10
5 9
4 8
1
A0 B0
A1 B1
A2 B2
A3 B3
COE
14 CX1
13 CY1
16 CX2
15 CY2
17 CX3
9340
4-BIT ARITHMETIC
LOGIC UNIT
WITH CARRY
LOOKAHEAD
CX 22
CY 23
2 S0
3 S1
F0
F1
F2
F3
18
19
20
21

V_{CC} = Pin 24
Gnd = Pin 12

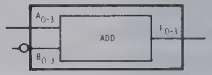
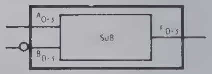
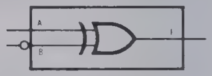
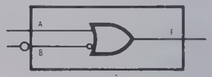
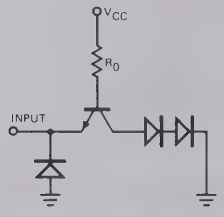
CONTROL INPUTS		OPERATION	EQUIVALENT LOGIC
S_0	S_1		
L	L	A ADD B	 A0-3 B0-3 ADD F0-3
H	L	A SUBTRACT B	 A0-3 B0-3 SUB F0-3
L	H	A EX OR B	
H	H	A OR $\overline{B}$	

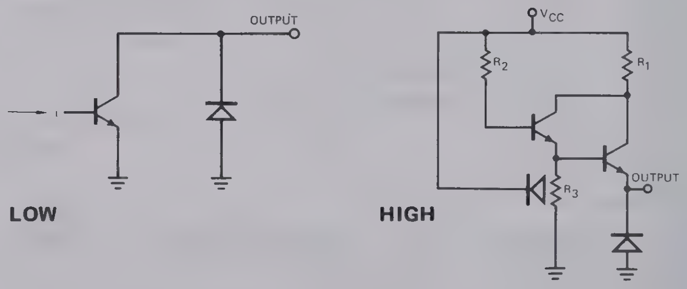
Fig.1d

TYPICAL INPUT AND OUTPUT CIRCUITS

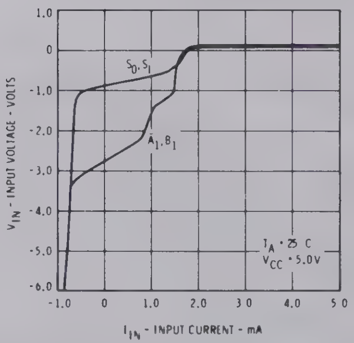
INPUTS EQUIVALENT CIRCUIT


VCC
R0
INPUT

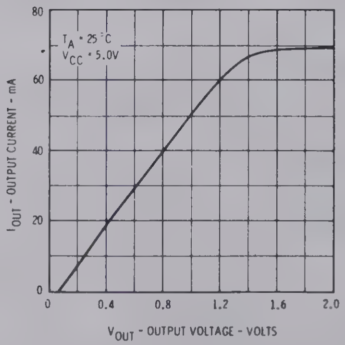
OUTPUTS EQUIVALENT CIRCUITS


OUTPUT
I
LOW
VCC
R2
R1
R3
OUTPUT
HIGH

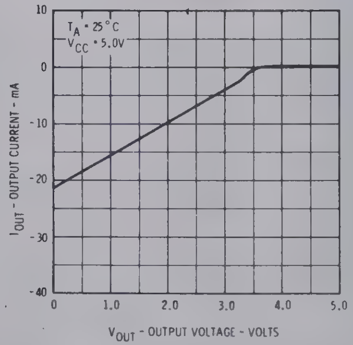
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
9340XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9340XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC}=MIN., I_{IN}=−12 mA, T_A=25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 µA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				µA	V_{CC} = MAX., V_{IN} = 2.4 V
	$S_0, S_1, \overline{CP}_1, \overline{CP}_2, \overline{CG}_3$		10	40		
	COE		15	60		
	$\overline{CG}_2$		20	80		
	$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$, $\overline{CG}_1$		30	120		
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.4 V
	$S_0, S_1, \overline{CP}_1, \overline{CP}_2, \overline{CG}_3$		−0.96	−1.6		
	COE		−1.44	−2.4		
	$\overline{CG}_2$		−1.92	−3.2		
	$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$, $\overline{CG}_1$		−2.88	−4.8		
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−30	−65	−100	mA	V_{CC} = MAX. V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		85	135	mA	9340XM V_{CC} = MAX.
			85	146	mA	9340XC

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS (Add Mode) MIN.	LIMITS (Add Mode) TYP.	LIMITS (Add Mode) MAX.	LIMITS (Subtract Mode) MIN.	LIMITS (Subtract Mode) TYP.	LIMITS (Subtract Mode) MAX.	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Turn off delay Turn on delay } Data Input to Data Output ($\overline{B}_0$ to $\overline{F}_3$)		23 23	30 30		28 25	37 32	ns ns	See Table 1 and Fig. 3	V_{CC} = 5.0V C_L = 15pF
t_{PLH} t_{PHL}	Turn off delay Turn on delay } Data Input to Carry Output ($\overline{B}_0$ to $\overline{CO}/\overline{CG}$)		15 16	20 20		18 17	25 22	ns ns	See Table 1 and Fig. 3	
t_{PLH} t_{PHL}	Turn off delay Turn on delay } Carry Input to Carry Output ($\overline{CG}_3$ to $\overline{CO}/\overline{CG}$)		15 15	19 19		15 15	19 19	ns ns	See Table 1 and Fig. 4	
t_{PLH} t_{PHL}	Turn off delay Turn on delay } Carry Input to Data Output ($\overline{CG}_3$ to $\overline{F}_3$)		23 22	31 29		23 22	31 29	ns ns	See Table 1 and Fig. 4	

TABLE I SWITCHING TEST CONDITIONS

PARAMETER	OPERATION	INPUTS AT 4.5V	INPUTS AT GND	WAVEFORM
t_{PLH} ($\overline{B}_0$ $\overline{F}_3$) t_{PHL} ($\overline{B}_0$ $\overline{F}_3$)	Add	S_0, $\overline{CG}_1$, $\overline{CP}_1$, $\overline{B}_1$, $\overline{B}_2$	S_1, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$, $\overline{B}_3$	1
t_{PLH} ($\overline{B}_0$ $\overline{F}_3$) t_{PHL} ($\overline{B}_0$ $\overline{F}_3$)	Subtract	$\overline{CG}_1$, $\overline{CP}_1$, $\overline{B}_3$	S_0, S_1, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, A_3 $\overline{B}_1$, $\overline{B}_2$	2
t_{PLH} ($\overline{B}_0$ $\overline{CO}/\overline{CG}$) t_{PHL} ($\overline{B}_0$ $\overline{CO}/\overline{CG}$)	Add	S_0, $\overline{CG}_1$, $\overline{CP}_1$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$	S_1, COE, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$	1
t_{PLH} ($\overline{B}_0$ $\overline{CO}/\overline{CG}$) t_{PHL} ($\overline{B}_0$ $\overline{CO}/\overline{CG}$)	Subtract	$\overline{CG}_1$, $\overline{CP}_1$	S_0, S_1, COE, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$ $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$	2
t_{PLH} ($\overline{CG}_3$ $\overline{CO}/\overline{CG}$) t_{PHL} ($\overline{CG}_3$ $\overline{CO}/\overline{CG}$)	Add	S_0, $\overline{CG}_1$, $\overline{CG}_2$, COE, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$	S_1, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$ $\overline{CP}_1$, $\overline{CP}_2$	1
t_{PLH} ($\overline{CG}_3$ $\overline{F}_3$) t_{PHL} ($\overline{CG}_3$ $\overline{F}_3$)	Add	S_0, $\overline{CG}_1$, $\overline{CG}_2$, $\overline{B}_3$ $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$	S_1, B_0, B_1, B_2 $\overline{CP}_1$, $\overline{CP}_2$	1

SWITCHING WAVEFORMS

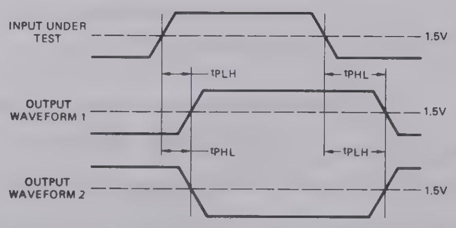


Fig. 2

TYPICAL PROPAGATION DELAYS DATA INPUT TO DATA OUTPUT AND DATA INPUT TO CARRY OUTPUT (ADD MODE)

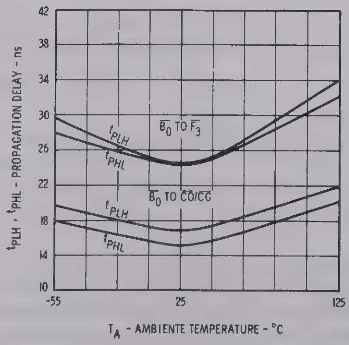


Fig. 3

TYPICAL PROPAGATION DELAYS CARRY INPUT TO CARRY OUTPUT AND CARRY INPUT TO DATA OUTPUT (ADD MODE)

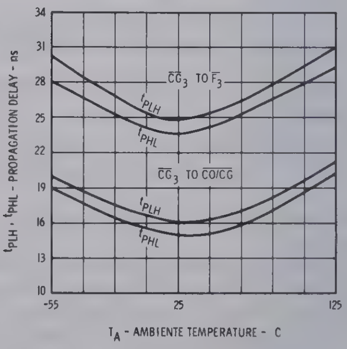


Fig. 4

TTL/MSI 9341/54181, 74181
4-BIT ARITHMETIC LOGIC UNIT

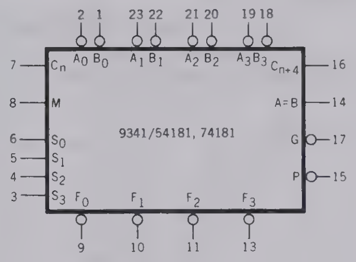
DESCRIPTION — The TTL/MSI 9341/54181, 74181 is a 4-bit high speed Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The ALU is fully compatible with all members of the Fairchild TTL family.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE,
  PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE–OR, COMPARE, AND, NAND, OR, NOR, PLUS
  TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS**
- **INPUT CLAMP DIODES**
- **TTL COMPATIBLE**

PIN NAMES		**LOADING** (Note a)
$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$	Operand (Active LOW) Inputs	3 U.L.
S_0, S_1, S_2, S_3	Function - Select Inputs	4 U.L.
M	Mode Control Input	1 U.L.
C_n	Carry Input	5 U.L.
$\overline{F}_0, \overline{F}_1, \overline{F}_2, \overline{F}_3$	Function (Active LOW) Outputs (Note b)	10 U.L.
A = B	Comparator Output	Open Collector
$\overline{G}$	Carry Generate (Active LOW) Output (Note b)	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output (Note b)	10 U.L.
C_{n+4}	Carry Output (Note b)	10 U.L.

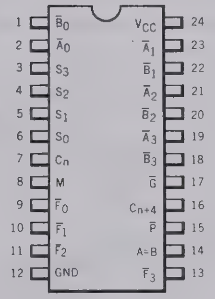
NOTES:
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC SYMBOL

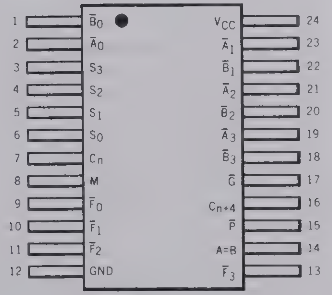

2 1 23 22 21 20 19 18
A0 B0 A1 B1 A2 B2 A3 B3
7 Cn
Cn+4 16
8 M
A=B 14
6 S0
5 S1
4 S2
3 S3
9341/54181, 74181
G 17
P 15
F0 F1 F2 F3
9 10 11 13

V_{CC} = Pin 24
GND = Pin 12

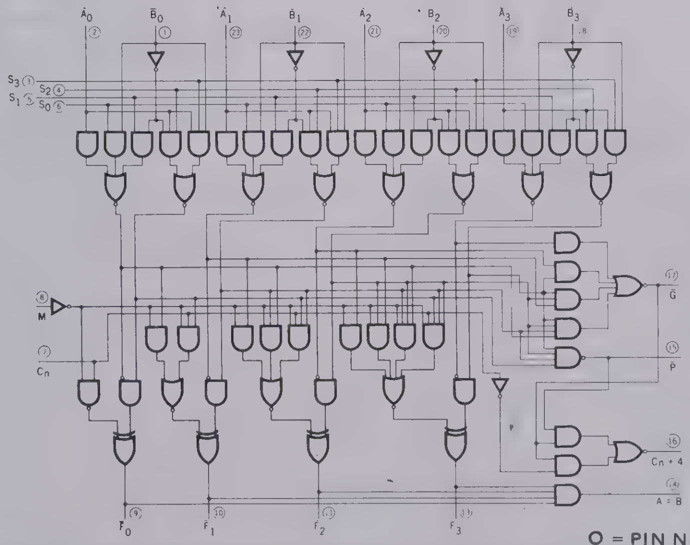
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 B̄0
2 Ā0
3 S3
4 S2
5 S1
6 S0
7 Cn
8 M
9 F̄0
10 F̄1
11 F̄2
12 GND
24 VCC
23 Ā1
22 B̄1
21 Ā2
20 B̄2
19 Ā3
18 B̄3
17 Ḡ
16 Cn+4
15 P̄
14 A=B
13 F̄3

FLATPAK (TOP VIEW)


1 B̄0
2 Ā0
3 S3
4 S2
5 S1
6 S0
7 Cn
8 M
9 F̄0
10 F̄1
11 F̄2
12 GND
24 VCC
23 Ā1
22 B̄1
21 Ā2
20 B̄2
19 Ā3
18 B̄3
17 Ḡ
16 Cn+4
15 P̄
14 A=B
13 F̄3

LOGIC DIAGRAM


Ā0 2
B̄0 1
Ā1 23
B̄1 22
Ā2 21
B̄2 20
Ā3 19
B̄3 18
S3 3
S2 4
S1 5
S0 6
M 8
Cn 7
17 Ḡ
15 P̄
16 Cn + 4
14 A = B
9 F0
10 F1
11 F2
13 F3

O = PIN NUMBERS

FUNCTIONAL DESCRIPTION – The TTL/MSI 9341/54181, 74181 is a 4-bit, high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs Logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs Arithmetic operations on the two, 4-bit words. The device incorporates full internal look-ahead carry and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals P (carry propagate) and G (carry generate). P and G are not affected by carry in. When speed requirements are not stringent, the 9341/54181, 74181 can be used in a simple ripple carry mode by connecting the carry out (C_{n+4}) signal to the carry input (C_n) of the next unit. For high speed operation the 9341/54181, 74181 is used in conjunction with the 9342/54182, 74182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 9341/54181, 74181 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the 9341/54181, 74181 goes HIGH when all four F outputs are HIGH and can be used to indicate logic equivalence over 4-bits when the unit is in the subtract mode. The A = B output is open collector and can be wire ANDed with other A = B outputs to give a comparison for more than 4-bits. The A = B signal can also be used with the carry out signal to indicate A > B and A < B.

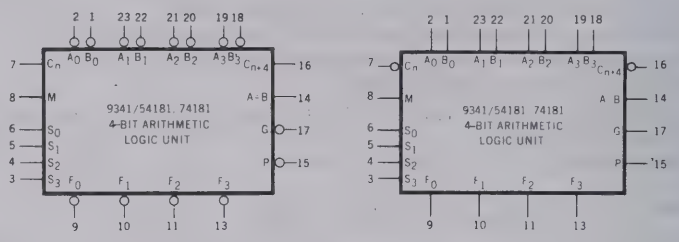
The Function Table lists the Arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus Select Code LHHL generates A minus B minus 1 (2's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1's complement), a CARRY OUT means BORROW; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated the 9341/54181, 74181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3 S_2 S_1 S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L L H L	$\overline{A + B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{R}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A + B}$	A plus $(A + \overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	$(A + B)$ plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L H H H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H L L L	$\overline{A}B$	A plus $(A + B)$	$\overline{A} + B$	A plus AB
H L L H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	$A\overline{B}$ plus $(A + B)$	B	$(A + \overline{B})$ plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	$A + \overline{B}$	$(A + B)$ plus A
H H H L	AB	$A\overline{B}$ plus A	A + B	$(A + \overline{B})$ plus A
H H H H	A	A	A	A minus 1

LOGIC SYMBOLS



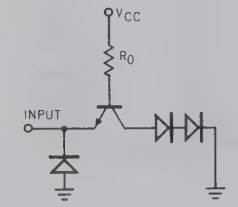
H = High Voltage Level
L = Low Voltage Level

V_{CC} = Pin 24
GND = Pin 12

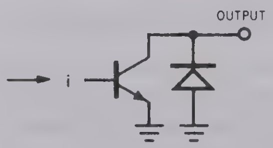
*Each bit is shifted to the next more significant position
**Arithmetic operations expressed in 2's complement notation

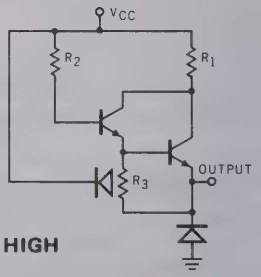
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUITS





INPUT CURRENT VERSUS INPUT VOLTAGE

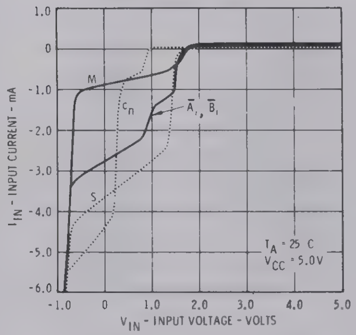


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

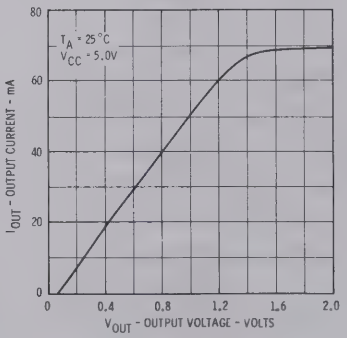


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE

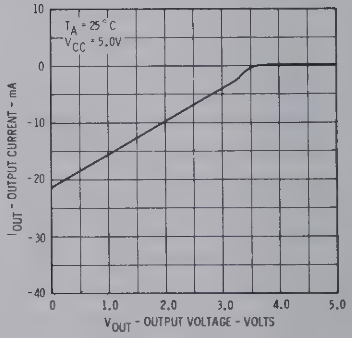


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9341XM/54181XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9341XC/74181XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS		UNITS	CONDITIONS	
		MIN.	MAX.			
V_{IH}	Input HIGH Voltage	2.0		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		0.8	V	Guaranteed Input LOW Voltage for all Inputs	
V_{CD}	Input Clamp Diode Voltage		−1.5	V	V_{CC} = MIN., $I_{IN} = -12$ mA, T_A = 25°C	
I_{CEX}	A = B Output Leakage Current (Open Collector)		250	µA	V_{CC} = MIN., V_{OUT} = 5.5 V	
V_{OH}	Output HIGH Voltage	2.4		V	V_{CC} = MIN., $I_{OH} = -800$ µA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.4	V	V_{CC} = MIN., I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
I_{IH}	Input HIGH Current			µA	V_{CC} = MAX., V_{IN} = 2.4 V	
	M		40			
	$\overline{A}_0\ \overline{A}_1\ \overline{A}_2\ \overline{A}_3\ \overline{B}_0\ \overline{B}_1\ \overline{B}_2\ \overline{B}_3$		120			
	$S_0\ S_1\ S_2\ S_3$		160			
	C_n		200			
	Input HIGH Current All Inputs		1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			mA	V_{CC} = MAX., V_{IN} = 0.4 V	
	M		−1.6			
	$\overline{A}_0\ \overline{A}_1\ \overline{A}_2\ \overline{A}_3\ \overline{B}_0\ \overline{B}_1\ \overline{B}_2\ \overline{B}_3$		−4.8			
	$S_0\ S_1\ S_2\ S_3$		−6.4			
	C_n		−8.0			
I_{SC} (I_{OS})	Output Short Circuit Current (Note 4)	−20	−55	mA	XM	V_{CC} = MAX., V_{OUT} = 0.0 V
		−18	−57	mA	XC	
I_{CC}	Power Supply Current		127	mA	XM	V_{CC} = MAX. C_n = $B_0 = B_1 = B_2 = B_3$ = GND All Other Inputs = 4.5 V
			140	mA	XC	
			135	mA	XM	V_{CC} = MAX. M = $S_0 = S_1 = S_2 = S_3$ = 4.5 V All Other Inputs = GND
			150	mA	XC	

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, Pin 12 = GND)

SYMBOL	PARAMETER	LIMITS		UNITS	CONDITIONS
		TYP.	MAX.		
t_{PLH} t_{PHL}	(C_n to $C_n + 4$)	12 13	16 17	ns	M = OV, (Sum or Diff Mode) See Fig. 4 and Tables I & II
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ outputs)	15 14	17 17	ns	M = OV, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	16 9	19 12	ns	M = $S_1 = S_2$ = OV, $S_0 = S_3$ = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	18 13	22 17	ns	M = $S_0 = S_3$ = OV, $S_1 = S_2$ = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	16 11	19 15	ns	M = $S_1 = S_2$ = OV, $S_0 = S_3$ = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	17 14	21 21	ns	M = $S_0 = S_3$ = OV, $S_1 = S_2$ = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs)	19 19	26 26	ns	M = $S_1 = S_2$ = OV, $S_0 = S_3$ = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs)	20 26	26 32	ns	M = $S_0 = S_3$ = OV, $S_1 = S_2$ = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_{i+1}$ outputs)	23 19	29 25	ns	M = OV, $S_0 = S_3$ = 4.5 V, $S_1 = S_2$ = OV (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_{i+1}$ outputs)	23 24	29 30	ns	M = OV, $S_0 = S_3$ = OV, $S_1 = S_2$ = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{F}$ outputs)	18 19	24 24	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output)	16 26	21 30	ns	M = OV, $S_0 = S_3$ = 4.5 V, $S_1 = S_2$ = OV (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output)	19 26	25 30	ns	M = OV, $S_0 = S_3$ = OV, $S_1 = S_2$ = 4.5 V (Diff Mode)
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to A = B output)	33 34	40 42	ns	M = $S_0 = S_3$ = OV, $S_1 = S_2$ = 4.5 V, R_o = 400 Ω to 5.0 V (Diff Mode) See Fig. 5 and Table II

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Note more than one output should be shorted at a time.

SWITCHING TIME WAVEFORMS

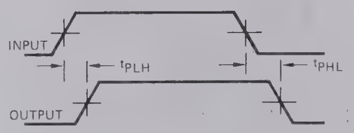


Fig. 4

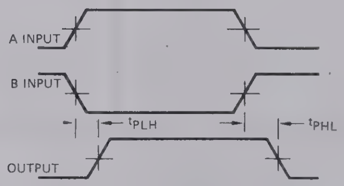


Fig. 5

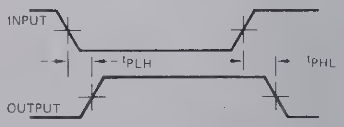


Fig. 6

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or $C_n + 4$

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 0$ V

TTL/MSI 93S41

4-BIT ARITHMETIC LOGIC UNIT

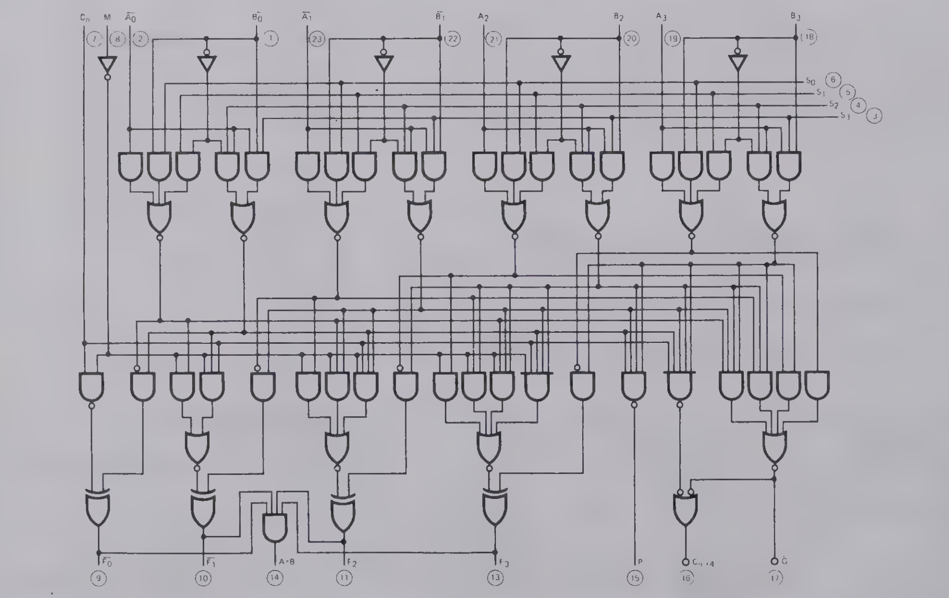
DESCRIPTION — The TTL/MSI 93S41 is a 4-bit high speed Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The ALU is fully compatible with all members of the Fairchild TTL family and incorporates the Schottky TTL process to achieve super high speeds.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS
  TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE–OR, COMPARE, AND, NAND, OR, NOR, PLUS
  TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS**
- **INPUT CLAMP DIODES**
- **TYPICAL ADD TIME FOR 16-BITS IS 19ns**
- **TYPICAL POWER DISSIPATION OF 500mW**

PIN NAMES

$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$	Operand (Active LOW) Inputs
S_0, S_1, S_2, S_3	Function — Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}_0, \overline{F}_1, \overline{F}_2, \overline{F}_3$	Function (Active LOW) Outputs
A = B	Comparator Output
$\overline{G}$	Carry Generate (Active LOW) Output
$\overline{P}$	Carry Propagate (Active LOW) Output
$C_n + 4$	Carry Output

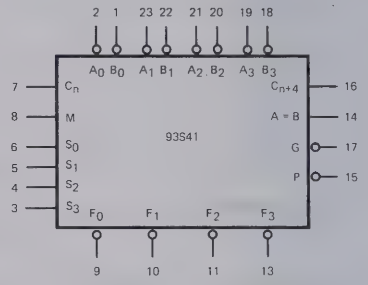
LOGIC DIAGRAM



Cn
M
Ā0
B̄0
Ā1
B̄1
A2
B2
A3
B3
7
8
2
1
23
22
21
20
19
18
S0 6
S1 5
S2 4
S3 3
F̄0
F̄1
A=B
F̄2
F̄3
P
Cn+4
G
9
10
14
11
13
15
16
17

○ = Pin Numbers

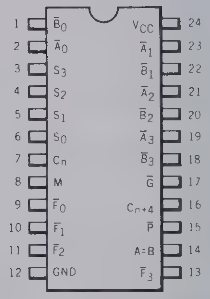
LOGIC SYMBOL



2
1
23
22
21
20
19
18
A0
B0
A1
B1
A2
B2
A3
B3
7
Cn
8
M
6
S0
5
S1
4
S2
3
S3
93S41
Cn+4
16
A = B
14
G
17
P
15
F0
F1
F2
F3
9
10
11
13

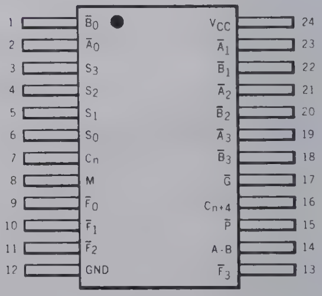
V_{CC} = PIN 24
GND = PIN 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 B̄0
2 Ā0
3 S3
4 S2
5 S1
6 S0
7 Cn
8 M
9 F̄0
10 F̄1
11 F̄2
12 GND
24 VCC
23 Ā1
22 B̄1
21 Ā2
20 B̄2
19 Ā3
18 B̄3
17 Ḡ
16 Cn+4
15 P̄
14 A=B
13 F̄3

FLATPAK (TOP VIEW)



1 B̄0
2 Ā0
3 S3
4 S2
5 S1
6 S0
7 Cn
8 M
9 F̄0
10 F̄1
11 F̄2
12 GND
24 VCC
23 Ā1
22 B̄1
21 Ā2
20 B̄2
19 Ā3
18 B̄3
17 Ḡ
16 Cn+4
15 P̄
14 A-B
13 F̄3

FUNCTIONAL DESCRIPTION – The TTL/MSI 93S41 is a 4-bit super high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs Logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs Arithmetic operations on the two, 4-bit words. The device incorporates full internal look-ahead carry and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals P (carry propagate) and G (carry generate). P and G are not affected by carry in. When speed requirements are not stringent, the 93S41 can be used in a simple ripple carry mode by connecting the carry out (C_{n+4}) signal to the carry input (C_n) of the next unit. For high speed operation the 93S41 is used in conjunction with the 93S42 carry look-ahead circuit. One carry look-ahead package is required for each group of four 93S41 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the 93S41 goes HIGH when all four F outputs are HIGH and can be used to indicate logic equivalence over 4-bits when the unit is in the subtract mode. The A = B output is open collector and can be wire ANDed with other A = B outputs to give a comparison for more than 4-bits. The A = B signal can also be used with the carry out signal to indicate A > B and A < B.

The Function Table lists the Arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus Select Code LHHL generates A minus B minus 1 (2's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1's complement), a CARRY OUT means BORROW; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

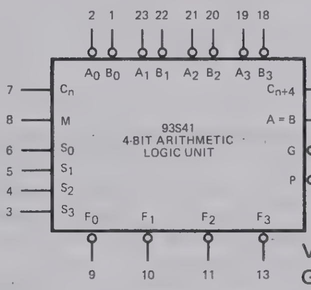
As indicated the 93S41 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3 S_2 S_1 S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L L H L	$\overline{A + B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{B}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A + B}$	A plus $(A + \overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	(A + B) plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L H H H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	AB minus 1
H L L L	$\overline{A}B$	A plus (A + B)	$\overline{A} + B$	A plus AB
H L L H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	$A\overline{B}$ plus (A + B)	B	$(A + \overline{B})$ plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	$A + \overline{B}$	(A + B) plus A
H H H L	AB	$A\overline{B}$ plus A	A + B	$(A + \overline{B})$ plus A
H H H H	A	A	A	A minus 1

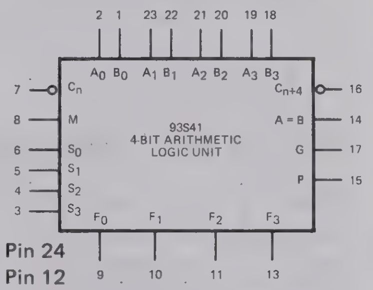
LOGIC SYMBOLS

ACTIVE LOW OPERANDS



V_{CC} = Pin 24
GND = Pin 12

ACTIVE HIGH OPERANDS



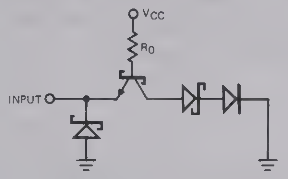
L = LOW Voltage Level H = HIGH Voltage Level

*Each bit is shifted to the next more significant position

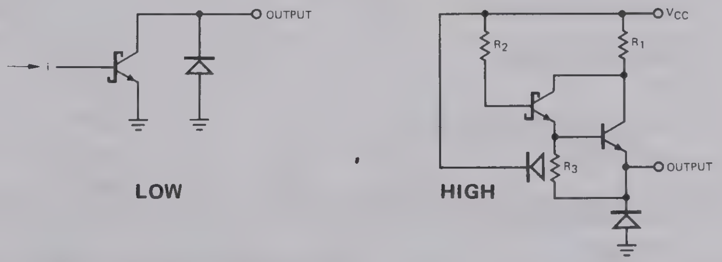
**Arithmetic operations expressed in 2's complement notation

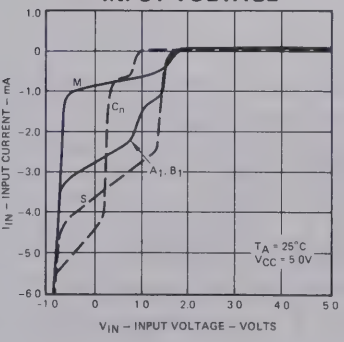
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT



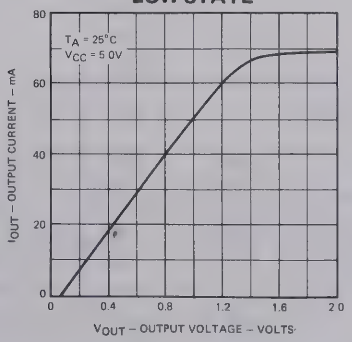
OUTPUTS EQUIVALENT CIRCUITS





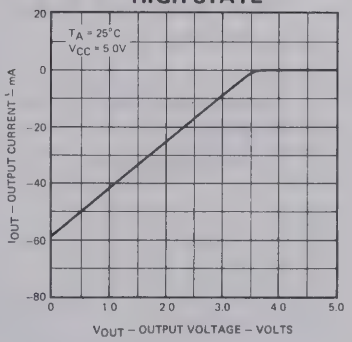
INPUT CURRENT VERSUS INPUT VOLTAGE

Fig. 1



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

Fig. 2



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE

Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93S41XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93S41XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage for all Inputs	
V_{CD}	Input Clamp Diode Voltage			−1.2	Volts	V_{CC} = MIN., I_{IN} = −18 mA, T_A = 25°C	
I_{CEX}	A = B Output Leakage Current (Open Collector)			250	μA	V_{CC} = MIN., V_{OUT} = 5.5 V	
V_{OH}	Output HIGH Voltage	2.5			Volts	XM	V_{CC} = MIN., I_{OH} = −1.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
		2.7				XC	
V_{OL}	Output LOW Voltage			0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA V_{IN} = V_{IH} or V_{IL} per Truth Table	
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.7 V	
	M			50			
	$\bar{A}_0$ $\bar{A}_1$ $\bar{A}_2$ $\bar{A}_3$ $\bar{B}_0$ $\bar{B}_1$ $\bar{B}_2$ $\bar{B}_3$			150			
	S_0 S_1 S_2 S_3			200			
	C_n			300			
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.4 V	
	M			−1.6			
	$\bar{A}_0$ $\bar{A}_1$ $\bar{A}_2$ $\bar{A}_3$ $\bar{B}_0$ $\bar{B}_1$ $\bar{B}_2$ $\bar{B}_3$			−4.8			
	S_0 S_1 S_2 S_3			−6.4			
	C_n			−9.6			
I_{SC} (I_{OS})	Output Short Circuit Current (Note 4)	−40		−100	mA	V_{CC} = MAX., V_{OUT} = 0 V	
I_{CC}	Power Supply Current		95	125	mA	XM	V_{CC} = MAX., C_n = B_0=B_1=B_2=B_3=GND All Other Inputs = 4.5 V
			95	140	mA	XC	
			105	135	mA	XM	V_{CC} = MAX., M = S_0=S_1=S_2=S_3=4.5 V All Other Inputs = GND
			105	150	mA	XC	

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, Pin 12 = GND)

SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH} t_{PHL}	(C_n to C_{n+4})	7.0 7.0	12 12	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I & II
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ outputs)	7.0 7.0	12 12	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	9.5 7.0	14 14	ns	$M = S_1 = S_2 = 0$ V, $S_0 = S_3 = 4.5$ V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	9.5 9.0	15 15	ns	$M = S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	8.5 8.0	14 14	ns	$M = S_1 = S_2 = 0$ V, $S_0 = S_3 = 4.5$ V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	8.5 10	15 15	ns	$M = S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to any $\overline{F}$ output)	15 9.0	20 20	ns	$M = S_1 = S_2 = 0$ V, $S_0 = S_3 = 4.5$ V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to any $\overline{F}$ output)	14 11	21 21	ns	$M = S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{F}$ outputs)	10 10	20 20	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output)	10 13	18.5 18.5	ns	M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output)	12 13	23 23	ns	M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (Diff Mode)
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to A = B output)	13	23	ns	$M = S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V, $R_o = 400\ \Omega$ to 5.0 V
t_{PHL}		13	23		(Diff Mode) See Fig. 5 and Table II

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Not more than one output should be shorted at a time.

SWITCHING TIME WAVEFORMS

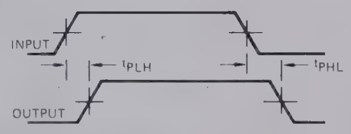


Fig. 4

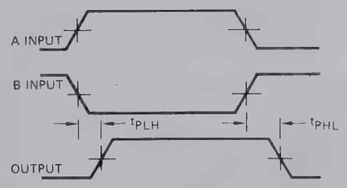


Fig. 5

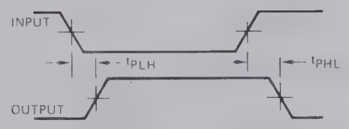


Fig. 6

SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 0$ V

TTL/MSI 9342/54182, 74182
LOOKAHEAD CARRY GENERATOR

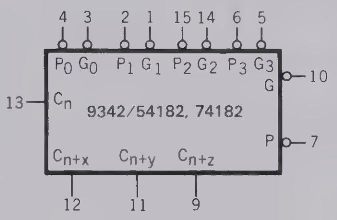
DESCRIPTION – The TTL/MSI 9342/54182, 74182 is a high speed Lookahead Carry Generator. It is generally used with the 9341/54181, 74181 4-Bit Arithmetic Logic Unit to provide high speed lookahead over word lengths of more than four bits. The lookahead carry generator is fully compatible with all members of the Fairchild TTL Family.

- **PROVIDES LOOKAHEAD CARRIES ACROSS A GROUP OF FOUR ALU'S**
- **MULTI-LEVEL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**
- **INPUT CLAMP DIODES**
- **TTL COMPATIBLE**

PIN NAMES		**LOADING** (Note a)
C_n	Carry Input	1 U.L.
$\overline{G}_0, \overline{G}_2$	Carry Generate (Active LOW) Inputs	7 U.L.
$\overline{G}_1$	Carry Generate (Active LOW) Input	8 U.L.
$\overline{G}_3$	Carry Generate (Active LOW) Input	4 U.L.
$\overline{P}_0, \overline{P}_1$	Carry Propagate (Active LOW) Inputs	4 U.L.
$\overline{P}_2$	Carry Propagate (Active LOW) Input	3 U.L.
$\overline{P}_3$	Carry Propagate (Active LOW) Input	2 U.L.
$C_{n+x}, C_{n+y}, C_{n+z}$	Carry Outputs (Note b)	10 U.L.
$\overline{G}$	Carry Generate (Active LOW) Output (Note b)	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output (Note b)	10 U.L.

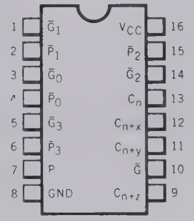
Notes:
(a) 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
(b) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC SYMBOL

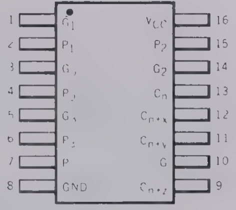

4 3 2 1 15 14 6 5
P0 G0 P1 G1 P2 G2 P3 G3
G 10
13 Cn
9342/54182, 74182
P 7
Cn+x Cn+y Cn+z
12 11 9

V_{CC} = Pin 16
GND = Pin 8

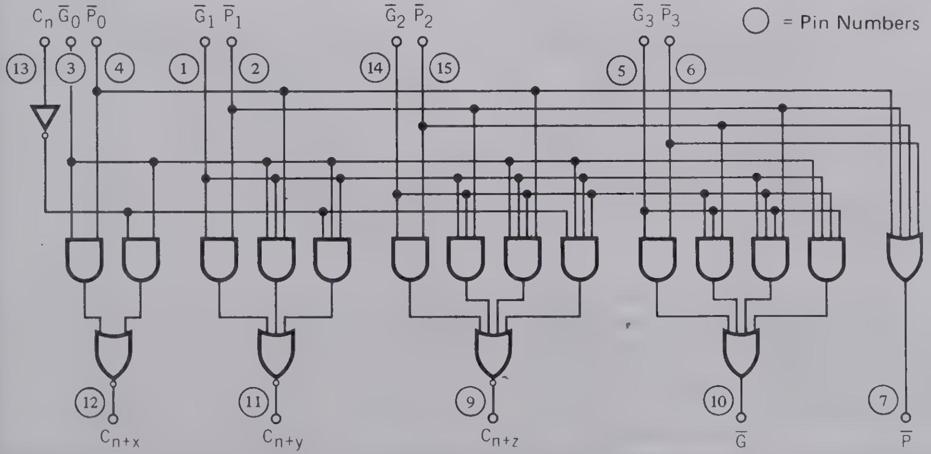
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 G1
2 P1
3 G0
4 P0
5 G3
6 P3
7 P
8 GND
16 VCC
15 P2
14 G2
13 Cn
12 Cn+x
11 Cn+y
10 G
9 Cn+z

FLATPAK (TOP VIEW)


1 G1
2 P1
3 G0
4 P0
5 G3
6 P3
7 P
8 GND
16 VCC
15 P2
14 G2
13 Cn
12 Cn+x
11 Cn+y
10 G
9 Cn+z

LOGIC DIAGRAM


Cn G0 P0
G1 P1
G2 P2
G3 P3
= Pin Numbers
13 3 4 1 2 14 15 5 6
12 Cn+x
11 Cn+y
9 Cn+z
10 G
7 P

FUNCTIONAL DESCRIPTION – The TTL/MSI 9342/54182, lookahead carry generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH Carry Input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 9342/54182, 74182 also has active LOW Carry Propagate (P) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$
\begin{aligned}
C_{n+x} &= G_0 + P_0C_n \\
C_{n+y} &= G_1 + P_1G_0 + P_1P_0C_n \\
C_{n+z} &= G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n \\
\overline{G} &= \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0} \\
\overline{P} &= \overline{P_3P_2P_1P_0}
\end{aligned}
$$

Also, the 9342/54182, 74182 can be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the lookahead carry generator are identical in both cases.

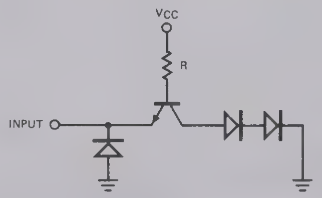
TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

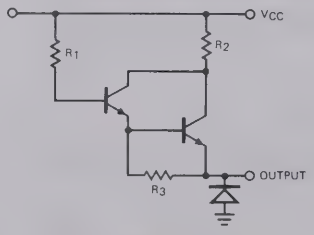
H = HIGH Voltage Level
L = LOW Voltage Level
X – Don't Care

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

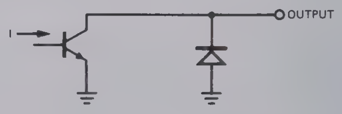
EQUIVALENT INPUT CIRCUIT



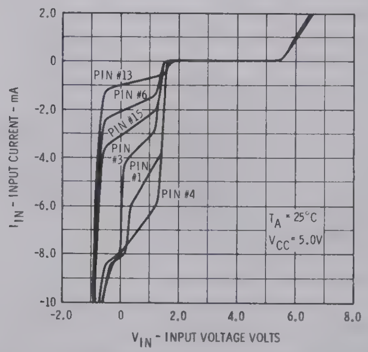
OUTPUT HIGH EQUIVALENT CIRCUIT



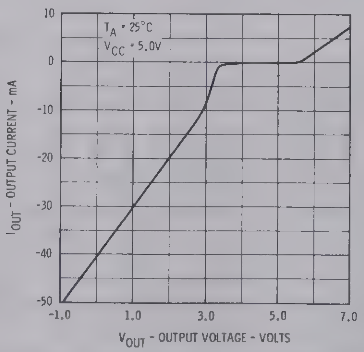
OUTPUT LOW EQUIVALENT CIRCUIT



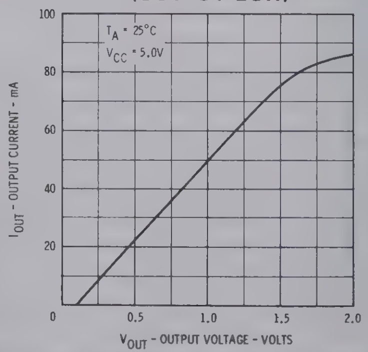
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9342XM/54182XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9342XC/74182XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS		UNITS	CONDITIONS
		MIN.	MAX.		
V_{OH}	Output HIGH Voltage	2.4		Volts	V_{CC} = MIN., I_{OH} = −800 μA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage		−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
I_{IL}	Input LOW Current $\overline{C}_n$ $\overline{P}_3$ $\overline{P}_2$ $\overline{P}_0$, $\overline{P}_1$ or $\overline{G}_3$ $\overline{G}_0$ or $\overline{G}_2$ $\overline{G}_1$		 −1.6 −3.2 −4.8 −6.4 −11.2 −12.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input HIGH Current $\overline{C}_n$ $\overline{P}_3$ $\overline{P}_2$ $\overline{P}_0$, $\overline{P}_1$ or $\overline{G}_3$ $\overline{G}_0$ or $\overline{G}_2$ $\overline{G}_1$		 40 80 120 160 280 320	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current all inputs		1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 4)	−40	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CCH}	Power Supply Current 9342XM/54182XM 9342XC/74182XC		 35 39	 mA mA	V_{CC} = MAX. All outputs HIGH
I_{CCL}	Power Supply Current 9342XM/54182XM 9342XC/74182XC		 65 72	 mA mA	V_{CC} = MAX. All Outputs LOW

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, Pin 8 = Gnd)

SYMBOL	PARAMETER	LIMITS		UNITS	CONDITIONS
		TYP.	MAX.		
t_{PLH} t_{PHL}	(C_n to C_{n+x}, C_{n+y}, C_{n+z})	12 15	16 19	ns	$\overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, $\overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5V Fig.1
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to C_{n+x}, C_{n+y}, or C_{n+z})	8 9	10 11	ns	$\overline{P}_x$ = Gnd (If not under test), $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5V, Fig.2
t_{PLH} t_{PHL}	($\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, or C_{n+z})	8 9	10 11	ns	$\overline{G}_x$ = 4.5V (If not under test), $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, Fig.2
t_{PLH} t_{PHL}	($\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$ or $\overline{P}$)	12 15	16 19	ns	$\overline{P}_x$ = Gnd (If not under test), $\overline{G}_0 = \overline{G}_1 = \overline{G}_2 = \overline{G}_3 = C_n$ = 4.5 V Fig.1
t_{PLH} t_{PHL}	($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ or $\overline{G}_3$ to $\overline{G}$)	12 15	16 19	ns	$\overline{G}_x$ = 4.5V (If not under test), $\overline{P}_1 = \overline{P}_2 = \overline{P}_3$ = Gnd, Fig. 1
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{P}$)	12 15	16 19	ns	$\overline{P}_x$ = Gnd (If not under test), Fig. 1

SWITCHING TIME WAVEFORMS

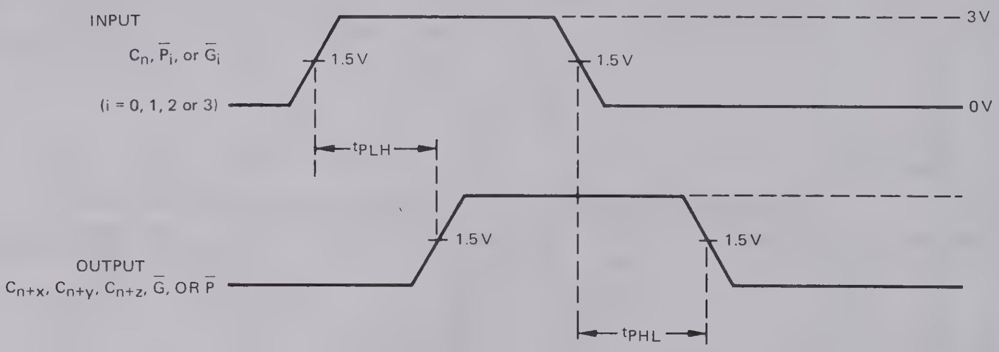

INPUT
C_n, $\overline{P}_i$, or $\overline{G}_i$
(i = 0, 1, 2 or 3)
1.5 V
1.5 V
3V
0V
t_{PLH}
OUTPUT
C_{n+x}, C_{n+y}, C_{n+z}, $\overline{G}$, OR $\overline{P}$
1.5 V
1.5 V
t_{PHL}

Fig. 1

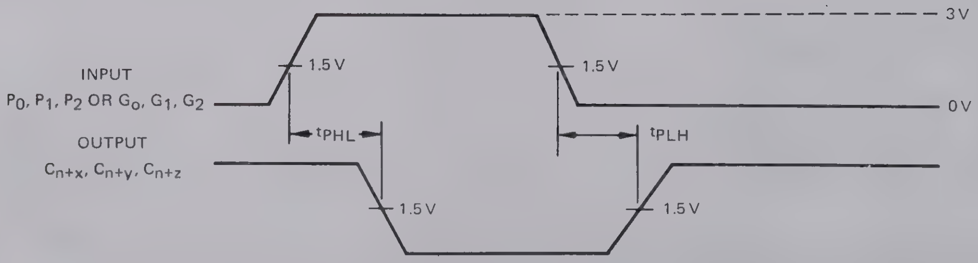

3V
INPUT
P_0, P_1, P_2 OR G_o, G_1, G_2
1.5 V
1.5 V
0V
OUTPUT
C_{n+x}, C_{n+y}, C_{n+z}
t_{PHL}
t_{PLH}
1.5 V
1.5 V

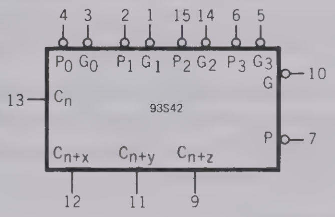
Fig. 2

TTL/MSI 93S42
LOOKAHEAD CARRY GENERATOR

DESCRIPTION — The TTL/MSI 93S42 is a high speed Lookahead Carry Generator. It is generally used with the 93S41 4-Bit Arithmetic Logic Unit to provide super high speed lookahead over word lengths of more than four bits. The lookahead carry generator is fully compatible with all members of the Fairchild TTL Family.

- **TYPICALLY 4 ns DELAY FOR EACH LEVEL OF LOOKAHEAD**
- **PROVIDES LOOKAHEAD CARRIES ACROSS A GROUP OF FOUR ALU'S**
- **MULTI-LEVEL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**
- **INPUT CLAMP DIODES**
- **TTL COMPATIBLE**

LOGIC SYMBOL

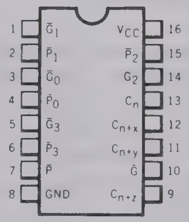

4
3
2
1
15
14
6
5
P0 G0 P1 G1 P2 G2 P3 G3
G
10
13
Cn
93S42
P
7
Cn+x Cn+y Cn+z
12
11
9

V_{CC} = Pin 16
GND = Pin 8

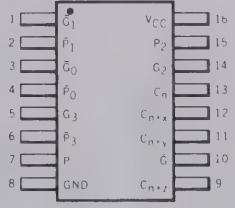
PIN NAMES

C_n	Carry Input
$\overline{G}_0$, $\overline{G}_2$	Carry Generate (Active Low) Inputs
$\overline{G}_1$	Carry Generate (Active Low) Input
$\overline{G}_3$	Carry Generate (Active Low) Input
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate (Active Low) Inputs
$\overline{P}_2$	Carry Propagate (Active Low) Input
$\overline{P}_3$	Carry Propagate (Active Low) Input
C_{n+x}, C_{n+y}, C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate (Active Low) Output
$\overline{P}$	Carry Propagate (Active Low) Output

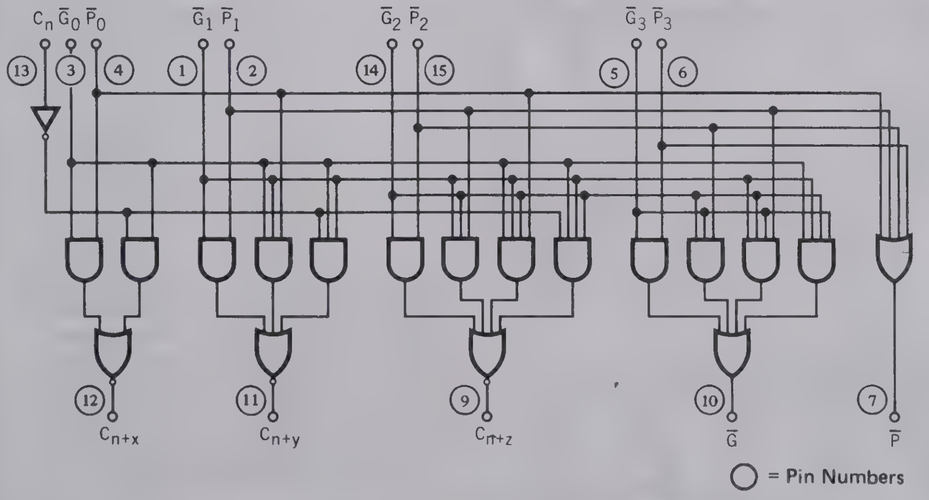
CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 G̅1
2 P̅1
3 G̅0
4 P̅0
5 G̅3
6 P̅3
7 P̅
8 GND
16 VCC
15 P̅2
14 G̅2
13 Cn
12 Cn+x
11 Cn+y
10 G̅
9 Cn+z

FLATPAK (TOP VIEW)


1 G̅1
2 P̅1
3 G̅0
4 P̅0
5 G3
6 P̅3
7 P
8 GND
16 VCC
15 P2
14 G2
13 Cn
12 Cn+x
11 Cn+y
10 G
9 Cn+z

LOGIC DIAGRAM


Cn G̅0 P̅0
13
3
4
G̅1 P̅1
1
2
G̅2 P̅2
14
15
G̅3 P̅3
5
6
12
Cn+x
11
Cn+y
9
Cn+z
10
G̅
7
P̅
= Pin Numbers

TTL/MSI 9344

BINARY (4-BIT BY 2-BIT) FULL MULTIPLIER

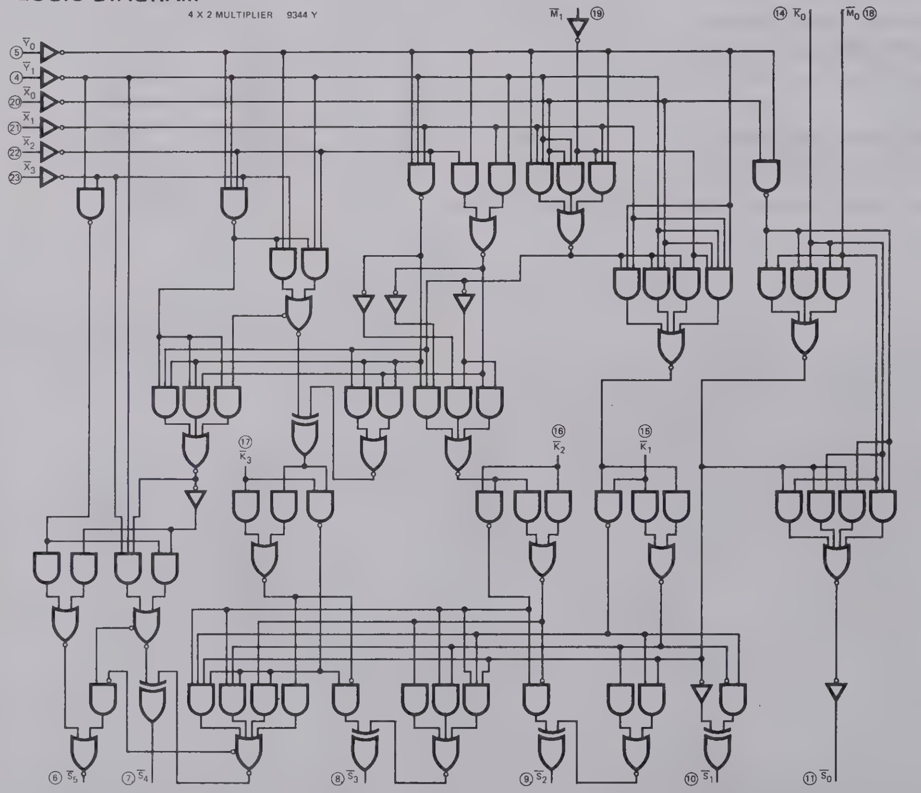
DESCRIPTION – The TTL/MSI 9344 is a 4-bit by 2-bit Full Multiplier building block. It multiplies two binary numbers and simultaneously adds two other binary numbers to the product. 9344's can be interconnected to form a high speed multiplier array of any size. The device is constructed with TTL compatible inputs and outputs. Inputs are buffered to reduce loading. The device is fully compatible with all members of the Fairchild TTL family.

- PERFORMS DIRECT MULTIPLICATION
- EXPANDS TO ANY SIZE ARRAY WITHOUT ADDITIONAL COMPONENTS
- MULTIPLIES AND ADDS SIMULTANEOUSLY
- TTL COMPATIBLE

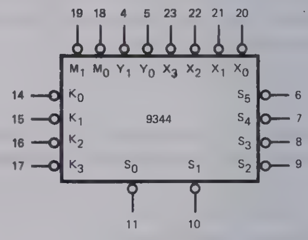
PIN NAMES		LOADING
$\overline{X_0}, \overline{X_1}, \overline{X_2}, \overline{X_3}$	Multiplicand Inputs (Active LOW)	2/3 U.L.
$\overline{Y_0}, Y_1$	Multiplier Inputs (Active LOW)	2/3 U.L.
$\overline{M_1}$	Additive	1.0 U.L.
$\overline{K_0}, \overline{M_0}$	Carry Inputs	4.0 U.L.
$\overline{K_1}, \overline{K_2}, \overline{K_3}$	(Active LOW)	2.0 U.L.
$\overline{S_0}, \overline{S_1}, \overline{S_2}, \overline{S_3}, \overline{S_4}, \overline{S_5}$	Outputs	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM

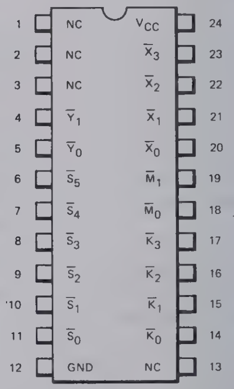

4 X 2 MULTIPLIER 9344 Y
M1 ⑲
⑭ K0
M0 ⑱
⑤ Y0
④ Y1
⑳ X0
㉑ X1
㉒ X2
㉓ X3
⑰ K3
⑯ K2
⑮ K1
⑥ S5
⑦ S4
⑧ S3
⑨ S2
⑩ S1
⑪ S0

LOGIC SYMBOL

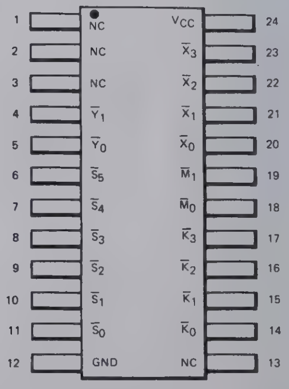

19
18
4
5
23
22
21
20
M1
M0
Y1
Y0
X3
X2
X1
X0
14
15
16
17
K0
K1
K2
K3
9344
S5
S4
S3
S2
6
7
8
9
S0
S1
11
10

V_{CC} = PIN 24
GND = PIN 12
NC = PIN 1, 2, 3, 13

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 NC
2 NC
3 NC
4 Y1
5 Y0
6 S5
7 S4
8 S3
9 S2
10 S1
11 S0
12 GND
24 VCC
23 X3
22 X2
21 X1
20 X0
19 M1
18 M0
17 K3
16 K2
15 K1
14 K0
13 NC

FLATPAK (TOP VIEW)


1 NC
2 NC
3 NC
4 Y1
5 Y0
6 S5
7 S4
8 S3
9 S2
10 S1
11 S0
12 GND
24 VCC
23 X3
22 X2
21 X1
20 X0
19 M1
18 M0
17 K3
16 K2
15 K1
14 K0
13 NC

FUNCTIONAL DESCRIPTION — The 9344 is a binary full multiplier for 4-bit by 2-bit words. It is easily expandable in an array to form a high speed parallel multiplier of any length.

The functional equation is illustrated below:

S(6-bits) = $\overline{X}$(4-bits) times $\overline{Y}$(2-bits) plus $\overline{M}$(2-bits) plus $\overline{K}$(4-bits)

Functionally the 9344 multiplies a 4-bit word ($\overline{X}_0 - \overline{X}_3$) by a two bit word ($\overline{Y}_0 - \overline{Y}_1$), generating eight partial products. Two other words, $\overline{K}_0 - \overline{K}_3$ and $\overline{M}_0 - \overline{M}_1$, are added to these partial products through a lookahead carry adder, generating a 6-bit product/sum.

The function can be described by the following equation (note that "+" means arithmetic addition):

$$S = 2^0 (\overline{X}_0\overline{Y}_0 + \overline{M}_0 + \overline{K}_0) + 2^1 (\overline{X}_1\overline{Y}_0 + \overline{X}_0\overline{Y}_1 + \overline{M}_1 + \overline{K}_1) + 2^2 (\overline{X}_2\overline{Y}_0 + \overline{X}_1\overline{Y}_1 + \overline{K}_2) + 2^3 (\overline{X}_3\overline{Y}_0 + \overline{X}_2\overline{Y}_1 + \overline{K}_3) + 2^4 (\overline{X}_3\overline{Y}_1).$$

All inputs and outputs are active LOW; X and Y inputs are buffered to present only one TTL unit load.

The device operates only on positive numbers. If two's complement mutliplication is required, then the numbers must be changed to sign-magnitude before multiplication, or else the product must be corrected following multiplication of the two's complement numbers. The correction algorithm depends on whether X or Y or both are negative.

If X is negative:
    Subtract Y from most significant half of product.

If Y is negative:
    Subtract X from most significant half of product.

If both X and Y are negative:
    Add X plus Y to most significant half of product.

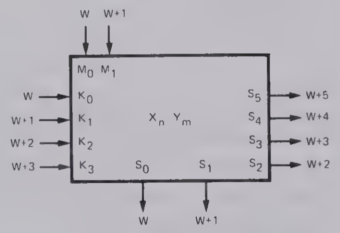
The result will be the correct two's complement product.

MULTIPLICATION TIME

NUMBER OF BITS	PACKAGES	TIME (ns)
8 x 8	8	150
12 x 12	18	260
16 x 16	32	350
24 x 24	72	550

Fig. 1

WEIGHTING FACTORS OF THE BASIC MULTIPLIER



This block represents the basic 4 by 2-bit multiplier, and indicates the weighting factors (power of two) attached to each of the inputs and outputs.

Fig. 2

SWITCHING CHARACTERISTICS

$\overline{M}_1$ TO $\overline{S}_3$

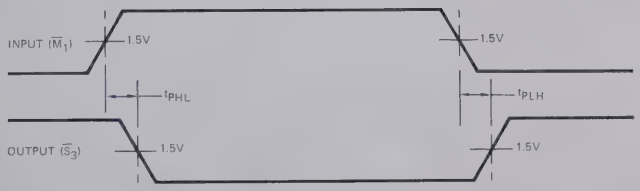


Fig. 3

$\overline{K}_0$ TO $\overline{S}_5$

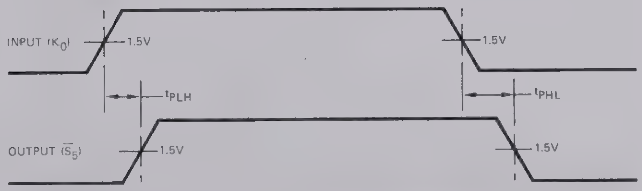


Fig. 4

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9344 XM	4.5 V	5.0 V	5.5 V	−55° C to 125° C
9344 XC	4.75 V	5.0 V	5.25 V	0° C to 75° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Votlage for All Inputs
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −800 μA, V_{IN} = V_{IH} or V_{IL}
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}
I_{IH}	Input HIGH Current					
	$\overline{Y}_{0,1}$; $\overline{X}_{0,1,2,3}$			27	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	$\overline{M}_1$			40		
	$\overline{K}_{1,2,3}$			80		
	$\overline{K}_0$, $\overline{M}_0$			160		
I_{IL}	Input LOW Current					
	$\overline{Y}_{0,1}$; $\overline{X}_{0,1,2,3}$			−1.07	mA	V_{CC} = MAX., V_{IN} = 0.4 V
	$\overline{M}_1$			−1.6		
	$\overline{K}_{1,2,3}$			−3.2		
	$\overline{K}_0$, $\overline{M}_0$			−6.4		
I_{SC}	Output Short Circuit Current (Note 5)	−20		−70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		110	150	mA	V_{CC} = MAX.
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output ($\overline{M}_1$ to $\overline{S}_3$)		40	51	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay Input to Output ($\overline{M}_1$ to $\overline{S}_3$)		40	52	ns	
t_{PLH}	Turn Off Delay Input to Output ($\overline{K}_0$ to $\overline{S}_5$)		16	22	ns	
t_{PHL}	Turn On Delay Input to Output ($\overline{K}_0$ to $\overline{S}_5$)		30	39	ns	

TYPICAL MULTIPLICATION ARRAYS

The 9344 can be assembled in an iterative structure to perform multi-bit multiplication. The blocks are interconnected so that partial product sums generated in a particular 9344 are applied, if necessary, to equal weight carry inputs ($\overline{K}_{0,1,2,3}$ or $\overline{M}_{0,1}$) of succeeding stages.

In the iteritive multiplication arrays shown, weighting factors of the carry and sums between 9344's are indicated (i.e., $0 = 2^0$, $1 = 2^1$, $2 = 2^2$, etc.). Labels inside the blocks identify bits multiplied in that block. For instance 0–0 refers to multiplicand bits $B_{0,1,2,3}$ and multiplier bits $A_{0,1}$, while 4–2 would represent multiplicant bits $B_{4,5,6,7}$ and multiplier bits $A_{2,3}$.

8-BIT BY 5-BIT MULTIPLICATION ARRAY

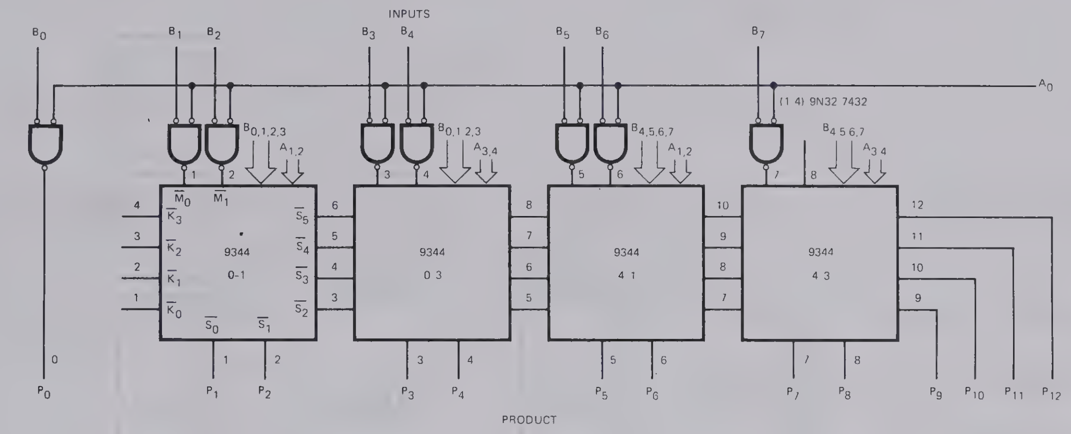

INPUTS
B0
B1
B2
B3
B4
B5
B6
B7
A0
(1 4) 9N32 7432
B0,1,2,3
A1,2
B0,1 2,3
A3,4
B4,5,6,7
A1,2
B4 5 6,7
A3 4
M0
M1
K3
K2
K1
K0
S0
S1
S2
S3
S4
S5
9344
0-1
9344
0 3
9344
4 1
9344
4 3
P0
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
PRODUCT

Fig. 5

8-BIT BY 8-BIT MULTIPLICATION ARRAY

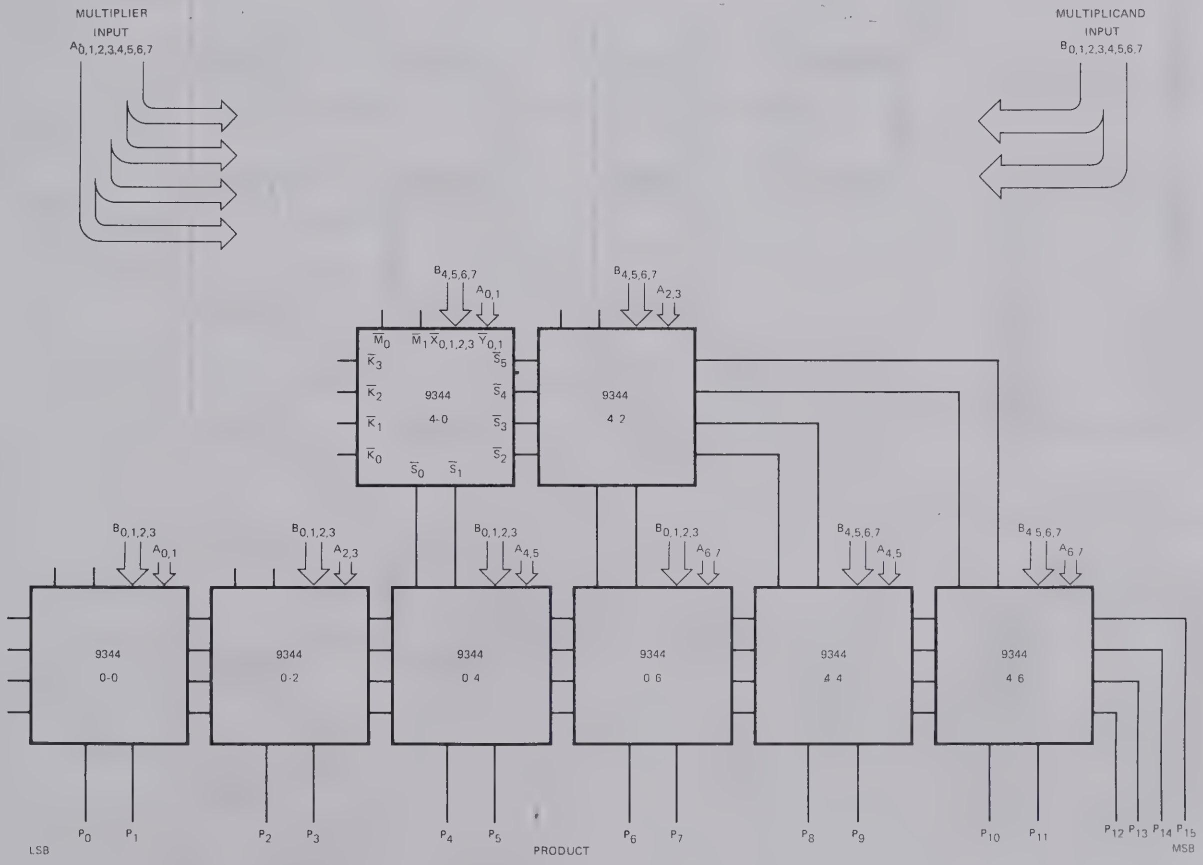
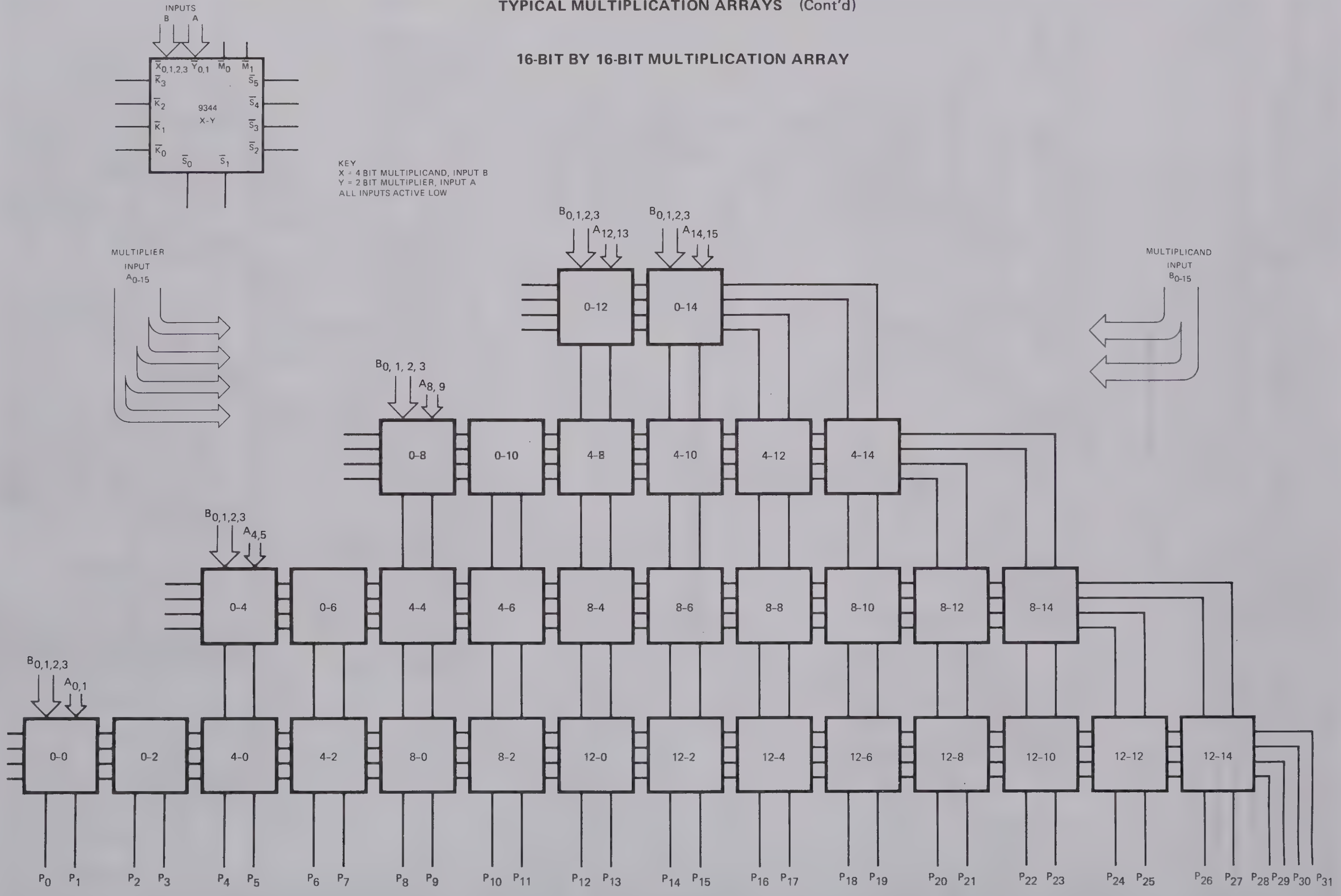

MULTIPLIER
INPUT
A0,1,2,3,4,5,6,7
MULTIPLICAND
INPUT
B0,1,2,3,4,5,6,7
B4,5,6,7
A0,1
B4,5,6,7
A2,3
M0
M1
X0,1,2,3
Y0,1
K3
K2
K1
K0
S0
S1
S2
S3
S4
S5
9344
4-0
9344
4 2
B0,1,2,3
A0,1
B0,1,2,3
A2,3
B0,1,2,3
A4,5
B0,1,2,3
A6 7
B4,5,6,7
A4,5
B4 5,6,7
A6 7
9344
0-0
9344
0-2
9344
0 4
9344
0 6
9344
4 4
9344
4 6
P0
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
LSB
PRODUCT
MSB

Fig. 6

TYPICAL MULTIPLICATION ARRAYS (Cont'd)

16-BIT BY 16-BIT MULTIPLICATION ARRAY


INPUTS
B A
$\overline{X}_{0,1,2,3}$ $\overline{Y}_{0,1}$ $\overline{M}_0$ $\overline{M}_1$
$\overline{K}_3$ $\overline{K}_2$ $\overline{K}_1$ $\overline{K}_0$
9344
X-Y
$\overline{S}_0$ $\overline{S}_1$ $\overline{S}_2$ $\overline{S}_3$ $\overline{S}_4$ $\overline{S}_5$
KEY
X = 4 BIT MULTIPLICAND, INPUT B
Y = 2 BIT MULTIPLIER, INPUT A
ALL INPUTS ACTIVE LOW
MULTIPLIER INPUT A_{0-15}
MULTIPLICAND INPUT B_{0-15}
$B_{0,1,2,3}$ $A_{0,1}$
$B_{0,1,2,3}$ $A_{4,5}$
$B_{0,1,2,3}$ $A_{8,9}$
$B_{0,1,2,3}$ $A_{12,13}$
$B_{0,1,2,3}$ $A_{14,15}$
0-12 0-14
0-8 0-10 4-8 4-10 4-12 4-14
0-4 0-6 4-4 4-6 8-4 8-6 8-8 8-10 8-12 8-14
0-0 0-2 4-0 4-2 8-0 8-2 12-0 12-2 12-4 12-6 12-8 12-10 12-12 12-14
P_0 P_1 P_2 P_3 P_4 P_5 P_6 P_7 P_8 P_9 P_{10} P_{11} P_{12} P_{13} P_{14} P_{15} P_{16} P_{17} P_{18} P_{19} P_{20} P_{21} P_{22} P_{23} P_{24} P_{25} P_{26} P_{27} P_{28} P_{29} P_{30} P_{31}
PRODUCT

Note: Each block represents one 9344. Labels inside the blocks identify bits multiplied in that block. The first number is the 4-bit B input, and the second number is the 2-bit A input. For instance, 12–0 refers to multiplicand bits $B_{12,13,14,15}$ and multiplier bits $A_{0,1}$.

Fig. 7

TTL/MSI 9345/5445, 7445
93145/54145, 74145
1-OF-10 DECODER/DRIVER

DESCRIPTION — The 9345/5445, 7445 and 93145/54145, 74145 1-of-10 Decoder/Drivers are designed to accept BCD inputs and provide appropriate outputs to drive 10 digit incandescent displays. All outputs remain off for all invalid binary input conditions. These devices are designed for use as indicator/relay drivers or as open-collector logic circuit drivers. Each of the high breakdown output transistors (9345/5445, 7445 = 30 V and 93145/54145, 74145 = 15 V) will sink up to 80 mA of current. Typical power dissipation is 215 mW.

PIN NAMES		**LOADING** (Note a)
P_A, P_B, P_C, P_D	BCD Inputs	1 U.L.
$\overline{Q}_0$ to $\overline{Q}_9$	Outputs	(Note b)

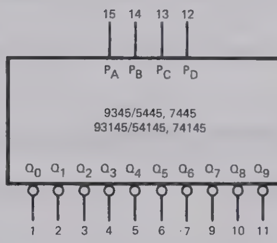
NOTES:

a. 1 U.L. = 40 μA HIGH/1.6 mA LOW.

b. Output Characteristics.

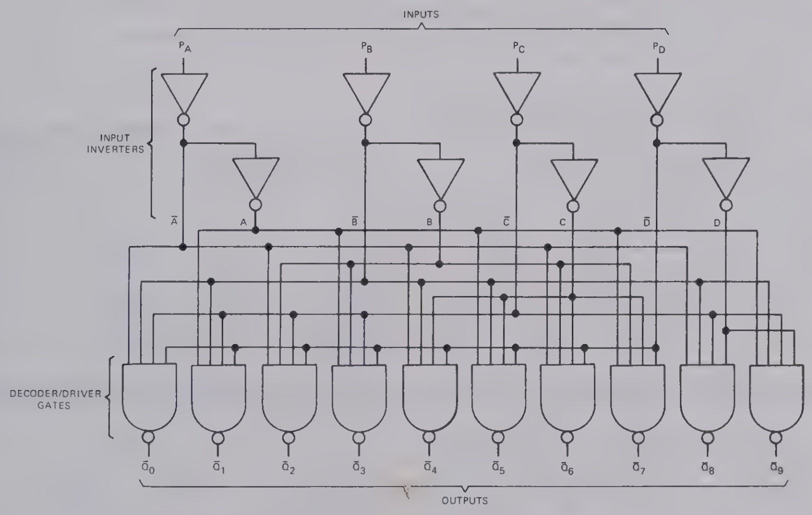
MAX. Sinking current in LOW state	80 mA.
MIN. HIGH Voltage breakdown:	
9345/5445, 7445	30 V
93145/54145, 74145	15 V

LOGIC SYMBOL

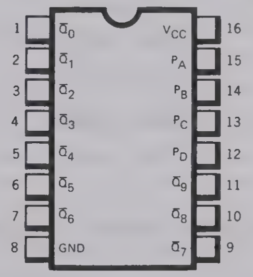

15 14 13 12
PA PB PC PD
9345/5445, 7445
93145/54145, 74145
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
1 2 3 4 5 6 7 9 10 11

V_{CC} = PIN 16
GND = PIN 8

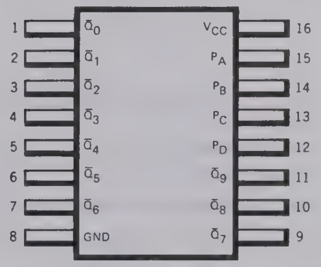
LOGIC DIAGRAM


INPUTS
PA
PB
PC
PD
INPUT INVERTERS
Ā
A
B̄
B
C̄
C
D̄
D
DECODER/DRIVER GATES
Q̄0
Q̄1
Q̄2
Q̄3
Q̄4
Q̄5
Q̄6
Q̄7
Q̄8
Q̄9
OUTPUTS

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 Q̄0
2 Q̄1
3 Q̄2
4 Q̄3
5 Q̄4
6 Q̄5
7 Q̄6
8 GND
16 VCC
15 PA
14 PB
13 PC
12 PD
11 Q̄9
10 Q̄8
9 Q̄7

FLATPAK (TOP VIEW)


1 Q̄0
2 Q̄1
3 Q̄2
4 Q̄3
5 Q̄4
6 Q̄5
7 Q̄6
8 GND
16 VCC
15 PA
14 PB
13 PC
12 PD
11 Q̄9
10 Q̄8
9 Q̄7

Positive Logic: See Truth Table.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5V to +30V
Output Current (dc) (Output LOW)	+80 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9345XM/5445XM 93145XM/54145XM			9345XC/7445XC 93145XC/74145XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 3)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
PARAMETER	9345/5445, 7445			93145/54145, 74145			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Voltage on Any Output (See Note 4)			30			15	Volts

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage		1 & 2
V_{OL}	Output LOW Voltage		0.5	0.9	Volts	I_{OL} = 80 mA	V_{CC} = MIN.	1
				0.4	Volts	I_{OL} = 20 mA		
V_{OH}	Output HIGH Voltage	30			Volts	9345/5445, 7445	V_{CC} = MAX.	2
		15			Volts	93145/54145, 74145	I_{OH} = 250 µA	
I_{IH}	Input HIGH Current (Each Input)			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current (Each Input			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{CC}	Supply Current		43	62	mA	9345/5445, 93145/54145	V_{CC} = MAX.	4
			43	70	mA	9345/7445, 93145/74145		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output			50	ns	V_{CC} = 5.0 V C_L = 5 pF R_L = 100Ω	A
t_{PHL}	Turn On Delay Input to Output			50	ns		

NOTES:

1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C.
3. These voltage values are with respect to network ground terminal
4. This rating applies when the output is off.

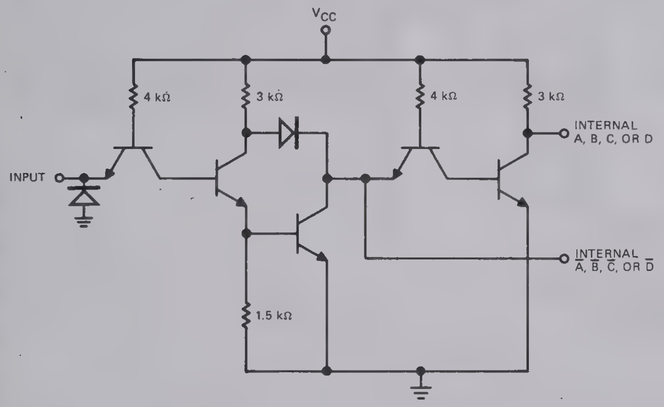
TRUTH TABLE

INPUTS				OUTPUTS									
P_D	P_C	P_B	P_A	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

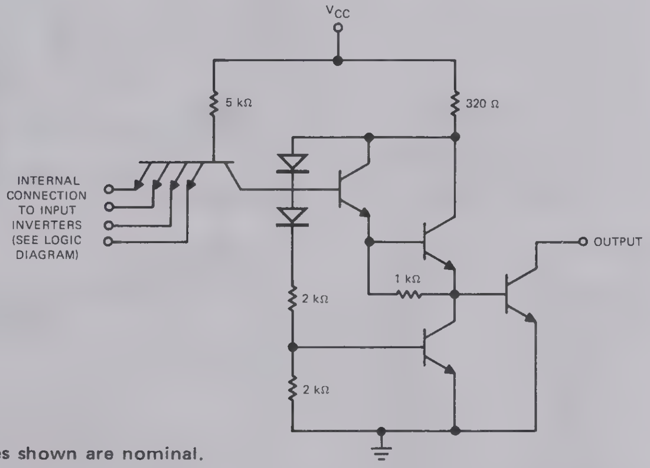
H = HIGH Voltage Level
L = LOW Voltage Level

SCHEMATIC DIAGRAMS

EACH PAIR OF INPUT INVERTERS


V_{CC}
4 kΩ
3 kΩ
4 kΩ
3 kΩ
INTERNAL A, B, C, OR D
INPUT
INTERNAL $\overline{A}$, $\overline{B}$, $\overline{C}$, OR $\overline{D}$
1.5 kΩ

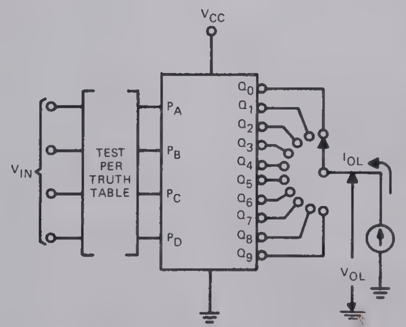
EACH DECODER/DRIVER GATE


V_{CC}
5 kΩ
320 Ω
INTERNAL CONNECTION TO INPUT INVERTERS (SEE LOGIC DIAGRAM)
OUTPUT
1 kΩ
2 kΩ
2 kΩ

NOTE: Component values shown are nominal.

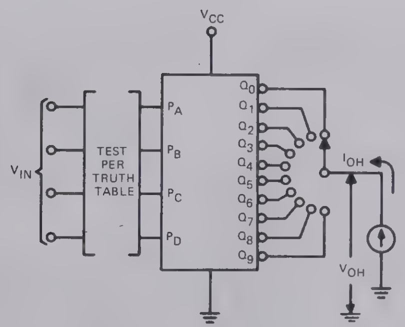
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*


V_{CC}
V_{IN}
TEST PER TRUTH TABLE
P_A
P_B
P_C
P_D
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
Q_8
Q_9
I_{OL}
V_{OL}

1. Each output is tested separately in the ON state.

Fig. 1


V_{CC}
V_{IN}
TEST PER TRUTH TABLE
P_A
P_B
P_C
P_D
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
Q_8
Q_9
I_{OH}
V_{OH}

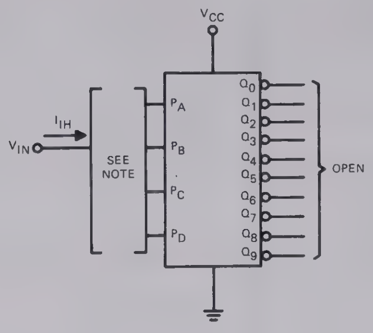
1. Each output is tested separately in the OFF state.

Fig. 2

*Arrows indicate actual direction of current flow.

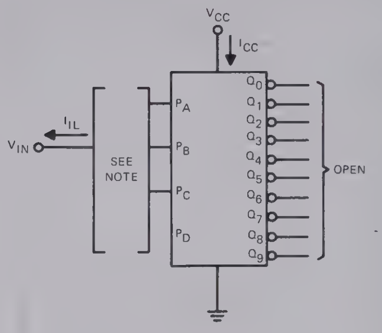
PARAMETER MEASUREMENT INFORMATION

D.C. TEST CIRCUITS* (Continued)


V_{CC}
I_{IH}
V_{IN}
SEE NOTE
P_A
P_B
P_C
P_D
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
Q_8
Q_9
OPEN

1. Each input is tested separately.

Fig. 3


V_{CC}
I_{CC}
I_{IL}
V_{IN}
SEE NOTE
P_A
P_B
P_C
P_D
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
Q_8
Q_9
OPEN

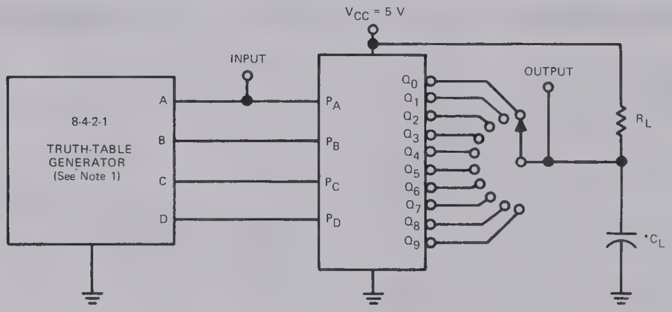
1. When testing I_{IL} each input is tested separately.
2. When testing I_{CC} all inputs are gounded and outputs are open.

Fig. 4

*Arrows indicate actual direction of current flow.

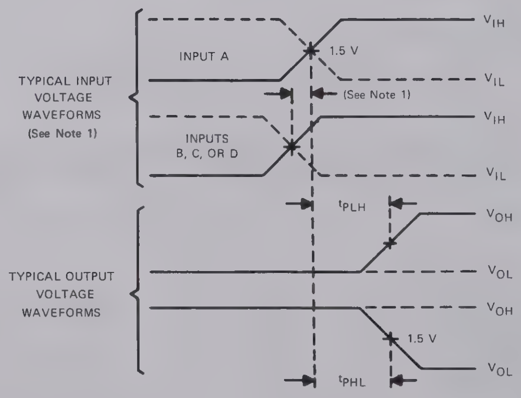
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS


V_{CC} = 5 V
INPUT
OUTPUT
8-4-2-1
TRUTH-TABLE GENERATOR (See Note 1)
A
B
C
D
P_A
P_B
P_C
P_D
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
Q_8
Q_9
R_L
$*C_L$

*Includes probe and jig capacitance.

TEST CIRCUIT


TYPICAL INPUT VOLTAGE WAVEFORMS (See Note 1)
INPUT A
1.5 V
V_{IH}
V_{IL}
(See Note 1)
INPUTS B, C, OR D
V_{IH}
V_{IL}
t_{PLH}
TYPICAL OUTPUT VOLTAGE WAVEFORMS
V_{OH}
V_{OL}
V_{OH}
1.5 V
V_{OL}
t_{PHL}

VOLTAGE WAVEFORMS

NOTE:

1. The truth-table generator has the following charateristics: $V_{OH} \geqslant 2.4$ V, $V_{OL} \leqslant 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions.

Fig. A SWITCHING TIMES

TTL/MSI 9348

12-INPUT PARITY CHECKER/GENERATOR

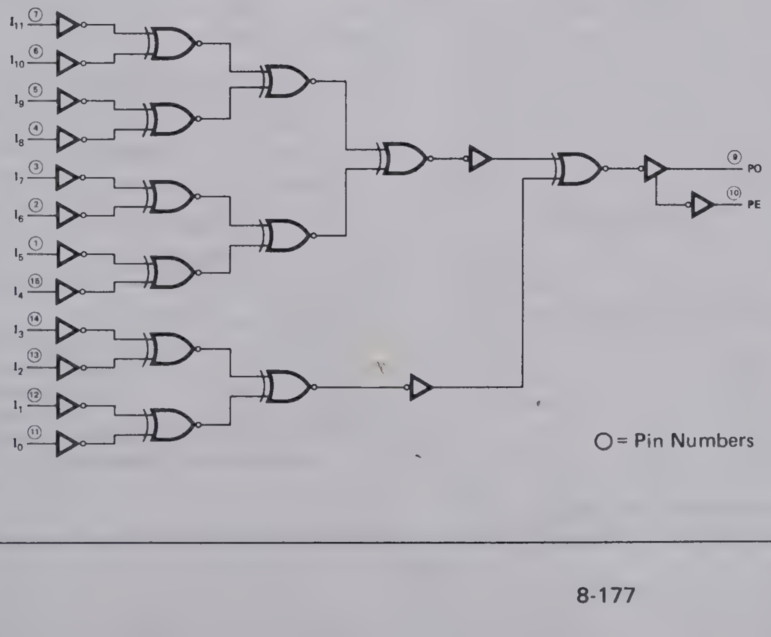
DESCRIPTION – The TTL/MSI 9348 is a 12-Input Parity Checker/Generator generating odd and even parity outputs. It can be used in high speed error detection applications. The 9348 uses TTL technology for high capacitive drive capability, and provides low impedance in both logic states for good ac noise immunity. All inputs feature diode clamping to reduce negative line transients. This device is compatible with all members of the TTL family of digital integrated circuits.

- **BOTH ODD AND EVEN PARITY OUTPUTS PROVIDED**
- **GENERATES A PARITY BIT FOR UP TO 12 BITS**
- **CHECKS FOR PARITY ON UP TO 12 BITS**
- **EASILY EXPANDABLE**
- **HIGH DRIVE OUTPUT CIRCUITRY**
- **INPUT CLAMP DIODE LIMITS HIGH SPEED TERMINATION EFFECTS**
- **TTL COMPATIBLE**

PIN NAMES		**LOADING** (Note a)
I_0 to I_{11}	Parity Inputs	2 U.L.
PO	Odd Parity Output (Note b)	10 U.L.
PE	Even Parity Output (Note b)	10 U.L.

NOTES:
(a) 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
(b) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

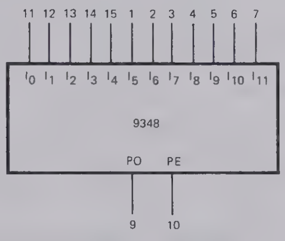
LOGIC DIAGRAM



I11 7
I10 6
I9 5
I8 4
I7 3
I6 2
I5 1
I4 15
I3 14
I2 13
I1 12
I0 11
9 PO
10 PE

○ = Pin Numbers

LOGIC SYMBOL

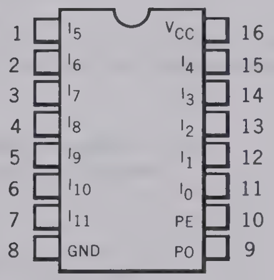


11 12 13 14 15 1 2 3 4 5 6 7
I0 I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11
9348
PO PE
9 10

V_{CC} = Pin 16
Gnd = Pin 8

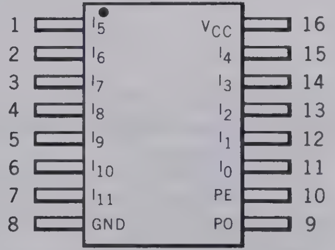
CONNECTION DIAGRAMS

DIP (TOP VIEW)



1 I5
2 I6
3 I7
4 I8
5 I9
6 I10
7 I11
8 GND
16 VCC
15 I4
14 I3
13 I2
12 I1
11 I0
10 PE
9 PO

FLATPAK (TOP VIEW)



1 I5
2 I6
3 I7
4 I8
5 I9
6 I10
7 I11
8 GND
16 VCC
15 I4
14 I3
13 I2
12 I1
11 I0
10 PE
9 PO

FUNCTIONAL DESCRIPTION – The MSI 9348 is a 12-input parity generator. It provides odd and even parity for up to 12 data bits. The Even Parity output (PE) will be HIGH if an even number of logic ones are present on the inputs. The Odd Parity output (PO) will be HIGH if an odd number of logic ones are present on the inputs. The logic equations for the outputs are shown below.

$$PO = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$$
$$PE = \overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$$

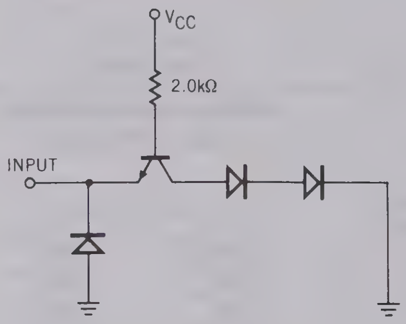
NOTE: Less through delay is encountered from the I_0, I_1, I_2, and I_3 inputs than I_4 thru I_{11} inputs. Therefore, if some signals are slower than others, the slower signals should be applied to these four inputs for maximum speed.

TRUTH TABLE

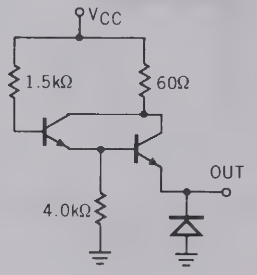
INPUTS	OUTPUTS	
$I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8, I_9, I_{10}, I_{11}$	P_O	P_E
All Twelve Inputs LOW	0	1
Any One Input HIGH	1	0
Any Two Inputs HIGH	0	1
Any Three Inputs HIGH	1	0
Any Four Inputs HIGH	0	1
Any Five Inputs HIGH	1	0
Any Six Inputs HIGH	0	1
Any Seven Inputs HIGH	1	0
Any Eight Inputs HIGH	0	1
Any Nine Inputs HIGH	1	0
Any Ten Inputs HIGH	0	1
Any Eleven Inputs HIGH	1	0
All Twelve Inputs HIGH	0	1

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

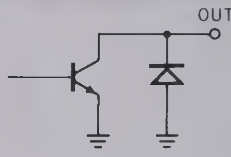
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE

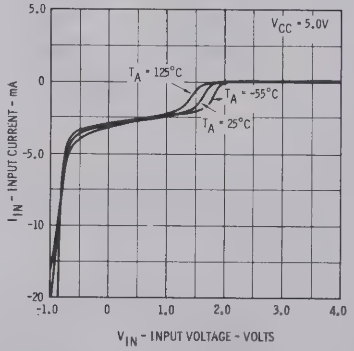


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

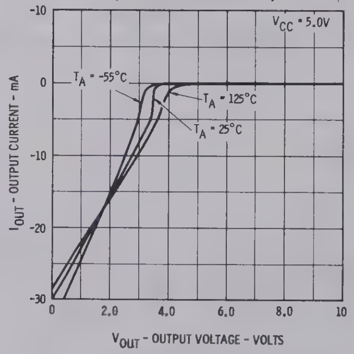


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

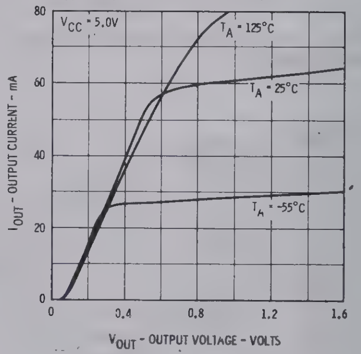


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9348XM	4.5 V	5.0 V	5.5 V	–55°C to 125°C
9348XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		20	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current		–1.92	–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	–20	–50	–70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		47	82	mA	V_{CC} = MAX.
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC}=MIN., I_{IN}=–12 mA, T_A=25°C

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

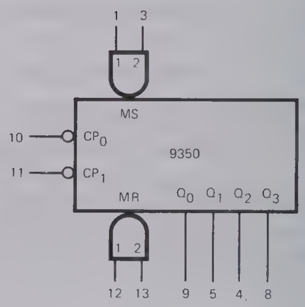
SYMBOL	PARAMETER	MIL LIMITS			IND LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output (I_4 to PO, Pin 15 to Pin 9)		40	46		40	48	ns	V_{CC} = 5.0 V, C_L = 15 pF Pins 3, 4, 13 & 14 = Gnd Others HIGH
t_{PHL}	Turn On Delay Input to Output (I_4 to PO, Pin 15 to Pin 9)		36	46		36	48	ns	
t_{PLH}	Turn Off Delay Input to Output (I_4 to PE, Pin 15 to Pin 10)		47	53		47	55	ns	
t_{PHL}	Turn On Delay Input to Output (I_4 to PE, Pin 15 to Pin 10)		41	48		41	50	ns	
t_{PLH}	Turn Off Delay Input to Output (I_3 to PO, Pin 14 to Pin 9)		20	27		20	29	ns	V_{CC} = 5.0 V, C_L = 15 pF Pins 1, 2, 4, 5, 6, 7, 11, 12, 13 & 15 = Gnd Pin 3 HIGH
t_{PHL}	Turn On Delay Input to Output (I_4 to PO, Pin 15 to Pin 9)		19	25		19	27	ns	V_{CC} = 5.0 V, C_L = 15 pF Pins 1, 2, 3, 4, 5, 6, 7, 11, 12, 13, 14 = Gnd

TTL/MSI 9350
DECADE COUNTER

DESCRIPTION – The TTL/MSI 9350 is a Monolithic Decade Counter. This multifunctional MSI building block is capable of being used as a divide-by-two, divide-by-five or divide-by-ten counter. It is useful in a large number of counting applications in digital computer systems, data handling systems and control systems.

- **FUNCTIONALLY EQUIVALENT TO THE 7490**
- **STANDARD CORNER POWER PINS FOR EASY USE**
- **HIGH SPEED, 18 MHz TYPICAL**
- **TYPICAL POWER DISSIPATION OF 160 mW**
- **TTL COMPATIBLE**
- **ALL CERAMIC, HERMETIC 14-LEAD DUAL IN-LINE PACKAGE**
- **INPUT DIODE CLAMPING**

LOGIC SYMBOL

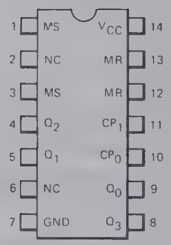

1
3
1
2
MS
10
$\overline{CP}_0$
9350
11
$\overline{CP}_1$
MR
Q_0
Q_1
Q_2
Q_3
1
2
12
13
9
5
4
8

V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 6

PIN NAMES		**LOADING** (Note a)
$\overline{CP}_0$	Clock First Stage Negative Edge Input	2 U.L.
$\overline{CP}_1$	Clock Second, Third, and Fourth Stage Negative Edge Input	4 U.L.
MR	"AND" Master Reset to Binary Zero (Asynchronous) Input	1 U.L.
MS	"AND" Master Set to Binary Nine (Asynchronous) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Counter Outputs (Note b)	10 U.L.

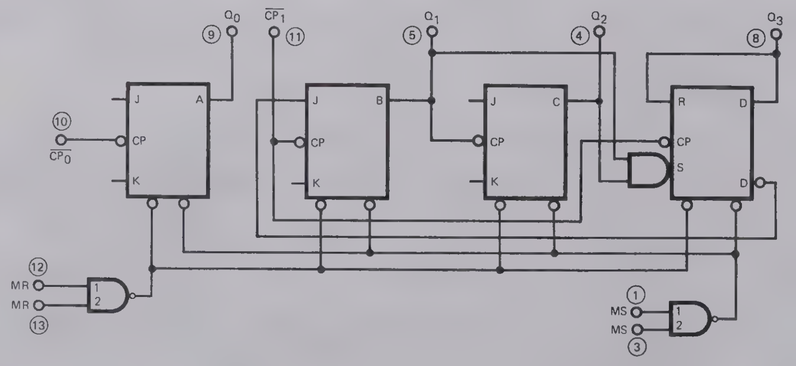
NOTES:
(a) 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
(b) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 MS
2 NC
3 MS
4 Q_2
5 Q_1
6 NC
7 GND
14 V_{CC}
13 MR
12 MR
11 CP_1
10 CP_0
9 Q_0
8 Q_3

NC — No internal connection

LOGIC DIAGRAM


Q_0
9
$\overline{CP}_1$
11
Q_1
5
Q_2
4
Q_3
8
10
$\overline{CP}_0$
J
A
CP
K
J
B
CP
K
J
C
CP
K
R
D
CP
S
D
12
MR
MR
13
1
2
1
MS
MS
3
1
2

○ = Pin Numbers

FUNCTIONAL DESCRIPTION

The 9350 is an up decade counter. It consists of four dual-rank, master-slave flip-flops internally interconnected to provide a dividy-by-two counter and a divide-by-five counter. A gated "AND" Master Reset is provided to inhibit counting and return all outputs to a LOW state. A gated "AND" Master Set is provided which will set the counter to a binary coded decimal count of nine (9), overriding all other count or reset conditions. Since the output from the first flip-flop is not internally connected to the succeeding stages, the device may be operated in three independent count modes:

A. BCD Decade Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two & Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. (CP_0 as the input and Q_0 as the output.) The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_1, Q_2, and Q_3 outputs.

NOTE: The 9350 flip-flops change state after the HIGH to LOW transition of the clock.

MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X		COUNT		
X	L	X	L		COUNT		
L	X	X	L		COUNT		
X	L	L	X		COUNT		

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care Condition

BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9350XC (IND)			UNITS
	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range	0	25	75	°C
Normalized Fan Out from Each Output, N			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9350XC*)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4	3.0		Volts	V_{CC} = 4.75 V, I_{OH} = −800 μA
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = 4.75 V, I_{OL} = 16 mA
I_{IH}	Input HIGH Current, MS, MR $\overline{CP}_0$ $\overline{CP}_1$		10 20 40	40 80 160	μA	V_{CC} = 5.25 V V_{IN} = 2.4 V
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = 5.25 V, V_{IN} = 5.5 V
I_{IL}	Input LOW Current, MS, MR $\overline{CP}_0$ $\overline{CP}_1$		−1.0 −2.0 −4.0	−1.6 −3.2 −6.4	mA	V_{CC} = 5.25 V, V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−18		−57	mA	V_{CC} = 5.25 V, V_{OUT} = 0V
I_{CC}	Power Supply Current		30	53	mA	V_{CC} = 5.25 V

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

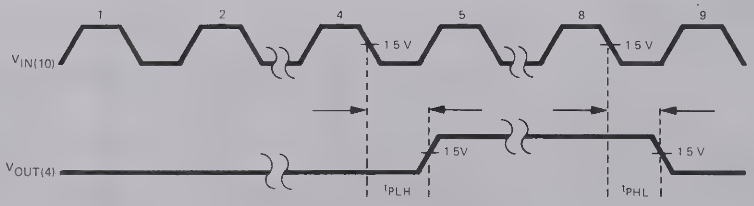
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{PLH}	Turn-Off Delay $\overline{CP}_0$ to Output Q_2		60	100	ns	V_{CC} = 5.0 V, C_L = 15 pF Q_0 Output Connected to $\overline{CP}_1$ Input
t_{PHL}	Turn-On Delay $\overline{CP}_0$ to Output Q_2		60	100	ns	
f_{max}	Maximum Frequency of Input Count Pulses	10	18		MHz	

SWITCHING TIME WAVEFORMS

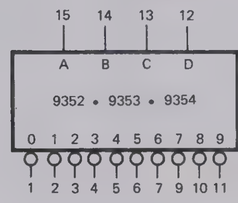


TTL/MSI 9352/5442, 7442
9353/5443, 7443 • 9354/5444, 7444
FOUR LINE TO TEN LINE DECODER (1-OF-10)

DESCRIPTION — These monolithic Decimal Decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic insures that all outputs remain off for all invalid input conditions.

The TTL/MSI 9352/5442, 7442 BCD-to-decimal; TTL/MSI 9353/5443, 7443 excess 3-to-decimal; and TTL/MSI 9354/5444, 7444 excess 3 gray-to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs compatible for use with other TTL and DTL circuits. The dc noise margins are typically 1.0V and power dissipation is typically 140 mW. Full fan out of 10 is available at all outputs.

LOGIC SYMBOL


15
14
13
12
A
B
C
D
9352 • 9353 • 9354
0 1 2 3 4 5 6 7 8 9
1 2 3 4 5 6 7 9 10 11

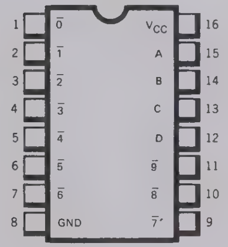
V_{CC} = Pin 16
GND = Pin 8

9352/5442, 7442
9353/5443, 7443
9354/5444, 7444

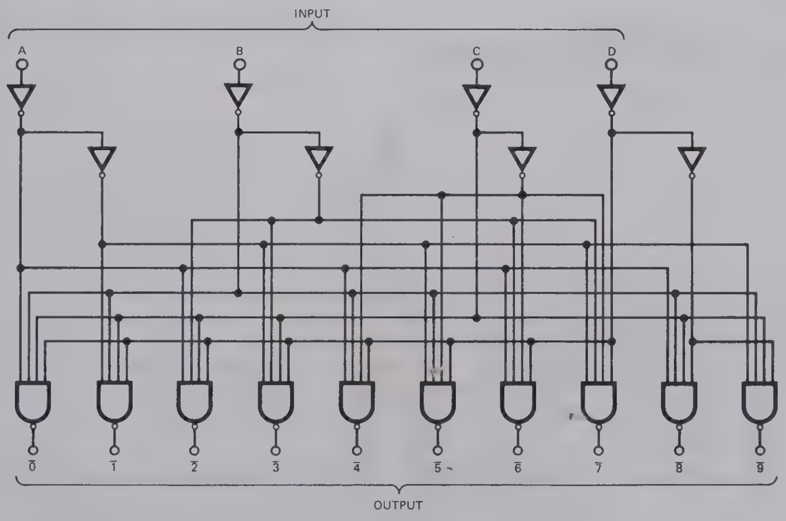
PIN NAMES		LOADING
A, B, C, D	BCD Inputs (9352)	1 U.L.
A, B, C, D	Excess 3 Inputs (9353)	1 U.L.
A, B, C, D	Excess 3 Gray Inputs (9354)	1 U.L.
$\overline{0}$ to $\overline{9}$	Decimal Output	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

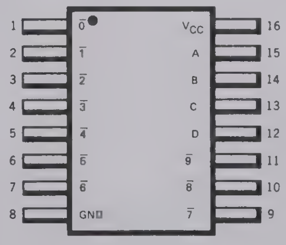
CONNECTION DIAGRAM
DIP (TOP VIEW)


1 $\overline{0}$
2 $\overline{1}$
3 $\overline{2}$
4 $\overline{3}$
5 $\overline{4}$
6 $\overline{5}$
7 $\overline{6}$
8 GND
16 V_{CC}
15 A
14 B
13 C
12 D
11 $\overline{9}$
10 $\overline{8}$
9 $\overline{7}$

LOGIC DIAGRAM
9352/5442, 7442 BCD-TO-DECIMAL


INPUT
A
B
C
D
$\overline{0}$
$\overline{1}$
$\overline{2}$
$\overline{3}$
$\overline{4}$
$\overline{5}$
$\overline{6}$
$\overline{7}$
$\overline{8}$
$\overline{9}$
OUTPUT

FLATPAK (TOP VIEW)

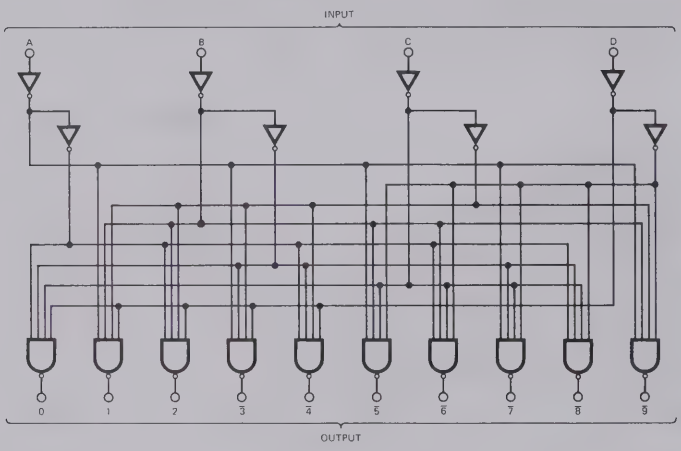

1 $\overline{0}$
2 $\overline{1}$
3 $\overline{2}$
4 $\overline{3}$
5 $\overline{4}$
6 $\overline{5}$
7 $\overline{6}$
8 GND
16 V_{CC}
15 A
14 B
13 C
12 D
11 $\overline{9}$
10 $\overline{8}$
9 $\overline{7}$

Positive logic: See truth table.

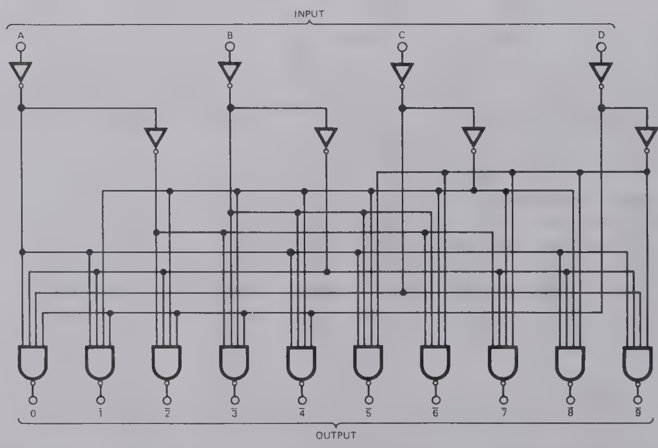
TRUTH TABLES

9352/5442, 7442 BCD INPUT				9353/5443, 7443 EXCESS 3 INPUT				9354/5444, 7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

LOGIC DIAGRAM
9353/5443, 7443 EXCESS 3-TO-DECIMAL



LOGIC DIAGRAM
9354/5444, 7444 EXCESS 3 GRAY-TO-DECIMAL



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9352XM/5442XM 9353XM/5443XM, 9354XM/5444XM			9352XC/7442XC 9353XC/7443XC, 9354XC/7444XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		1 & 2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IH} = 2.0 V V_{IL} = 0.8 V		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V V_{IL} = 0.8 V		1
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	Each Input	4
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9352/5442, 9353/5443, 9354/5444	V_{CC} = MAX.	5
		−18		−55	mA	9352/7442, 9353/7443, 9354/7444		
I_{CC}	Supply Current		28	41	mA	9352/5442, 9353/5443, 9354/5444	V_{CC} = MAX.	4
			28	56	mA	9352/7442, 9353/7443, 9354/7444		

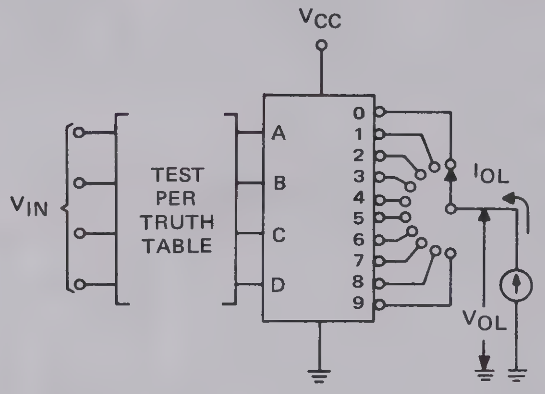
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PHL}	Turn On Delay Input to Output (Through Two Logic Levels)	10	22	30	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output (Through Three Logic Levels)		23	35			
t_{PLH}	Turn Off Delay Input to Output (Through Two Logic Levels)	10	17	25	ns		A
t_{PLH}	Turn Off Delay Input to Output (Through Three Logic Levels)		26	35			

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

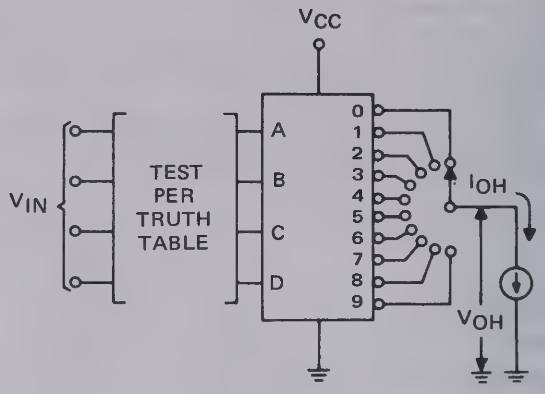
DC TEST CIRCUITS*

PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{IN}
TEST PER TRUTH TABLE
A
B
C
D
0
1
2
3
4
5
6
7
8
9
I_{OL}
V_{OL}

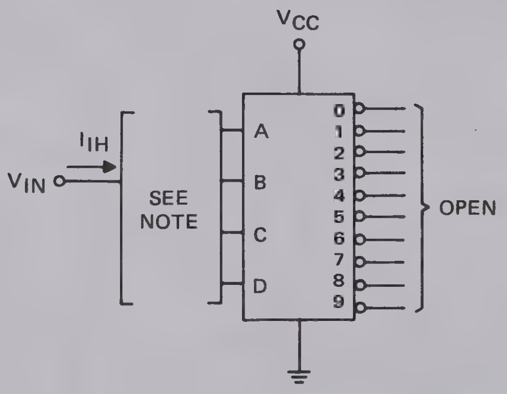
1. Each input is tested separately.

Fig. 1


V_{CC}
V_{IN}
TEST PER TRUTH TABLE
A
B
C
D
0
1
2
3
4
5
6
7
8
9
I_{OH}
V_{OH}

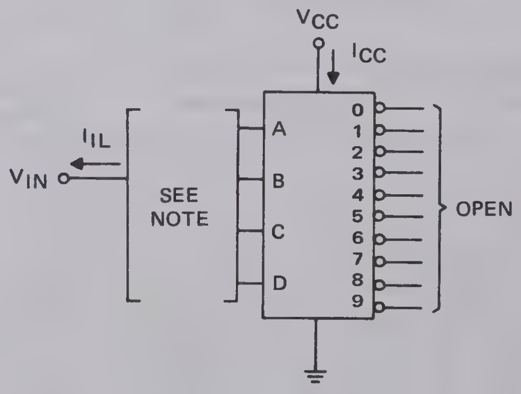
1. Each output is tested separately.

Fig. 2


V_{CC}
I_{IH}
V_{IN}
SEE NOTE
A
B
C
D
0
1
2
3
4
5
6
7
8
9
OPEN

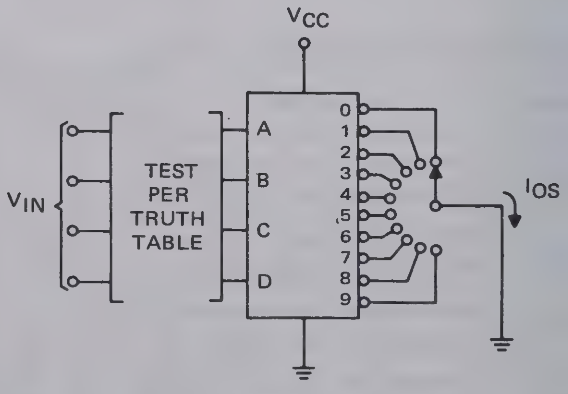
1. Each output is tested separately.

Fig. 3


V_{CC}
I_{CC}
I_{IL}
V_{IN}
SEE NOTE
A
B
C
D
0
1
2
3
4
5
6
7
8
9
OPEN

1. When testing I_{IL} each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

Fig. 4


V_{CC}
V_{IN}
TEST PER TRUTH TABLE
A
B
C
D
0
1
2
3
4
5
6
7
8
9
I_{OS}

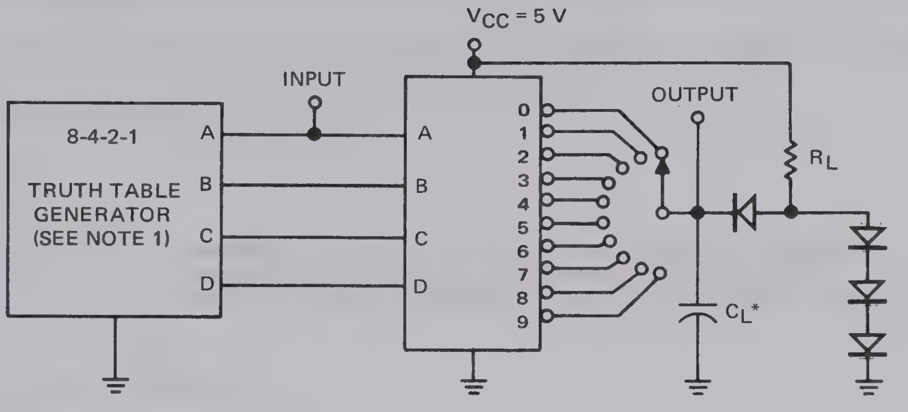
1. Each output is tested separately.

Fig. 5

*Arrows indicate actual direction of current flow.

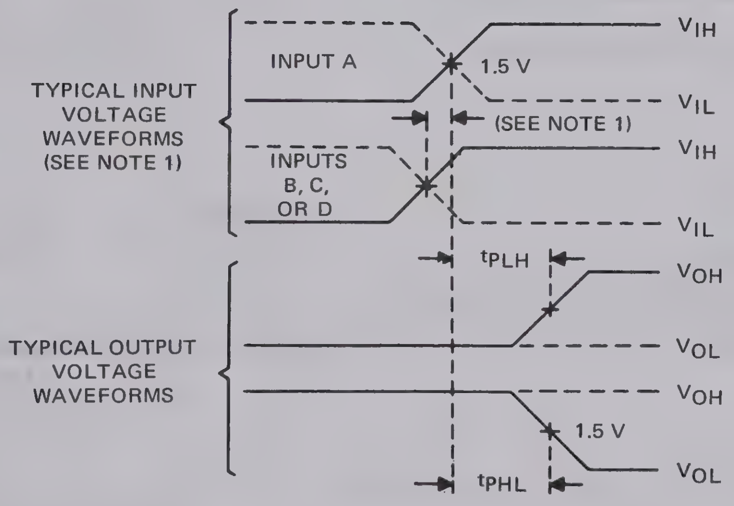
PARAMETER MEASUREMENT INFORMATION (Con't.)

SWITCHING CHARACTERISTICS


$V_{CC} = 5$ V
INPUT
OUTPUT
8-4-2-1
TRUTH TABLE GENERATOR (SEE NOTE 1)
A
B
C
D
0
1
2
3
4
5
6
7
8
9
R_L
C_L*

*C_L includes probe and jig capacitance.

TEST CIRCUIT


TYPICAL INPUT VOLTAGE WAVEFORMS (SEE NOTE 1)
INPUT A
1.5 V
V_{IH}
V_{IL}
(SEE NOTE 1)
INPUTS B, C, OR D
V_{IH}
V_{IL}
t_{PLH}
TYPICAL OUTPUT VOLTAGE WAVEFORMS
V_{OH}
V_{OL}
V_{OH}
1.5 V
V_{OL}
t_{PHL}

VOLTAGE WAVEFORMS

NOTE:

1. The truth table generator has the following characteristics: $V_{OH} \geqslant 2.4$ V, $V_{OL} \leqslant 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Input B, C, and D transitions occur simultaneously with or prior to input A transitions.

Fig. A SWITCHING TIMES

TTL/MSI 9356
4-BIT BINARY COUNTER

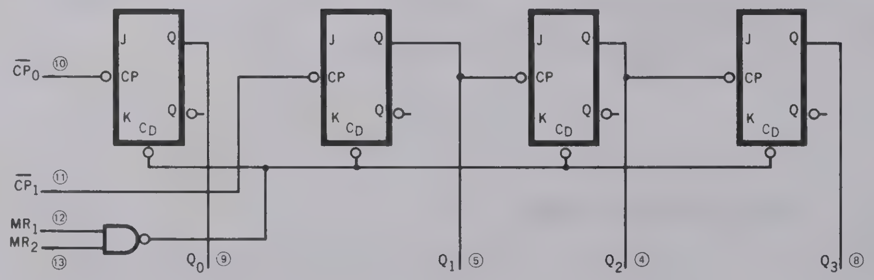
DESCRIPTION — The TTL/MSI 9356 is a monolithic 4-Bit Binary Counter. This device is capable of being used as a divided-by-two, divided-by-eight or a divided-by-sixteen counter. It is useful in a large number of counting applications in digital computer systems, data handling systems and control systems.

- **FUNCTIONALLY EQUIVALENT TO THE 7493**
- **STANDARD CORNER POWER PINS FOR EASY USE**
- **HIGH SPEED, 18 MHz TYPICAL**
- **TYPICAL POWER DISSIPATION OF 160 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL COMPATIBLE**
- **ALL CERAMIC, HERMETIC 14-LEAD DUAL IN-LINE PACKAGE**

PIN NAMES		**LOADING** (Note a)
$\overline{CP}_0$	Clock First Stage Negative Edge Input	2 U.L.
$\overline{CP}_1$	Clock Second, Third, and Fourth Stage Negative Edge Input	2 U.L.
MR	"AND" Master Reset to Binary Zero (Asynchronous) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Counter Outputs (Note b)	10 U.L.

NOTES:
(a) 1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
(b) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

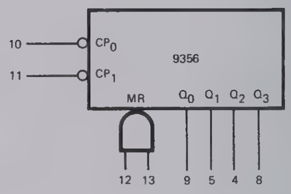
LOGIC DIAGRAM



CP0 ⑩
CP1 ⑪
MR1 ⑫
MR2 ⑬
J
Q
CP
K
CD
Q0 ⑨
Q1 ⑤
Q2 ④
Q3 ⑧

○ = Pin Numbers

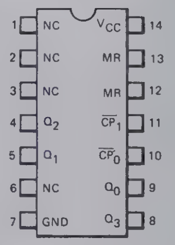
LOGIC SYMBOL



10
11
CP0
CP1
9356
MR
Q0 Q1 Q2 Q3
12 13
9 5 4 8

V_{CC} = Pin 14
Gnd = Pin 7
NC = Pins 1, 2, 3, 6

CONNECTION DIAGRAM
DIP (TOP VIEW)



1 NC
2 NC
3 NC
4 Q2
5 Q1
6 NC
7 GND
14 VCC
13 MR
12 MR
11 CP1
10 CP0
9 Q0
8 Q3

NC — No Internal Connection

FUNCTIONAL DESCRIPTION – The MSI 9356 is an 4-bit up binary counter. It consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated "AND" master reset is provided to inhibit the counting and return all outputs to a LOW state.* Since the output from the first flip-flop is not internally connected to the succeeding flip-flops, the device may be operated in two independent modes:

A. 4-Bit Ripple Counter – The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter – The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

*(i.e., When both inputs of the "AND" master reset are HIGH outputs $Q_{0\text{-}3}$ will be forced LOW, resetting the flip-flops, regardless of all other input conditions.)

NOTE: The 9356 flip-flops change state after the HIGH to LOW transition of the clock.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care Condition

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	0	25	75	°C
Normalized Fan Out from Each Output, N			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9356XC*)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS & COMMENTS
		MIN.	TYP. Note 4	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold for All Inputs
V_{OH}	Output HIGH Voltage	2.4	3.0		Volts	V_{CC} = 4.75 V, I_{OH} = –800 µA
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = 4.75 V, I_{OL} = 16 mA
I_{IH}	Input HIGH Current, MR		10	40	µA	V_{CC} = 5.25 V, V_{IN} = 2.4 V
	$\overline{CP}_0$, $\overline{CP}_1$		20	80		
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = 5.25 V, V_{IN} = 5.5 V
I_{IL}	Input LOW Current, MR		–1.0	–1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.4 V
	$\overline{CP}_0$, $\overline{CP}_1$		–2.0	–3.2		
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	–18		–57	mA	V_{CC} = 5.25 V, V_{OUT} = 0V
I_{CC}	Power Supply Current		30	53	mA	V_{CC} = 5.25 V

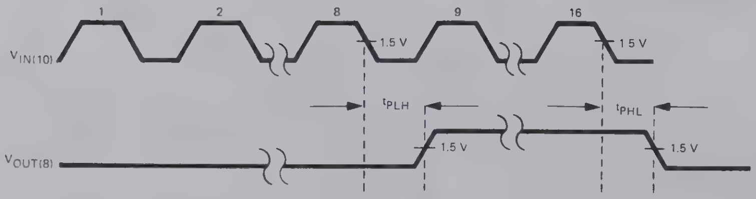
*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating range.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{PLH}	Turn-Off Delay $\overline{CP}_0$ to Output Q_3		75	135	ns	V_{CC} = 5.0 V, C_L = 15 pF Q_0 Output Connected To $\overline{CP}_1$ Input
t_{PHL}	Turn-On Delay $\overline{CP}_0$ to Output Q_3		75	135	ns	
f_{max}	Maximum Frequency of Input Count Pulses	10	18		MHz	

SWITCHING TIME WAVEFORMS



TTL/MSI 9357A/5446, 7446
9357B/5447, 7447
BCD TO 7-SEGMENT DECODER/DRIVER

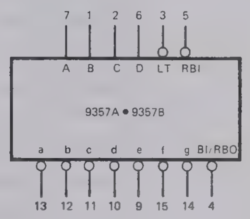
DESCRIPTION – The 9357A/5446, 7446 and 9357B/5447, 7447 are TTL, BCD to 7-segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the 9357A/5446, 7446; 9357B/5447, 7447 are designed to withstand the relatively high voltages required for 7-segment indicators. The 9357A/5446, 7446 outputs will withstand 30 V and the 9357B/5447, 7447 outputs will withstand 15 V with a maximum reverse current of 250 μA. Indicator segments requiring up to 20 mA of current may be driven directly from the 9357A/5446, 7446 or 9357B/5447, 7447 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The 9357A/5446, 7446; 9357B/5447, 7447 incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{\text{RBI}}$ and $\overline{\text{RBO}}$). Lamp test ($\overline{\text{LT}}$) of these types may be performed at any time when the $\overline{\text{BI}}/\overline{\text{BRO}}$ node is a HIGH level. Both contain an overriding blanking input ($\overline{\text{BI}}$) which can be used to control the lamp intensity or to inhibit the outputs.

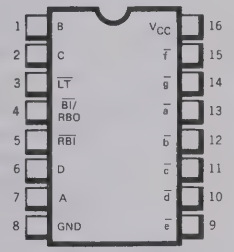
PIN NAMES		LOADING
A, B, C, D	BCD Inputs	1 U.L.
$\overline{\text{RBI}}$	Ripple Blanking Input	1 U.L.
$\overline{\text{LT}}$	Lamp Test Input	1 U.L.
$\overline{\text{BI}}/\overline{\text{RBO}}$	Blanking Input or	2.6 U.L.
	Ripple Blanking Output	5 U.L.
$\overline{a}$, to $\overline{g}$	Outputs	12.5 U.L.

LOGIC SYMBOL

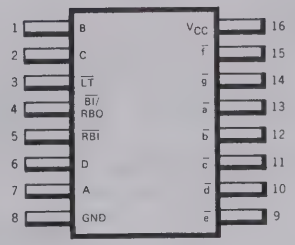

7 1 2 6 3 5
A B C D LT RBI
9357A • 9357B
a b c d e f g BI/RBO
13 12 11 10 9 15 14 4

V_{CC} = Pin 16
GND = Pin 8
9357A/5446, 7446
9357B/5447, 7447

CONNECTION DIAGRAM
DIP (TOP VIEW)

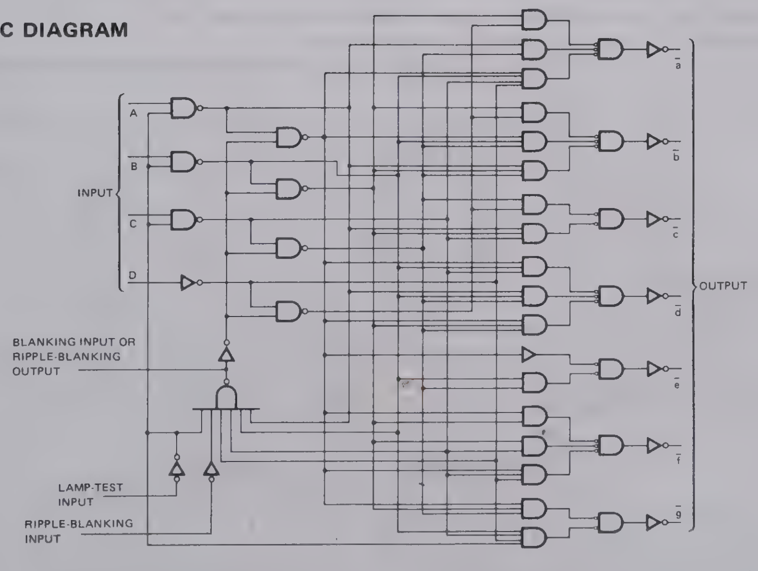

1 B
2 C
3 LT
4 BI/RBO
5 RBI
6 D
7 A
8 GND
16 VCC
15 f
14 g
13 a
12 b
11 c
10 d
9 e

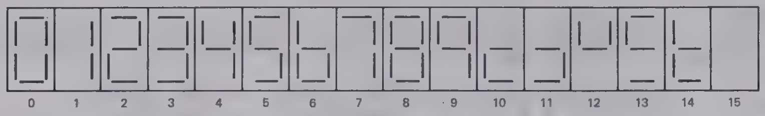
FLATPAK (TOP VIEW)


1 B
2 C
3 LT
4 BI/RBO
5 RBI
6 D
7 A
8 GND
16 VCC
15 f
14 g
13 a
12 b
11 c
10 d
9 e

Positive logic: See truth table.

LOGIC DIAGRAM


A
B
C
D
INPUT
OUTPUT
a
b
c
d
e
f
g
BLANKING INPUT OR RIPPLE-BLANKING OUTPUT
LAMP-TEST INPUT
RIPPLE-BLANKING INPUT



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE

	INPUTS						OUTPUTS								
DECIMAL OR FUNCTION	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	D	C	B	A	$\overline{\text{BI}}/\overline{\text{RBO}}$	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
$\overline{\text{LT}}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

NOTES:

(A) $\overline{\text{BI}}/\overline{\text{RBO}}$ is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output ($\overline{\text{RBO}}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{\text{RBI}}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output ($\overline{\text{BI}}/\overline{\text{RBO}}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9357AXM/5446XM 9357BXM/5447XM			9357AXC/7446XC 9357BXC/7447XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 3)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out From Outputs $\bar{a}$ through $\bar{g}$ to Series 54/74 Loads				24			24	
Normalized Fan Out From $\overline{\text{BI}}/\overline{\text{RBO}}$ Node to Series 54/74 Loads				5.0			5.0	
Output Sink Current, I_{OL}:	Outputs $\bar{a}$ through $\bar{g}$			40			40	mA
	$\overline{\text{BI}}/\overline{\text{RBO}}$ Node			8.0			8.0	mA

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

PARAMETER	9357A/5446, 7446			9357B/5447, 7447			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Continuous Voltage at Outputs $\bar{a}$ through $\bar{g}$			30			15	Volts

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	1 & 2
V_{on}	On-State Output Voltage at Outputs $\overline{a}$ through $\overline{g}$		0.3	0.4	Volts	V_{CC} = MIN., I_{OL} = 40 mA	1
V_{OL}	Output LOW Voltage at $\overline{\text{BI/RBO}}$ Node		0.3	0.4	Volts	V_{CC} = MIN., I_{OL} = 8.0 mA	1
V_{off}	Off-State Output Voltage at Outputs $\overline{a}$ through $\overline{g}$	30			Volts	9357A/5446, 7446 V_{CC} = MAX., I_{off} = 250 µA	2
V_{off}	Off-State Output Voltage at Outputs $\overline{a}$ through $\overline{g}$	15			Volts	9357B/5447, 7447 V_{CC} = MAX., I_{off} = 250 µA	2
V_{OH}	Output HIGH Voltage at $\overline{\text{BI/RBO}}$ Node	2.4	3.7		Volts	V_{CC} = MIN., I_{OH} = −0.2 mA	2
I_{IL}	Input LOW Current at Any Input Except $\overline{\text{BI/RBO}}$ Node			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	3
	Input LOW Current at $\overline{\text{BI/RBO}}$ Node			−4.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	3
I_{IH}	Input HIGH Current at Any Input Except $\overline{\text{BI/RBO}}$ Node			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{OS}	Output Short Circuit Current at $\overline{\text{BI/RBO}}$ Node			−4.0	mA	V_{CC} = MAX.	5
I_{CC}	Supply Current		64	85	mA	9357A/5446, 9357B/5447 V_{CC} = MAX.	4
			64	103	mA	9357A/7446, 9357B/7447	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) These voltage values are with respect to network ground terminal.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output A Input to Any Output			100	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 120Ω	A
t_{PHL}	Turn On Delay Input to Output A Input to Any Output			100	ns		A
t_{PLH}	Turn Off Delay Input to Output $\overline{\text{RBI}}$ Input to Any Output			100	ns		A
t_{PHL}	Turn On Delay Input to Output $\overline{\text{RBI}}$ Input to Any Output			100	ns		A

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

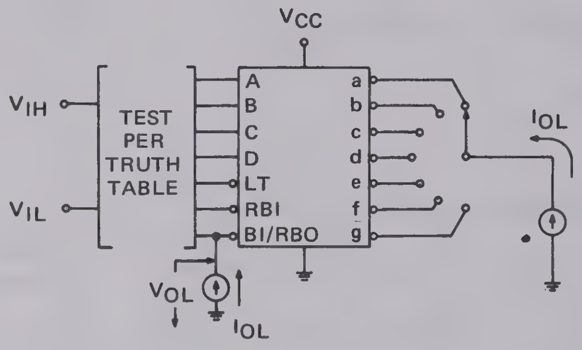

VCC
VIH
VIL
TEST PER TRUTH TABLE
A
B
C
D
LT
RBI
BI/RBO
a
b
c
d
e
f
g
IOL
VOL
IOL

Fig. 1

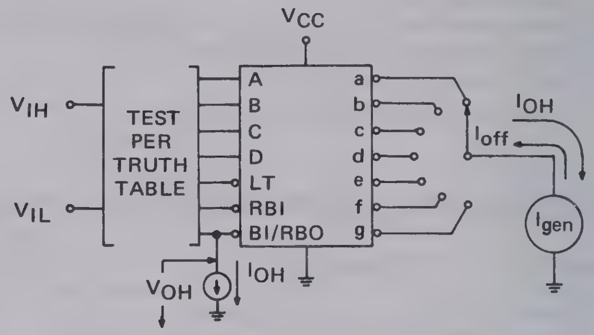
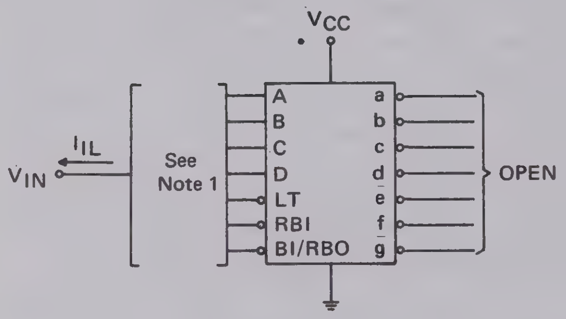
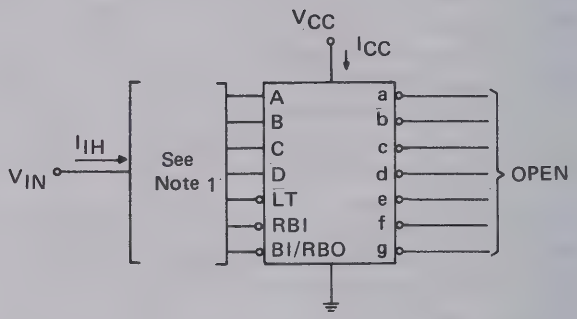

VCC
VIH
VIL
TEST PER TRUTH TABLE
A
B
C
D
LT
RBI
BI/RBO
a
b
c
d
e
f
g
IOH
Ioff
Igen
VOH
IOH

Fig. 2


VCC
IIL
VIN
See Note 1
A
B
C
D
LT
RBI
BI/RBO
a
b
c
d
e
f
g
OPEN

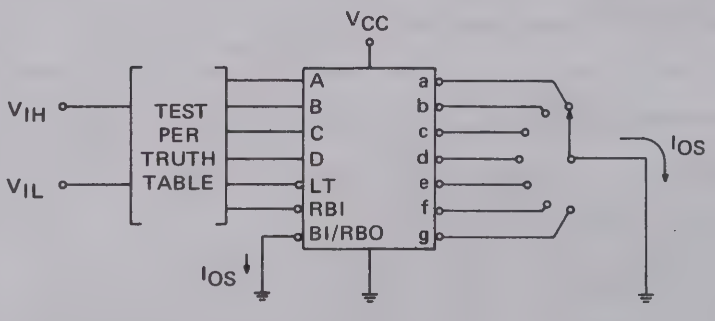
1. Each input is tested separately.

Fig. 3


VCC
ICC
IIH
VIN
See Note 1
A
B
C
D
LT
RBI
BI/RBO
a
b
c
d
e
f
g
OPEN

1. Each input is tested separately for I_{IH}.

Fig. 4


VCC
VIH
VIL
TEST PER TRUTH TABLE
A
B
C
D
LT
RBI
BI/RBO
a
b
c
d
e
f
g
IOS
IOS

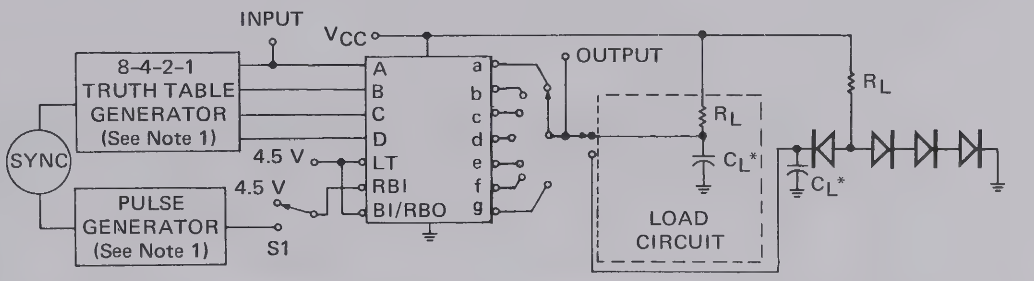
1. Each output is tested separately.

Fig. 5

*Arrows indicate actual direction of current flow. Logic symbol used is representative for all types.

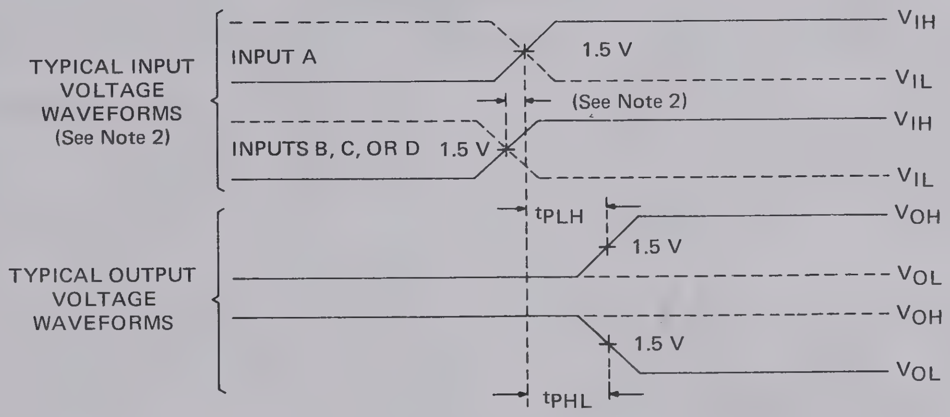
PARAMETER MEASUREMENT INFORMATION (con't.)

SWITCHING CHARACTERISTICS

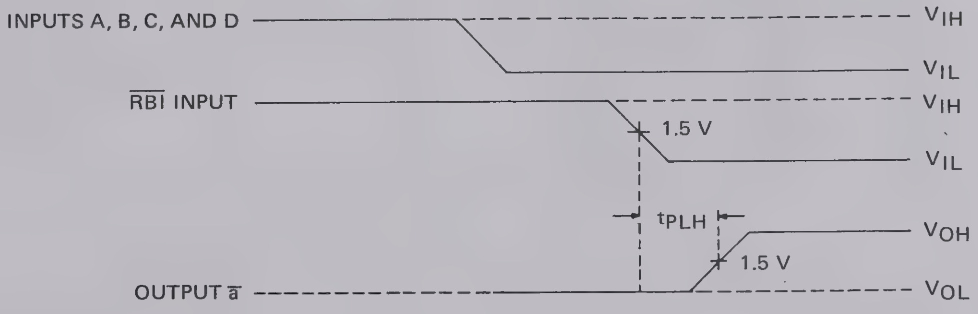

INPUT
VCC
8-4-2-1 TRUTH TABLE GENERATOR (See Note 1)
SYNC
PULSE GENERATOR (See Note 1)
4.5 V
4.5 V
S1
A
B
C
D
LT
RBI
BI/RBO
a
b
c
d
e
f
g
OUTPUT
RL
CL*
LOAD CIRCUIT
RL
CL*

*C_L includes probe and jig capacitance.

TEST CIRCUIT


TYPICAL INPUT VOLTAGE WAVEFORMS (See Note 2)
INPUT A
1.5 V
VIH
VIL
(See Note 2)
INPUTS B, C, OR D
1.5 V
VIH
VIL
TYPICAL OUTPUT VOLTAGE WAVEFORMS
tPLH
1.5 V
VOH
VOL
VOH
1.5 V
VOL
tPHL

VOLTAGE WAVEFORMS – A INPUT TO OUTPUTS


INPUTS A, B, C, AND D
VIH
VIL
RBI INPUT
VIH
1.5 V
VIL
tPLH
VOH
1.5 V
OUTPUT a
VOL

VOLTAGE WAVEFORMS – RBI INPUT TO OUTPUTS

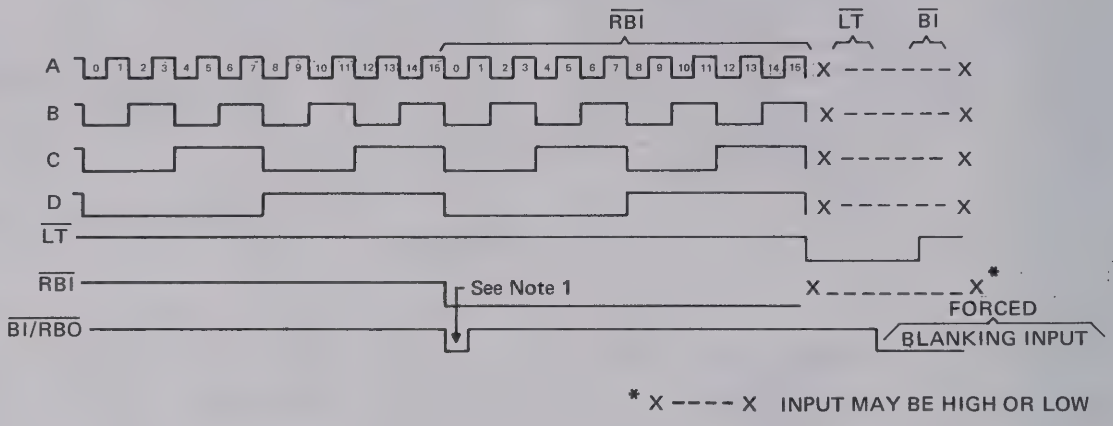
NOTES:

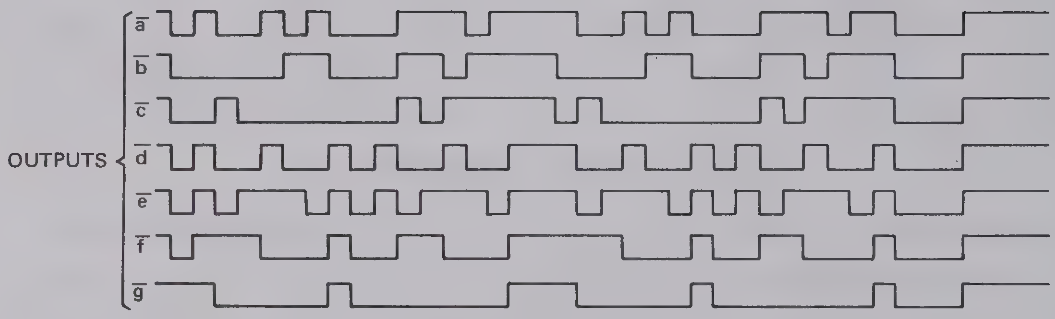
1. The truth table generator and pulse generator have the following characteristics: $V_{OH} \geq 2.4$ V, $V_{OL} \leq 0.4$ V, t_r and $t_f \leq 10$ ns, and PRR = 1 MHz.
2. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. $\overline{RBI}$ = 4.5 V.

Fig. A SWITCHING TIMES

TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS

SWITCHING CHARACTERISTICS (Continued)


$\overline{RBI}$
$\overline{LT}$
$\overline{BI}$
A
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
X ------- X
B
X ------- X
C
X ------- X
D
X ------- X
$\overline{LT}$
$\overline{RBI}$
See Note 1
X --------- X*
$\overline{BI}/\overline{RBO}$
FORCED
BLANKING INPUT
* X ---- X INPUT MAY BE HIGH OR LOW


OUTPUTS
$\overline{a}$
$\overline{b}$
$\overline{c}$
$\overline{d}$
$\overline{e}$
$\overline{f}$
$\overline{g}$

NOTE:

1. This LOW level represents the $\overline{RBO}$ response.

TTL/MSI 9358/5448, 7448
9359/5449, 7449
BCD TO 7-SEGMENT DECODER

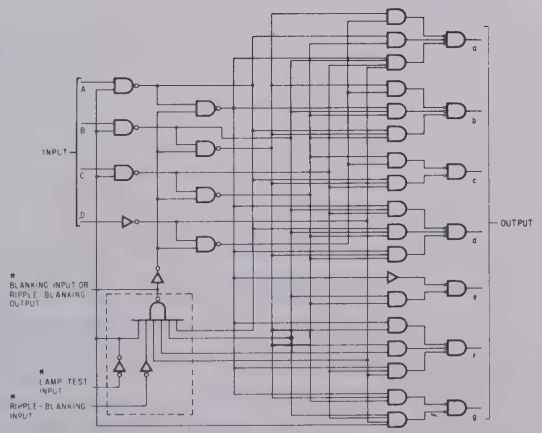
DESCRIPTION — The 9358/5448, 7448 and 9359/5449, 7449 are TTL, BCD to 7-Segment Decoders consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. The 9358/5448, 7448 offers active HIGH, open-collector outputs for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input for the 9358/5448, 7448. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the 9359/5449, 7449.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs are shown in the truth tables.

The 9358/5448, 7448 circuit incorporates automatic leading and/or trailing edge zero-blanking control ($\overline{\text{RBI}}$ and $\overline{\text{RBO}}$). Lamp test ($\overline{\text{LT}}$) of these types may be performed at any time when the $\overline{\text{BI}}/\overline{\text{RBO}}$ node is a HIGH level. They contain an overriding blanking input ($\overline{\text{BI}}$) which can be used to control the lamp intensity or to inhibit the outputs.

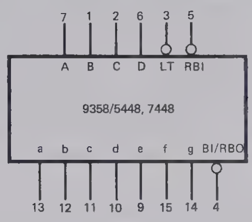
PIN NAMES		LOADING
A, B, C, D	BCD Inputs	1 U.L.
$\overline{\text{RBI}}$	Ripple Blanking Input	1 U.L.
$\overline{\text{LT}}$	Lamp Test Input	1 U.L.
$\overline{\text{BI}}/\overline{\text{RBO}}$	Blanking Input or	2.6 U.L.
	Ripple Blanking Output	5 U.L.
$\overline{\text{BI}}$	Blanking Input	1 U.L.
a to g	Outputs	6 U.L.

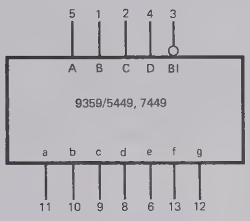
LOGIC DIAGRAM


A
B
INPUT
C
D
*
BLANKING INPUT OR
RIPPLE BLANKING
OUTPUT
*
LAMP TEST
INPUT
*
RIPPLE-BLANKING
INPUT
a
b
c
d
e
f
g
OUTPUT

* NOT INCLUDED WITH THE 9359/5449

LOGIC SYMBOL

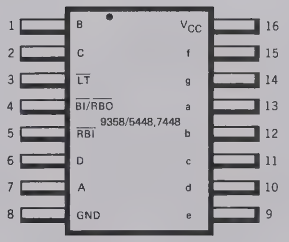

7
1
2
6
3
5
A
B
C
D
LT
RBI
9358/5448, 7448
a
b
c
d
e
f
g
BI/RBO
13
12
11
10
9
15
14
4

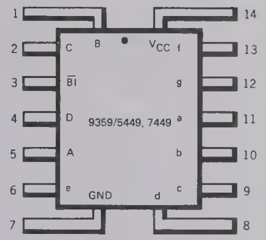

5
1
2
4
3
A
B
C
D
BI
9359/5449, 7449
a
b
c
d
e
f
g
11
10
9
8
6
13
12

V_{CC} = Pin 16
GND = Pin 8

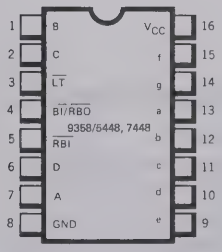
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
FLATPAKS (TOP VIEW)

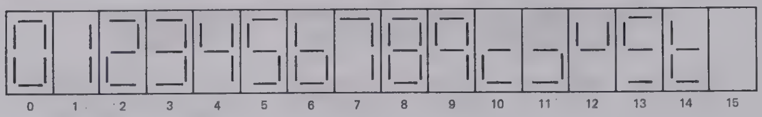

1
2
3
4
5
6
7
8
B
C
LT
BI/RBO
RBI
D
A
GND
9358/5448,7448
VCC
f
g
a
b
c
d
e
16
15
14
13
12
11
10
9


1
2
3
4
5
6
7
C
B
VCC
f
BI
g
D
9359/5449, 7449
a
A
b
e
GND
d
c
14
13
12
11
10
9
8

DIP (TOP VIEW)


1
2
3
4
5
6
7
8
B
C
LT
BI/RBO
9358/5448, 7448
RBI
D
A
GND
VCC
f
g
a
b
c
d
e
16
15
14
13
12
11
10
9

Positive logic: See truth table



NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

TRUTH TABLE 9358/5448, 7448

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	a	b	c	d	e	f	g	NOTE
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{RBI}$	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
$\overline{LT}$	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:

(1) $\overline{BI}/\overline{RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X=input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

(3) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp-test input, all segment outputs go to a LOW level.

TRUTH TABLE 9359/5449, 7449

	INPUTS					OUTPUTS							
DECIMAL OR FUNCTION	D	C	B	A	$\overline{BI}$	a	b	c	d	e	f	g	NOTE
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	L	L	L	L	L	L	L	L	2

NOTES:

(1) The blanking input must be open or held at a HIGH level when output functions 0 through 15 are desired.

(2) When a LOW level is applied to the blanking input all segment outputs go to a LOW level regardless of the state of any other input condition. X = input may be HIGH or LOW.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9358XM/5448XM 9359XM/5449XM			9358XC/7448XC 9359XC/7449XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 3)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

PARAMETER		9358/5448, 7448			9359/5449, 7449			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Continuous Voltage at Outputs a through g							5.5	Volts
Normalized Fan Out From Outputs a through g to Series 54/74 Loads				4.0			6.0	
Normalized Fan Out From $\overline{BI}/\overline{RBO}$ Node to Series 54/74 Loads				5.0				
Output Sink Current, I_{OL}:	Outputs a through g			6.4			10	mA
	$\overline{BI}/\overline{RBO}$ Node			8.0				mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts			1 & 2
V_{IL}	Input LOW Voltage			0.6	Volts	9359/5449		1 & 2
				0.8		9358/5448, 7448; 9359/7449		
V_{on}	On-State Output Voltage		0.27	0.4	Volts	9359/5449, 7449	V_{CC} = MIN. I_{OL} = MAX.	1
V_{OL}	Output LOW Voltage		0.27	0.4	Volts	9358/5448, 7448	V_{CC} = MIN. I_{OL} = MAX.	1
V_{off}	Off-State Output Voltage	5.5			Volts	9359/5449, 7449	V_{CC} = MAX. I_{off} = 0.25 mA	2
V_{OH}	Output HIGH Voltage at $\overline{BI}/\overline{RBO}$ Node	2.4	3.7		Volts	9358/5448, 7448	V_{CC} = MIN. I_{OH} = –0.2 mA	2
	Output HIGH Voltage at Outputs a through g	2.4	4.2		Volts	9358/5448, 7448	V_{CC} = MIN. I_{OH} = –0.4 mA	2
I_{OH}	Output HIGH Current at Outputs a through g	–1.3	–2.0		mA	9358/5448, 7448	V_{CC} = MIN. V_{OUT} = 0.85 V	2
I_{IL}	Input LOW Current at Any Input Except $\overline{BI}/\overline{RBO}$ Node of 9358/5448, 7448			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at $\overline{BI}/\overline{RBO}$ Node			–4.2	mA	9358/5448, 7448	V_{CC} = MAX. V_{IN} = 0.4 V	3
I_{IH}	Input HIGH Current at Any Input Except $\overline{BI}/\overline{RBO}$ Node of 9358/5448, 7448			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V		4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{OS}	Output Short Circuit Current at Any Output Except Outputs a through g 9359/5449, 7449			–4.0	mA	V_{CC} = MAX.		5
I_{CC}	Supply Current		53	76	mA	9358/5448	V_{CC} = MAX.	4
			53	90	mA	9358/7448		
			33	47	mA	9359/5449		
			33	56	mA	9359/7449		

SWITCHING CHARACTERISTICS (T_A = 25°C)

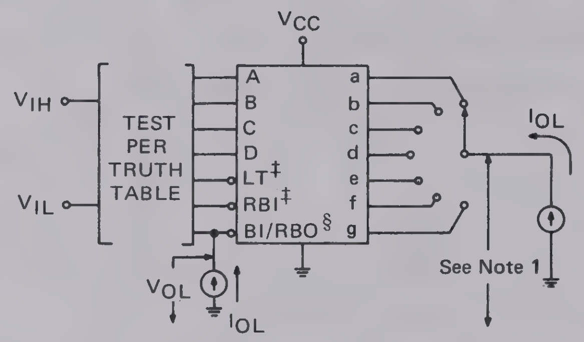
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output A Input to Any Output			100	ns	V_{CC} = 5.0 V C_L = 15 pF R_L*	A
t_{PHL}	Turn On Delay Input to Output A Input to Any Output			100	ns		A
t_{PLH}	Turn Off Delay Input to Output $\overline{RBI}$ Input to Any Output			100	ns		A
t_{PHL}	Turn On Delay Input to Output $\overline{RBI}$ Input to Any Output			100	ns		A

*R_L = 1 kΩ for 9358/5448 and 9359/5449; R_L = 667Ω for 9358/7448 and 9359/7449.

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) These voltage values are with respect to network ground terminal.

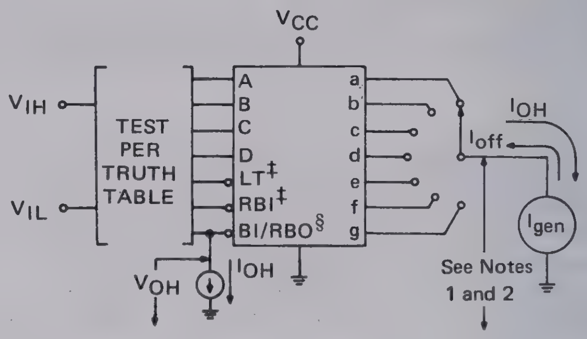
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*


VCC
VIH
VIL
TEST PER TRUTH TABLE
A
B
C
D
LT‡
RBI‡
BI/RBO§
a
b
c
d
e
f
g
IOL
See Note 1
VOL
IOL

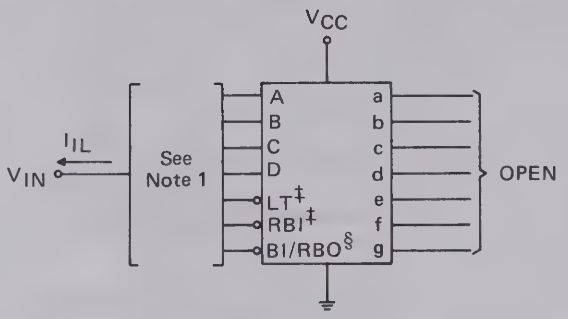
1. Measure V_{on} for 9359/5449, 7449.
   Measure V_{OL} for 9358/5448, 7448.

Fig. 1


VCC
VIH
VIL
TEST PER TRUTH TABLE
A
B
C
D
LT‡
RBI‡
BI/RBO§
a
b
c
d
e
f
g
IOH
Ioff
Igen
See Notes 1 and 2
VOH
IOH

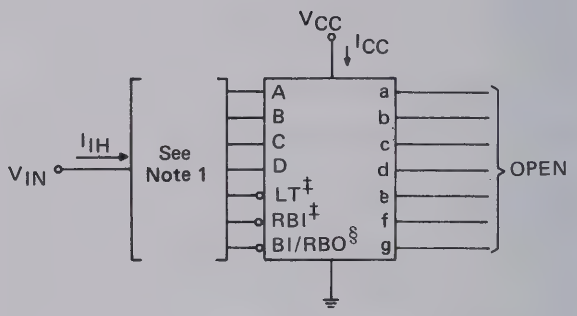
1. Measure V_{off} for 9359/5449, 7449.
2. Measure V_{OH} for 9358/5448, 7448.

Fig. 2


VCC
IIL
VIN
See Note 1
A
B
C
D
LT‡
RBI‡
BI/RBO§
a
b
c
d
e
f
g
OPEN

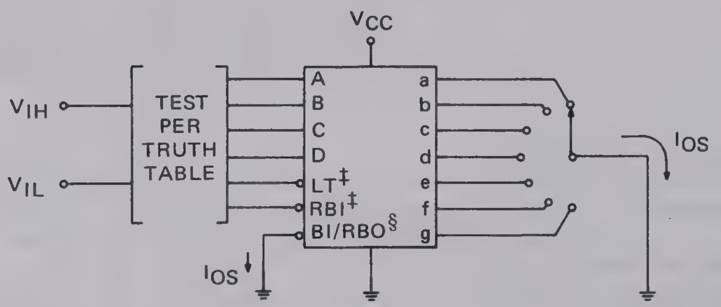
1. Each input is tested separately.

Fig. 3


VCC
ICC
IIH
VIN
See Note 1
A
B
C
D
LT‡
RBI‡
BI/RBO§
a
b
c
d
e
f
g
OPEN

1. Each input is tested separately for I_{IH}.

Fig. 4


VCC
VIH
VIL
TEST PER TRUTH TABLE
A
B
C
D
LT‡
RBI‡
BI/RBO§
a
b
c
d
e
f
g
IOS
IOS

1. Each output is tested separately.

Fig. 5

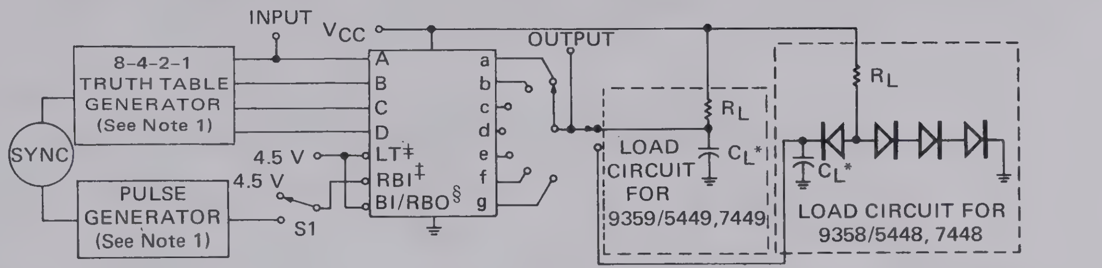
*Arrows indicate actual direction of current flow. Logic symbol used is representative for all types.

‡Available on 9358/5448, 7448 only.

§BI is available on all types. RBO node is available on 9358/5448, 7448 only.

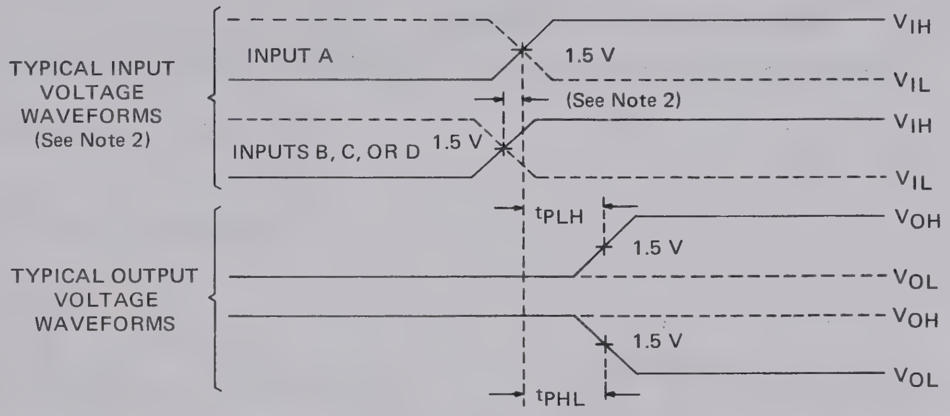
PARAMETER MEASUREMENT INFORMATION (con't.)

SWITCHING CHARACTERISTICS

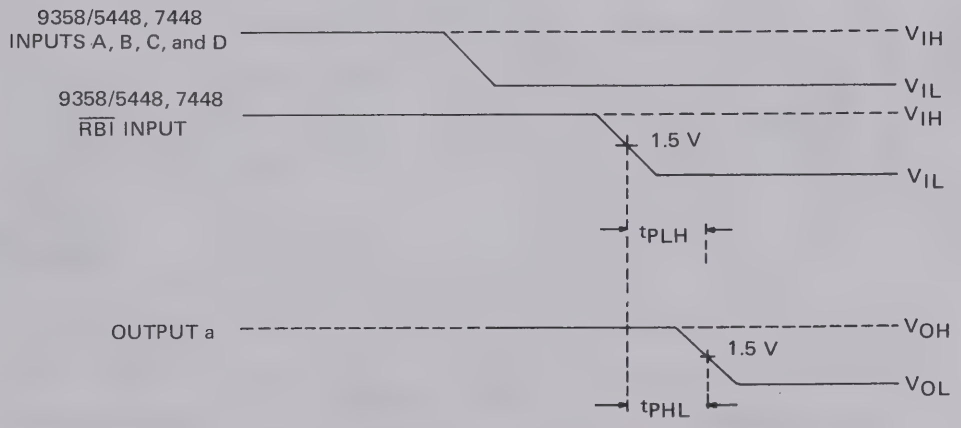

INPUT
V_{CC}
OUTPUT
8-4-2-1 TRUTH TABLE GENERATOR (See Note 1)
SYNC
PULSE GENERATOR (See Note 1)
A
B
C
D
LT‡
RBI‡
BI/RBO§
a
b
c
d
e
f
g
4.5 V
4.5 V
S1
R_L
C_L*
LOAD CIRCUIT FOR 9359/5449,7449
R_L
C_L*
LOAD CIRCUIT FOR 9358/5448, 7448

*C_L includes probe and jig capacitance.

TEST CIRCUIT


TYPICAL INPUT VOLTAGE WAVEFORMS (See Note 2)
INPUT A
1.5 V
V_{IH}
V_{IL}
(See Note 2)
INPUTS B, C, OR D
1.5 V
V_{IH}
V_{IL}
t_{PLH}
TYPICAL OUTPUT VOLTAGE WAVEFORMS
1.5 V
V_{OH}
V_{OL}
V_{OH}
1.5 V
V_{OL}
t_{PHL}

VOLTAGE WAVEFORMS – A INPUT TO OUTPUTS


9358/5448, 7448 INPUTS A, B, C, and D
V_{IH}
V_{IL}
9358/5448, 7448 $\overline{RBI}$ INPUT
V_{IH}
1.5 V
V_{IL}
t_{PLH}
OUTPUT a
V_{OH}
1.5 V
V_{OL}
t_{PHL}

VOLTAGE WAVEFORMS – RBI INPUT TO OUTPUTS

NOTES:

1. The truth table generator and pulse generator have the following characteristics: $V_{OH} \geq 2.4$ V, $V_{OL} \leq 0.4$ V, t_r and $t_f \leq 10$ ns, and PRR = 1 MHz.
2. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. RBI = 4.5 V.

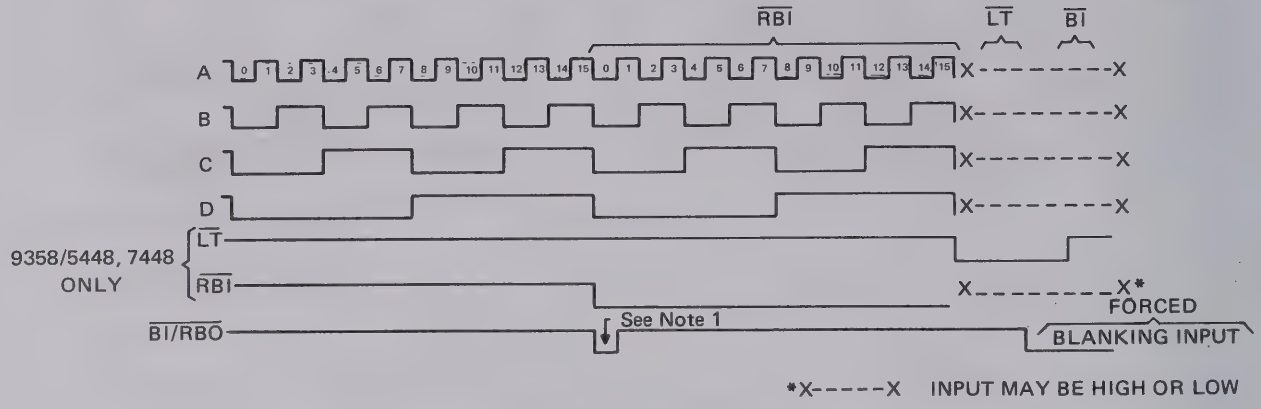
‡Available on 9358/5448, 7448 only.

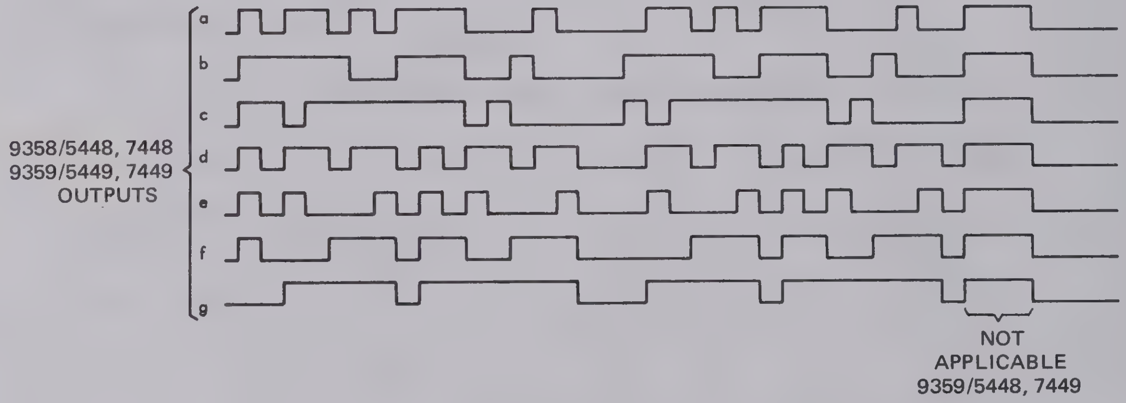
§$\overline{BI}$ is available on all types. $\overline{RBO}$ node is available on 9358/5448, 7448 only.

Fig. A SWITCHING TIMES

TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS

SWITCHING CHARACTERISTICS (Continued)


RBI
LT
BI
A
B
C
D
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
9358/5448, 7448 ONLY
LT
RBI
BI/RBO
See Note 1
FORCED BLANKING INPUT
*X-----X INPUT MAY BE HIGH OR LOW


9358/5448, 7448
9359/5449, 7449
OUTPUTS
a
b
c
d
e
f
g
NOT APPLICABLE 9359/5448, 7449

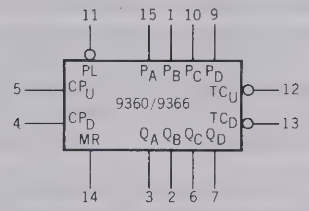
NOTE:

1. For the 9358/5448, 7448 this LOW level represents the $\overline{\text{RBO}}$ response. For the 9359/5449, 7449 a LOW level pulse is applied to the blanking input.

TTL/MSI 9360/54192, 74192
9366/54193, 74193
UP/DOWN DECADE AND BINARY COUNTERS

DESCRIPTION — The TTL/MSI 9360/54192, 74192 is a synchronous Up/Down BCD Decade Counter, and the TTL/MSI 9366/54193, 74193 is a synchronous Up/Down 4-Bit Binary Counter. Both counters have separate up/down clocks, parallel load facility, terminal count outputs for multidecade operation and an asynchronous overriding master reset. The circuits use TTL technology for high speed, and are compatible with the entire Fairchild TTL family.

LOGIC SYMBOL

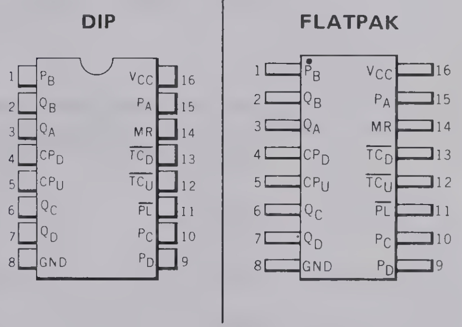

11
15 1 10 9
PL
P_A P_B P_C P_D
5
CP_U
9360/9366
TC_U
12
4
CP_D
TC_D
13
MR
Q_A Q_B Q_C Q_D
14
3 2 6 7

9360/54192, 74192 & 9366/54193, 74193

V_{CC} = Pin 16
GND = Pin 8

- **SYNCHRONOUS OPERATION**
- **CASCADING CIRCUITRY INTERNALLY PROVIDED**
- **PARALLEL LOAD FACILITY**
- **ASYNCHRONOUS MASTER RESET**
- **30MHz TYPICAL COUNT FREQUENCY**
- **TYPICAL POWER DISSIPATION OF 300mW**
- **INPUT CLAMP DIODES**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE**
- **TTL COMPATIBLE**

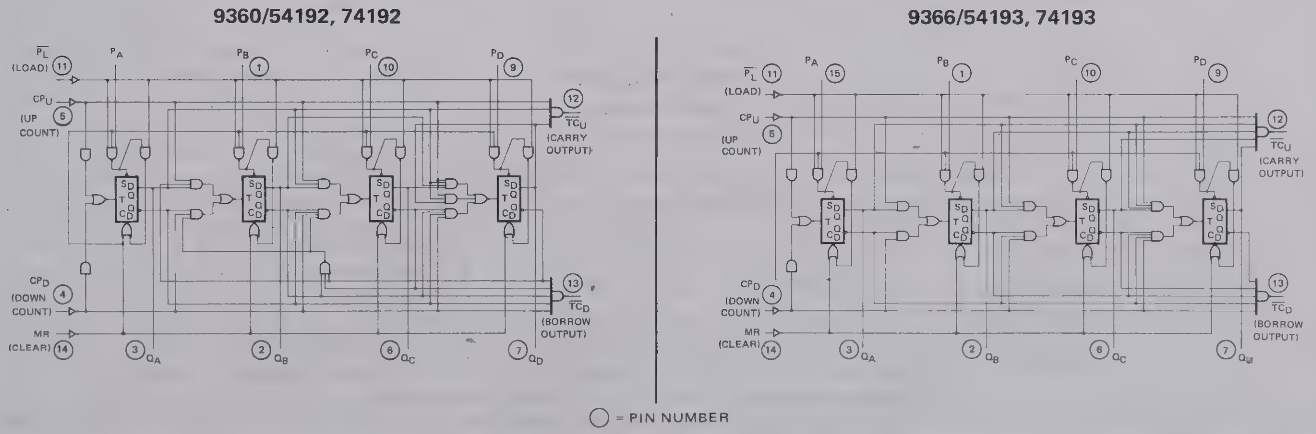
CONNECTION DIAGRAMS
(TOP VIEWS)


DIP
FLATPAK
1 P_B
2 Q_B
3 Q_A
4 CP_D
5 CP_U
6 Q_C
7 Q_D
8 GND
16 V_{CC}
15 P_A
14 MR
13 $\overline{TC_D}$
12 $\overline{TC_U}$
11 $\overline{PL}$
10 P_C
9 P_D

PIN NAMES		LOADING
$\overline{PL}$	Parallel Load (Active LOW) Input	1 U.L.
P_A, P_B, P_C, P_D	Parallel Data Inputs	1 U.L.
CP_U	Count Up Clock Pulse Input	1 U.L.
CP_D	Count Down Clock Pulse Input	1 U.L.
MR	Master Reset (Clear) Input (Asynchronous)	1 U.L.
Q_A, Q_B, Q_C, Q_D	Counter Outputs	10 U.L.
$\overline{TC_U}$	Terminal Count Up (Carry) Output	10 U.L.
$\overline{TC_D}$	Terminal Count Down (Borrow) Output	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAMS


9360/54192, 74192
9366/54193, 74193
$\overline{P_L}$ (LOAD) 11
CP_U (UP COUNT) 5
P_A 15
P_B 1
P_C 10
P_D 9
S_D T Q C_D $\overline{Q}$
12 $\overline{TC_U}$ (CARRY OUTPUT)
13 $\overline{TC_D}$ (BORROW OUTPUT)
CP_D (DOWN COUNT) 4
MR (CLEAR) 14
3 Q_A
2 Q_B
6 Q_C
7 Q_D

○ = PIN NUMBER

FUNCTIONAL DESCRIPTION – The 9360/54192, 74192 and 9366/54193, 74193 can be reset, preset and count up or down. These operating modes of the 9360/54192, 74192 and 9366/54193, 74193 are tabulated in Mode Selection table. The operating modes of the 9360/54192, 74192 and 9366/54193, 74193 are identical; the only difference between the devices is the count sequences.

Counting is synchronous, with the outputs changing state after the LOW to HIGH transition of either the Count-Up Clock (CP_U) or Count-Down Clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is HIGH. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are LOW simultaneously.) Both counters will respond to a clock pulse on either input by changing to the next appropriate state of the count sequence. (The state diagram for the 9360/54192, 74192 shows the regular sequence and in addition shows the sequence of states if a code greater than nine is present in the counter.

Both the 9360/54192, 74192 and the 9366/54193, 74193 have a parallel load (asynchronous) facility which permits the counter to be preset. Whenever the parallel load ($\overline{PL}$) input is LOW, and Master Reset is LOW, the information present on the Parallel Data inputs (P_A, P_B, P_C, P_D) will be loaded into the counters and appear on the outputs independent of the conditions of the clock inputs. When the Parallel Load Input goes HIGH this information is stored in the counters and when the counters are clocked they change to the next appropriate state in the count sequence. The Parallel Data inputs are inhibited when the Parallel Load is HIGH and have no effect on the counters.

The Terminal Count-Up ($\overline{TC}_U$) and Terminal Count-Down ($\overline{TC}_D$) outputs (carry and borrow respectively) allow multidecade counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and terminal count-down clock input of the following counter.

The terminal count-up outputs for the 9360/54192, 74192 and 9366/54193, 74193 are LOW when their count-up clock inputs are LOW and the counters are in state nine and state fifteen respectively. Similarly, the terminal count-down outputs are LOW when their count-down clock inputs are LOW and both counters are in state zero. Thus, when the 9360/54192, 74192 counter is in state nine and the 9366/54193, 74193 counter is in state fifteen and both are counting up, or both counters are in state zero and counting down, a clock pulse will change the counter's state on the rising edge and simultaneously clock the following counter through the appropriate active LOW terminal count output. There are two gate delays per state when these counters are cascaded.

The asynchronous Master Reset input (MR), when HIGH, overrides all input and clears the counters. Master reset overrides parallel load so that when both are activated the counters will be reset. (Obviously, both parallel load and master reset must not be deactivated simultaneously for predictable operation).

9360/54192, 74192 LOGIC EQUATIONS FOR TERMINAL COUNT

$$TC_U = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot \overline{CP_U}$$

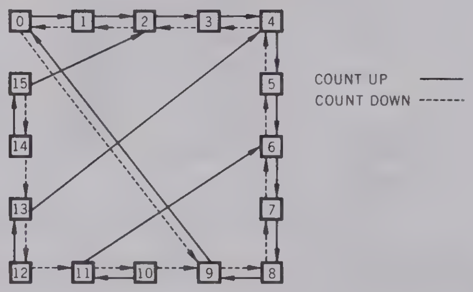
$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

9366/54193, 74193 LOGIC EQUATIONS FOR TERMINAL COUNT

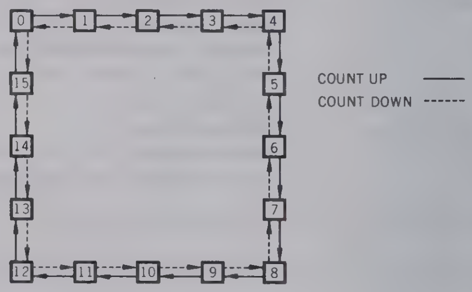
$$TC_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$$

$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

9360/54192, 74192 STATE DIAGRAM



9366/54193, 74193 STATE DIAGRAM



MODE SELECTION
(Both Counters)

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care Condition
CP = Clock Pulse

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9360XM/54192XM; 9366XM/54193XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9360XC/74192XC; 9366XC/74193XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH Threshold voltage for all inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input LOW Threshold voltage for all inputs
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −400µA, V_{IH} = 2.0 V, V_{IL} = 0.8V
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA, V_{IH} = 2.0V, V_{IL} = 0.8V
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 3)	-18		-65	mA	V_{CC} = MAX.
I_{CC}	Power Supply Current		65	102	mA	V_{CC} = MAX.

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0V, 25°C.

(3) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Input Count Frequency		30		MHz	V_{CC} = 5.0V, C_L = 15pF, R_L = 400Ω
t_{PLH}	Turn Off Delay, Count-Up Input (CP_U) to Carry Output ($\overline{TC_U}$)		22	26	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400 Ω
t_{PHL}	Turn On Delay, Count-Up Input (CP_U) to Carry Output ($\overline{TC_U}$)		18	24	ns	
t_{PLH}	Turn Off Delay, Count-Down Input (CP_D) to Borrow Output ($\overline{TC_D}$)		22	24	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400 Ω
t_{PHL}	Turn On Delay, Count-Down Input (CP_D) to Borrow Output ($\overline{TC_D}$)		18	24	ns	
t_{PLH}	Turn Off Delay, Either Count Input to Q Output		27	38	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400 Ω
t_{PHL}	Turn On Delay, Either Count Input to Q Output		37	47	ns	

TTL/MSI 93S62

9-INPUT PARITY CHECKER/GENERATOR

TO BE ANNOUNCED

DESCRIPTION — The TTL/MSI 93S63 is a very high speed 9-input parity checker/generator for use in error detection in data transmission applications. The 93S62 is implemented with Schottky barrier diode clamped TTL technology to insure high speed.

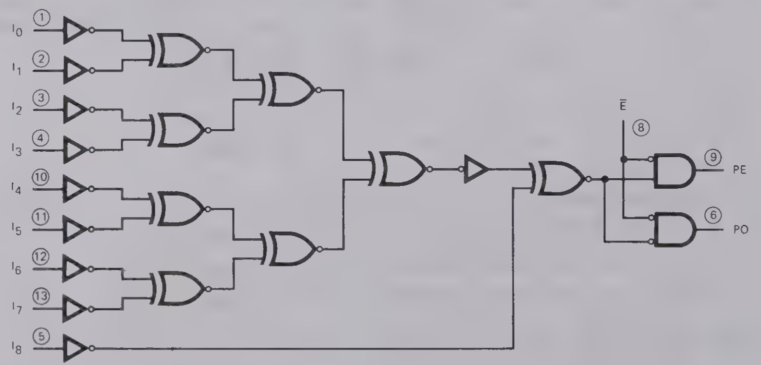
The 93S62 provides odd and even parity for up to nine data bits. The even parity output (PE) will be HIGH is an even number of logic ones are present on the inputs. The odd parity output (PO) will be HIGH if an odd number of logic ones are present. An enable input ($\overline{E}$) is provided which forces both outputs to a LOW level when the input is HIGH.

- **INPUT TO OUTPUT DELAY 16 ns**
- **OUTPUT ENABLE TERMINAL**
- **BOTH ODD AND EVEN PARITY OUTPUTS PROVIDED**
- **GENERATES A PARITY BIT FOR UP TO NINE BITS**
- **CHECKS FOR PARITY ON UP TO NINE BITS**
- **EASILY EXPANDABLE**
- **SCHOTTKY-CLAMPED TTL DESIGN**

PIN NAMES

I_0 to I_8	Data Inputs
$\overline{E}$	Output Enable
PO	Odd parity output
PE	Even parity output

LOGIC DIAGRAM



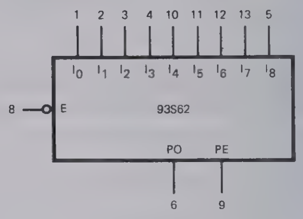
I_0 ①
I_1 ②
I_2 ③
I_3 ④
I_4 ⑩
I_5 ⑪
I_6 ⑫
I_7 ⑬
I_8 ⑤
$\overline{E}$ ⑧
⑨ PE
⑥ PO

$PO = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8$

$PE = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8$

○ = Pin Numbers

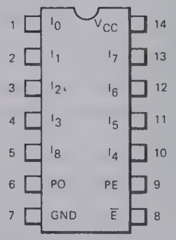
LOGIC SYMBOL



1 2 3 4 10 11 12 13 5
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 I_8
8 E
93S62
PO PE
6 9

V_{CC} = PIN 14
GND = PIN 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



1 I_0
2 I_1
3 I_2
4 I_3
5 I_8
6 PO
7 GND
14 V_{CC}
13 I_7
12 I_6
11 I_5
10 I_4
9 PE
8 $\overline{E}$

TTL/MSI 93H72

HIGH SPEED 4-BIT SHIFT REGISTER WITH ENABLE

DESCRIPTION – The 93H72 High Speed MSI 4-Bit Shift Register is a multifunctional sequential logic block which is useful in a wide variety of register applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data transfers. The circuit is compatible with all Fairchild 9300 MSI/TTL Integrated circuits.

The 93H72 has three synchronous modes of operation: shift, parallel load and hold (do nothing). The hold capability permits information storage in the register independent of the clock.

- **60 MHz TYPICAL SHIFT FREQUENCY**
- **SYNCHRONOUS PARALLEL ENTRY**
- **DATA HOLD (DO NOTHING) INDEPENDENT OF CLOCK**
- **FULLY SYNCHRONOUS WITH EDGE TRIGGERED TYPE CHARACTERISTICS ON INPUTS (EXCEPT $\overline{MR}$)**
- **ASYNCHRONOUS MASTER RESET**
- **TYPICAL POWER DISSIPATION OF 475 mW**
- **TTL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **INPUT CLAMP DIODES**

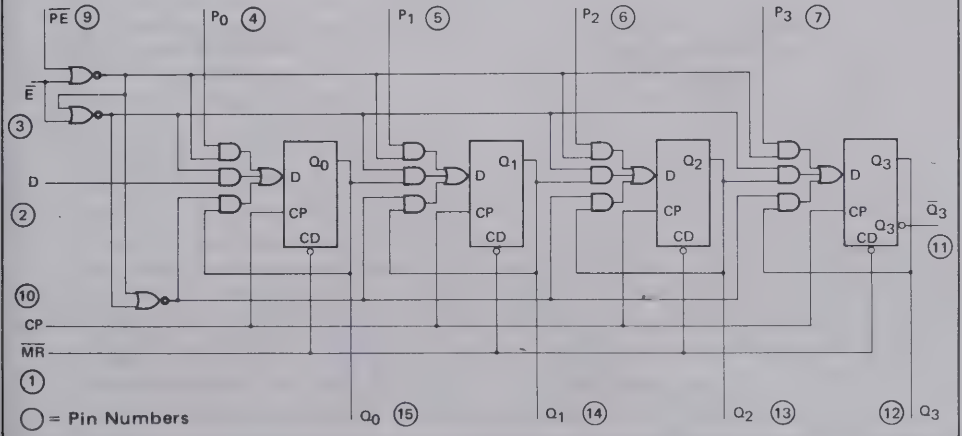
PIN NAMES		LOADING (Note a)
$\overline{E}$	Active LOW Enable Input	2 U.L.
$\overline{PE}$	Active LOW Parallel Enable Input	1 U.L.
P_0, P_1, P_2, P_3	Parallel Data Inputs	1 U.L.
CP	Clock Input	2 U.L.
$\overline{MR}$	Active LOW Master Reset Input	1 U.L.
Q_0 to Q_3	Parallel Outputs (Note b)	10 U.L.
$\overline{Q}_3$	Last Stage Complementary Output (Note b)	10 U.L.
D	Serial Data Input	1 U.L.

NOTES:

a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

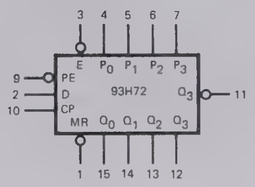
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



$\overline{PE}$ ⑨
P_0 ④
P_1 ⑤
P_2 ⑥
P_3 ⑦
$\overline{E}$
③
D
②
⑩
CP
$\overline{MR}$
①
D
Q_0
CP
CD
D
Q_1
CP
CD
D
Q_2
CP
CD
D
Q_3
CP
$\overline{Q}_3$
CD
$\overline{Q}_3$
⑪
Q_0 ⑮
Q_1 ⑭
Q_2 ⑬
⑫ Q_3
○ = Pin Numbers

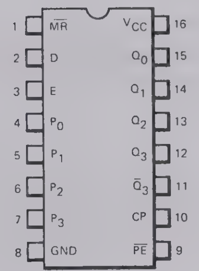
LOGIC SYMBOL



3
4
5
6
7
E
P_0
P_1
P_2
P_3
9
PE
2
D
10
CP
93H72
$\overline{Q}_3$
11
MR
Q_0
Q_1
Q_2
Q_3
1
15
14
13
12

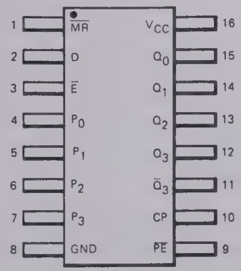
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 $\overline{MR}$
2 D
3 E
4 P_0
5 P_1
6 P_2
7 P_3
8 GND
16 V_{CC}
15 Q_0
14 Q_1
13 Q_2
12 Q_3
11 $\overline{Q}_3$
10 CP
9 $\overline{PE}$

FLATPAK (TOP VIEW)



1 $\overline{MR}$
2 D
3 $\overline{E}$
4 P_0
5 P_1
6 P_2
7 P_3
8 GND
16 V_{CC}
15 Q_0
14 Q_1
13 Q_2
12 Q_3
11 $\overline{Q}_3$
10 CP
9 $\overline{PE}$

FUNCTIONAL DESCRIPTION — The 93H72 is a 4-bit shift register with three modes of operation: shift, parallel load and hold (do nothing). The register is fully synchronous with any output change occuring after the rising clock edge. The 93H72 features edge triggered type characteristics on all inputs (except $\overline{MR}$) which means there are no restrictions on the activity of these inputs ($\overline{PE}$, $\overline{E}$, P_0, P_1, P_2, P_3, D) for logic operation except for the set up requirements prior to the LOW to HIGH clock transition.

The mode of operation of the 93H72 is determined by the two inputs, parallel enable ($\overline{PE}$) and enable ($\overline{E}$) as shown in Table I. The active LOW enable when HIGH, places the register in the hold mode with the register flip-flops retaining their information. When the enable is activated (LOW) the parallel enable ($\overline{PE}$) determines whether the register operates in a shift or parallel data entry mode.

When the enable is LOW and the parallel enable input is LOW the parallel inputs are selected and will determine the next condition of the register synchronously with the clock as shown in Table II. In this mode the element appears as four common clocked D flip-flops. With $\overline{E}$ LOW and the $\overline{PE}$ input HIGH the device acts as a 4-bit shift register with serial data entry through the D input shown in Table III. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the clock input.

The asynchronous active LOW master reset overrides all inputs and clears the register forcing outputs Q_{0-3} LOW and $\overline{Q}_3$ HIGH.

To provide for left shift operation, P_3 is used as the serial data input and Q_0 is the serial data output. The other outputs are tied back to the previous parallel inputs, with Q_3 tied to P_2, Q_2 tied to P_1 and Q_1 tied to P_0.

TABLE I. MODE SELECTION

MODE		$\overline{MR}$	$\overline{E}$	$\overline{PE}$	P_0	P_1	P_2	P_3	D
Synchronous	Parallel Load	H	L	L	Parallel Data Entry				X
	Serial Shift	H	L	H	X	X	X	X	Serial Data Entry
	Hold	H	H	L	X	X	X	X	X
	Hold	H	H	H	X	X	X	X	X
Asynchronous	Reset	L	X	X	All Outputs Set LOW				

TABLE III. SERIAL DATA ENTRY

D INPUT AT t_n	Q_0 AT t_{n+1}
L	L
H	H

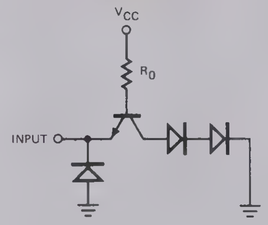
TABLE II. PARALLEL DATA ENTRY

P_0, P_1, P_2 OR P_3 INPUT AT t_n	Q at t_{n+1}
L	L
H	H

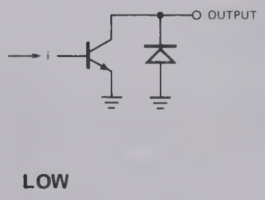
L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
t_n = Present State
t_{n+1} = State After Next Clock

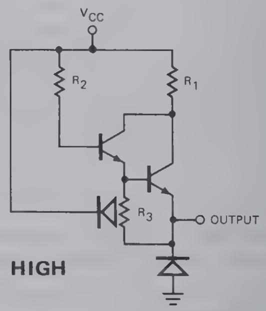
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

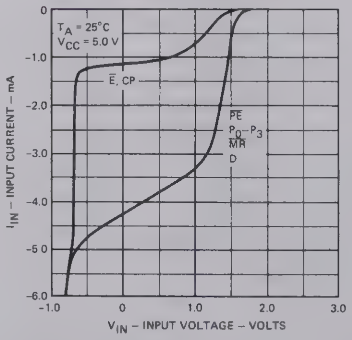


OUTPUTS EQUIVALENT CIRCUITS

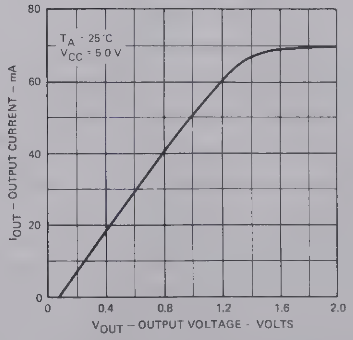




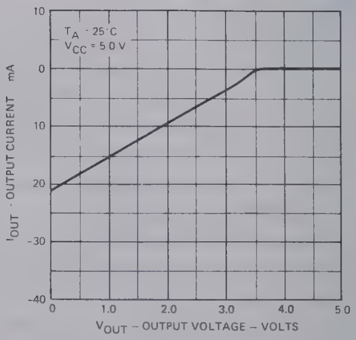
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93H72XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93H72XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS (Over operating temperature ranges)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage For All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold For All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., $I_{IN} = -12mA$, $T_A = 25°C$
V_{OH}	Output HIGH Voltage	2.4	2.7		Volts	V_{CC} = MIN., $I_{OH} = -800\ \mu A$
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 16.0 mA
I_{IL}	Input Load Current $\overline{MR}$, D, P_0, P_1, P_2, P_3, $\overline{PE}$		−1.08	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IL}	Input Load Current $\overline{E}$, CP		−2.16	−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input Leakage Current $\overline{MR}$, D, P_0, P_1, P_2, P_3, $\overline{PE}$		10	40	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IH}	Input Leakage Current $\overline{E}$, CP		20	80	µA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{CC}	Supply Current		95	120	mA	V_{CC} = MAX., 93H72XM
			100	135	mA	V_{CC} = MAX., 93H72XC
I_{SC}	Short-Circuit Output Current (Note 5)	30	75	100	mA	V_{CC} = MAX., V_{OUT} = 0.0V

NOTES:

1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C and max. loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF)

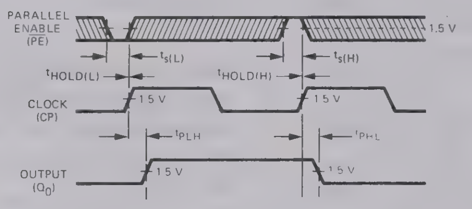
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f_{sr}	Shift Right Frequency	45	60		MHz	
t_{PHL}	Turn On Delay from Positive Clock Edge to Any Output		14.5	21	ns	Fig. 1
t_{PLH}	Turn Off Delay from Positive Clock Edge to Any Output		10	16	ns	Fig. 1
t_{PHL} ($\overline{MR}$)	Delay from Master Reset to Any Output		19	26	ns	Fig. 4
t_s (Data)	Setup Time for Data (D, P_0, P_1, P_2, P_3)	7.0	3.5		ns	Fig. 3
t_s ($\overline{E}$)	Setup Time for Enable, $\overline{E}$ (H or L)	17	9.0		ns	Fig. 2
t_s($\overline{PE}$)	Setup Time for Parallel Enable, $\overline{PE}$	19	10		ns	Fig. 1
t_{rec}($\overline{MR}$)	Recovery Time for $\overline{MR}$	7.0	3.0		ns	Fig. 4
t_{pw} $\overline{MR}$	Required Pulse Width for $\overline{MR}$	19	11		ns	Fig. 4
t_{HOLD} (Data) ($\overline{E}$) or ($\overline{PE}$)	Hold Time for Data, $\overline{E}$, or $\overline{PE}$	0			ns	Fig. 1, 2 and 3

NOTES:

6. SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the register to respond.
7. HOLD TIME: t_{HOLD} is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained to insure continued recognition.
8. RECOVERY TIME FOR $\overline{MR}$: t_{rec} ($\overline{MR}$) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order for the flip-flop(s) to respond to the clock.

SWITCHING TIME WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

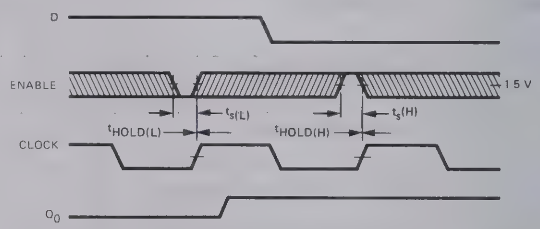


SET UP TIME (t_s) FOR PARALLEL ENABLE

PARALLEL ENABLE (PE)
1.5 V
$t_{s(L)}$
$t_{s(H)}$
$t_{HOLD(L)}$
$t_{HOLD(H)}$
CLOCK (CP)
1.5 V
1.5 V
t_{PLH}
t_{PHL}
OUTPUT (Q_0)
1.5 V
1.5 V

Other Conditions: P_0 = H
$\overline{E}$ = L
D = L

Fig. 1

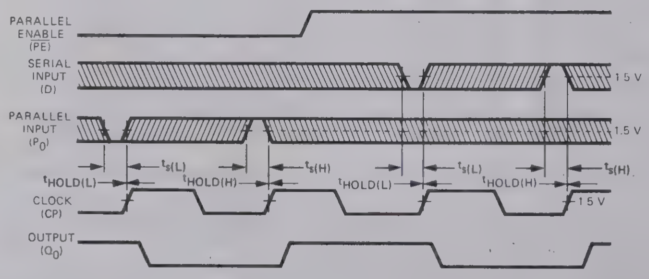


SET UP TIME (t_s) FOR ENABLE ($\overline{E}$)

D
ENABLE
1.5 V
$t_{s(L)}$
$t_{s(H)}$
$t_{HOLD(L)}$
$t_{HOLD(H)}$
CLOCK
Q_0

Other Conditions: $\overline{PE}$ = H

Fig. 2

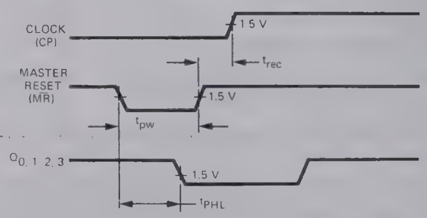


SET UP TIME (t_s) FOR DATA (D, $P_{0, 1, 2, 3}$)

PARALLEL ENABLE (PE)
SERIAL INPUT (D)
1.5 V
PARALLEL INPUT (P_0)
1.5 V
$t_{s(L)}$
$t_{s(H)}$
$t_{s(L)}$
$t_{s(H)}$
$t_{HOLD(L)}$
$t_{HOLD(H)}$
$t_{HOLD(L)}$
$t_{HOLD(H)}$
CLOCK (CP)
1.5 V
OUTPUT (Q_0)

Other Conditions: $\overline{E}$ = L

Fig. 3



DELAY FROM $\overline{MR}$ TO OUTPUT t_{PHL}
MASTER RESET RECOVERY TIME (t_{rec})
REQUIRED MASTER RESET PULSE WIDTH

CLOCK (CP)
1.5 V
t_{rec}
MASTER RESET ($\overline{MR}$)
1.5 V
t_{pw}
$Q_{0, 1, 2, 3}$
1.5 V
t_{PHL}

Other Conditions: $\overline{E}$ = L, $\overline{PE}$ = L, $P_0 = P_1 = P_2 = P_3$ = H

Fig. 4

TTL/MSI 9375/5475, 7475
9377/5477, 7477
4-BIT LATCH

DESCRIPTION – The TTL/MSI 9375/5475, 7475 and 9377/5477, 7477 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is HIGH and the Q output will follow the data input as long as the clock remains HIGH. When the clock goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go HIGH.

The 9375/5475, 7475 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in the 16-lead packages. For higher component density applications the 9377/5477, 7477 4-bit latch is available in the 14-lead package with $\overline{Q}$ outputs omitted.

PIN NAMES		LOADING
D_1, D_2, D_3, D_4	Data Inputs	2 U.L.
$\overline{CP}_{1-2}$	Clock Input Latches 1 & 2	4 U.L.
$\overline{CP}_{3-4}$	Clock Input Latches 3 & 4	4 U.L.
Q_1, Q_2, Q_3, Q_4	Latch Outputs	10 U.L.
$\overline{Q}_1, \overline{Q}_2, \overline{Q}_3, \overline{Q}_4$	Complementary Latch Outputs	10 U.L.

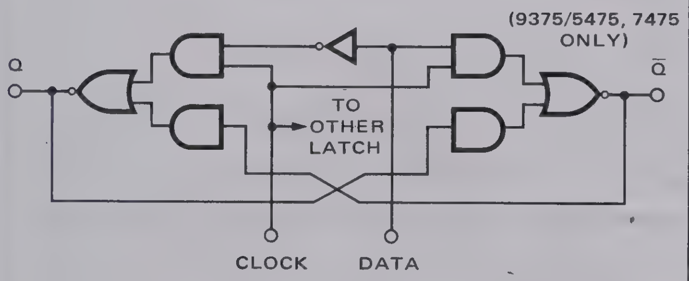
Note: 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE
(Each Latch)

t_n	t_{n+1}
D	Q
H	H
L	L

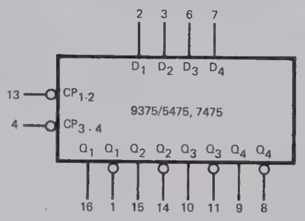
NOTES:
t_n = bit time before clock negative-going transition.
t_{n+1} = bit time after clock negative-going transition.

LOGIC DIAGRAM
(EACH LATCH)



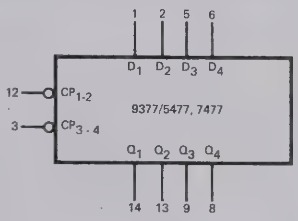
(9375/5475, 7475 ONLY)
Q
$\overline{Q}$
TO OTHER LATCH
CLOCK
DATA

LOGIC SYMBOL



2 3 6 7
D1 D2 D3 D4
13 CP1-2
4 CP3-4
9375/5475, 7475
Q1 $\overline{Q}_1$ Q2 $\overline{Q}_2$ Q3 $\overline{Q}_3$ Q4 $\overline{Q}_4$
16 1 15 14 10 11 9 8

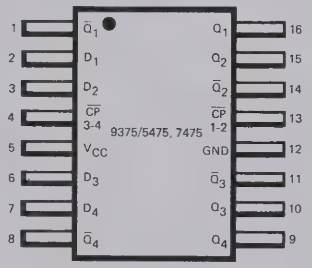
V_{CC} = Pin 5
GND = Pin 12



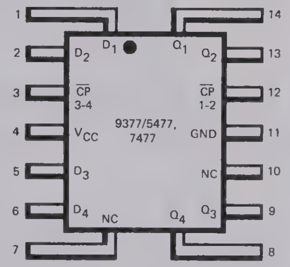
1 2 5 6
D1 D2 D3 D4
12 CP1-2
3 CP3-4
9377/5477, 7477
Q1 Q2 Q3 Q4
14 13 9 8

V_{CC} = Pin 4
GND = Pin 11
NC = Pin 7, 10

CONNECTION DIAGRAM
FLATPAKS (TOP VIEW)

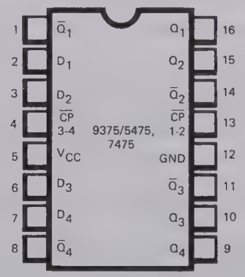


9375/5475, 7475
1 $\overline{Q}_1$
2 D1
3 D2
4 $\overline{CP}$ 3-4
5 V_{CC}
6 D3
7 D4
8 $\overline{Q}_4$
16 Q1
15 Q2
14 $\overline{Q}_2$
13 $\overline{CP}$ 1-2
12 GND
11 $\overline{Q}_3$
10 Q3
9 Q4



9377/5477, 7477
1 D1
2 D2
3 $\overline{CP}$ 3-4
4 V_{CC}
5 D3
6 D4
7
14 Q1
13 Q2
12 $\overline{CP}$ 1-2
11 GND
10 NC
9 Q3
8
NC
Q4

DIP (TOP VIEW)



9375/5475, 7475
1 $\overline{Q}_1$
2 D1
3 D2
4 $\overline{CP}$ 3-4
5 V_{CC}
6 D3
7 D4
8 $\overline{Q}_4$
16 Q1
15 Q2
14 $\overline{Q}_2$
13 $\overline{CP}$ 1-2
12 GND
11 $\overline{Q}_3$
10 Q3
9 Q4

Positive logic: See truth table.
NC — No internal connection.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to + 150°C
Temperature (Ambient) Under Bias	–55°C to + 125°C
V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0 V
*Input Voltage (dc)	–0.5V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9375XM/5475XM 9377XM/5477XM			9375XC/7475XC 9377XC/7477XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan Out from Outputs			10			10	

X = package type; F for Flatpak; D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –0.4 mA		1 & 2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1 & 2
I_{IH}	Input HIGH Current at D			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Clock			160	µA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at D			–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at Clock			–6.4	mA	V_{CC} = MAX.		3
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9375/5475; 9377/5477	V_{CC} = MAX.	4
		–18		–57	mA	9375/7475; 9377/7477		
I_{CC}	Supply Current		32	46	mA	9375/5475; 9377/5477	V_{CC} = MAX.	5
			32	53	mA	9375/7475; 9377/7477		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{setupH}	At D Input		7.0	20	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{setupL}	At D Input		14	20	ns		A
t_{holdH}	At D Input	0	15*		ns		A
t_{holdL}	At D Input	0	6.0*		ns		A
t_{PLH}	D to Q		16	30	ns	V_{CC} = 5.0 V, C_L = 15 pF R_L = 400Ω	A
t_{PHL}			14	25			
t_{PLH}	D to $\overline{Q}$ (9375/5475, 7475)		24	40	ns	V_{CC} = 5.0 V, C_L = 15 pF R_L = 400Ω	A
t_{PHL}			7.0	15			
t_{PLH}	$\overline{CP}$ to $\overline{Q}$		16	30	ns	V_{CC} = 5.0 V, C_L = 15 pF R_L = 400Ω	A
t_{PHL}			7.0	15			
t_{PLH}	$\overline{CP}$ to Q (9375/5475, 7475)		16	30	ns	V_{CC} = 5.0 V, C_L = 15 pF R_L = 400Ω	A
t_{PHL}			7.0	15			

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

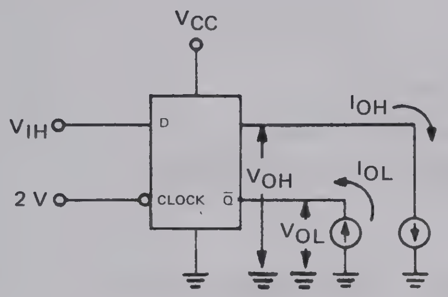
(3) Not more than one output should be shorted at a time.

(4) These voltage values are with respect to network ground terminal.

* These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5 V when data at the D input will still be recognized at stored.

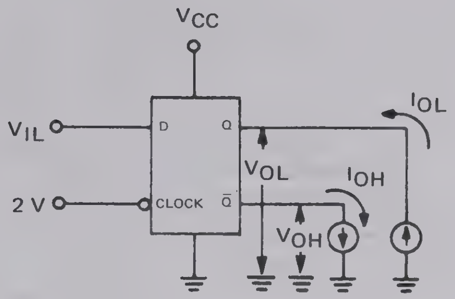
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*


VCC
VIH
2 V
D
CLOCK
Q̄
IOH
VOH
IOL
VOL

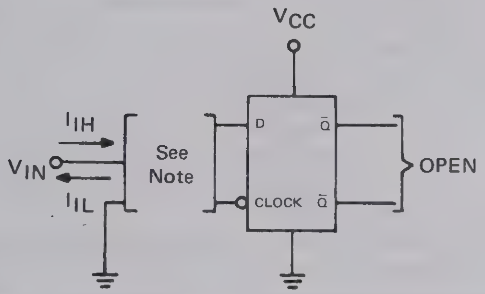
1. Each latch is tested separately.

Fig. 1


VCC
VIL
2 V
D
Q
CLOCK
Q̄
IOL
VOL
IOH
VOH

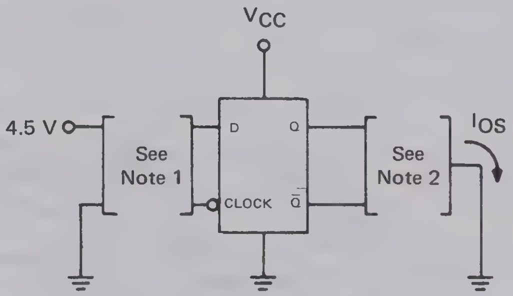
1. Each latch is tested separately.

Fig. 2


VCC
IIH
VIN
IIL
See Note
D
Q̄
CLOCK
Q̄
OPEN

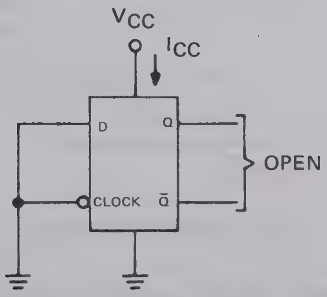
1. Each input is tested separately.
2. When testing I_{IH} at D ground clock.
3. When testing I_{IH} at clock ground all D inputs.

Fig. 3


VCC
4.5 V
See Note 1
D
Q
CLOCK
Q̄
See Note 2
IOS

1. Input conditions are in accordance with truth table.
2. Each latch and each output is tested separately.

Fig. 4


VCC
ICC
D
Q
CLOCK
Q̄
OPEN

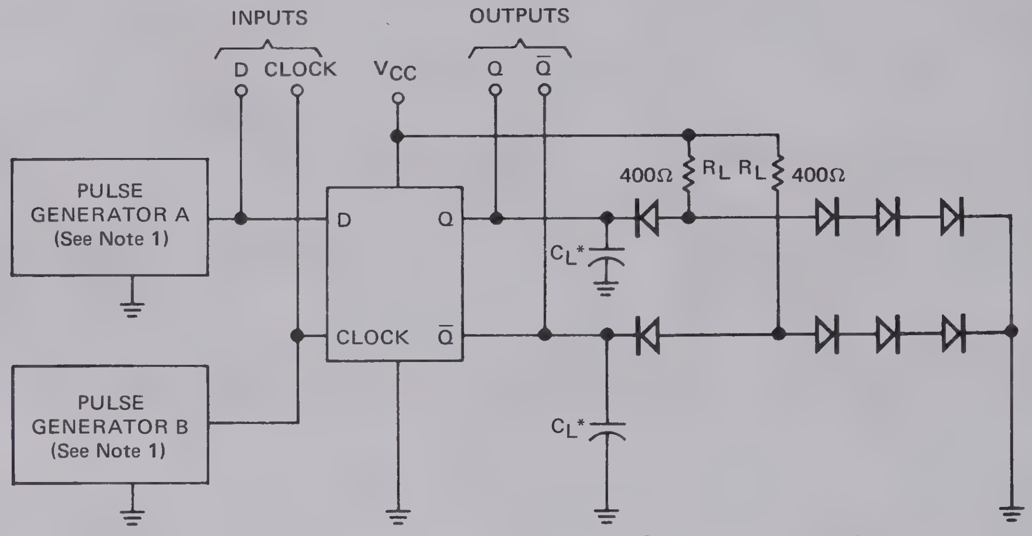
1. All latches are tested simultaneously.

Fig. 5

*Arrows indicate actual direction of current flow. Complementary Q̄ outputs are available on the 9375/5475, 7475.

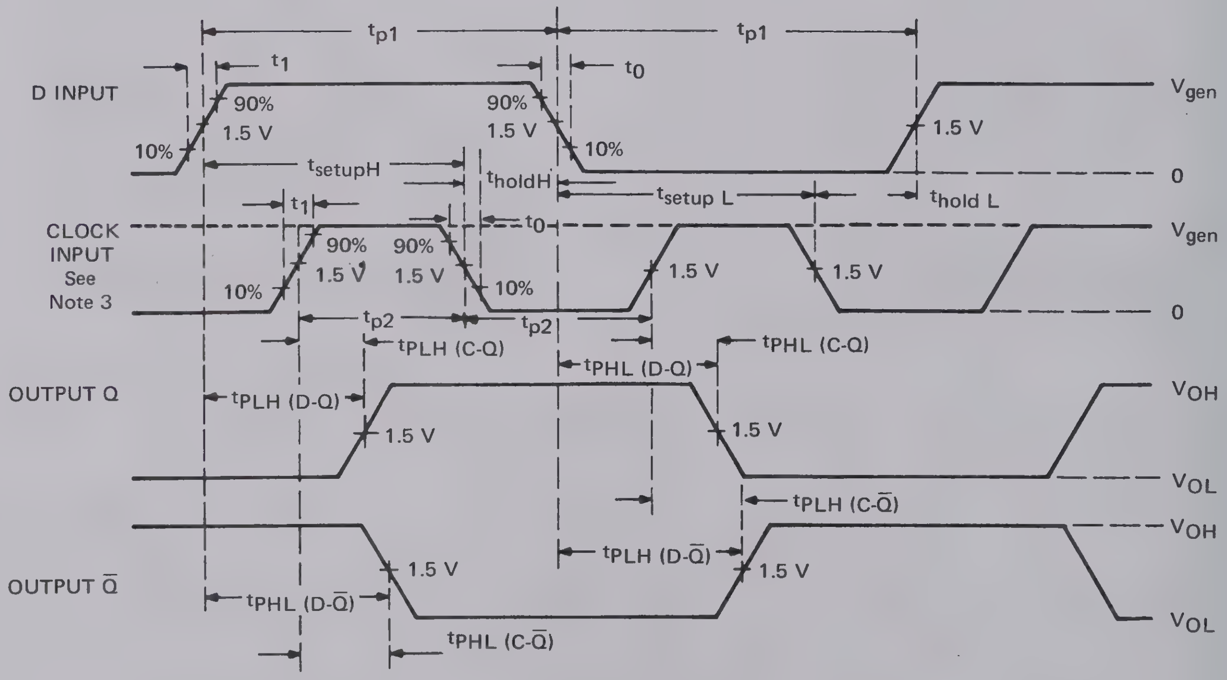
PARAMETER MEASUREMENT INFORMATION (con't)

SWITCHING CHARACTERISTICS*


INPUTS
D
CLOCK
VCC
OUTPUTS
Q
Q̄
PULSE GENERATOR A (See Note 1)
PULSE GENERATOR B (See Note 1)
D
Q
CLOCK
Q̄
400Ω
RL
RL
400Ω
CL*
CL*

*C_L includes probe and jig capacitance.

TEST CIRCUIT


tp1
tp1
t1
t0
D INPUT
90%
1.5 V
10%
90%
1.5 V
10%
1.5 V
Vgen
0
tsetupH
tholdH
tsetup L
thold L
t1
t0
CLOCK INPUT See Note 3
90%
1.5 V
10%
90%
1.5 V
10%
1.5 V
1.5 V
Vgen
0
tp2
tp2
tPLH (C-Q)
tPHL (D-Q)
tPHL (C-Q)
OUTPUT Q
tPLH (D-Q)
1.5 V
1.5 V
VOH
VOL
tPLH (C-Q̄)
tPLH (D-Q̄)
1.5 V
VOH
OUTPUT Q̄
1.5 V
tPHL (D-Q̄)
tPHL (C-Q̄)
VOL

VOLTAGE WAVEFORMS

NOTES:

1. The pulse generators have the following characteristics: $V_{gen} = 3$ V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \approx 50\Omega$. For pulse generator A $t_{p1} = 1$ μs and PRR = 500 kHz. For pulse generator B, $t_{p2} = 500$ ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. When measuring t_{PLH} (D-Q) and t_{PHL} (D-Q) or t_{PHL} (D-Q) and t_{PLH} (D-$\bar{Q}$) for the 9375/5475, 7475, clock input must be held at high level.

Fig. A SWITCHING TIMES

*Complementary Q outputs are on the 9375/5475, 7475.

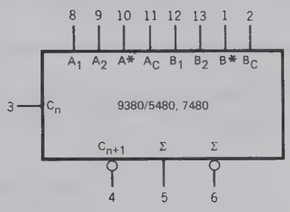
TTL/MSI 9380/5480, 7480
GATED FULL ADDER

DESCRIPTION — The TTL/MSI 9380/5480, 7480 is a single-bit, high speed, Binary Full Adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. It is designed for medium and high speed, multiple-bit, parallel-add/serial-carry applications. The circuit utilizes DTL for the gated inputs and high speed, high fan out TTL for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

PIN NAMES		**LOADING**
A_1, A_2, B_1, B_2	Non Inverting Data Inputs	1 U.L.
A^*, B^*	Inverting Data Inputs	1.65 U.L.
A_C, B_C	Control Inputs	1 U.L.
C_n	Carry Input	5 U.L.
$\overline{C_{n+1}}$	Carry Output	5 U.L.
Σ, Σ	Sum Outputs	10 U.L.
A^*, B^*	When Used as Outputs	3 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

LOGIC SYMBOL


8
9
10
11
12
13
1
2
A_1
A_2
A^*
A_C
B_1
B_2
B^*
B_C
3
C_n
9380/5480, 7480
C_{n+1}
Σ
Σ
4
5
6

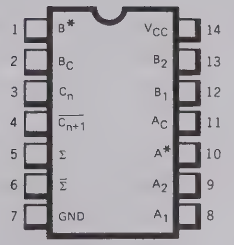
TRUTH TABLE

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

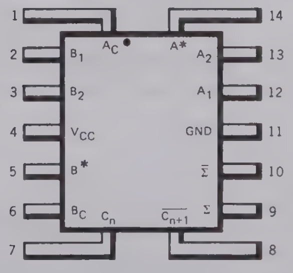
NOTES:

1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$ where $A^* = \overline{A_1 \cdot A_2}$.
   $B^* = \overline{B_1 \cdot B_2}$
2. When A^* or B^* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A^* or B^* respectively must be open or used to perform Dot-OR logic.

CONNECTION DIAGRAM
DIP (TOP VIEW)

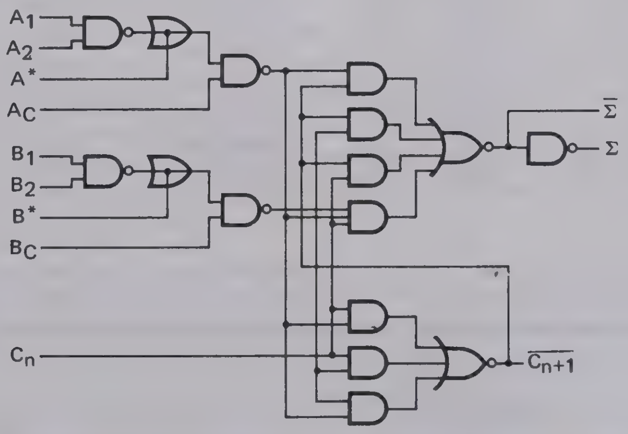

1
B^*
2
B_C
3
C_n
4
$\overline{C_{n+1}}$
5
Σ
6
$\overline{\Sigma}$
7
GND
14
V_{CC}
13
B_2
12
B_1
11
A_C
10
A^*
9
A_2
8
A_1

FLATPAK (TOP VIEW)


1
2
3
4
5
6
7
14
13
12
11
10
9
8
B_1
A_C
A^*
A_2
B_2
A_1
V_{CC}
GND
B^*
$\overline{\Sigma}$
B_C
C_n
$\overline{C_{n+1}}$
Σ

Positive logic: See truth table

LOGIC DIAGRAM


A_1
A_2
A^*
A_C
B_1
B_2
B^*
B_C
C_n
$\overline{\Sigma}$
Σ
$\overline{C_{n+1}}$

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9380XM/5480XM			9380XC/7480XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out from Outputs	$\overline{C_{n+1}}$, N			5.0			5.0	
	Σ or $\overline{\Sigma}$, N			10			10	
	A* or B*, N			3.0			3.0	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}		1 & 2
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN.		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at A_1, A_2, B_1, B_2, A_c or B_c			15	µA	V_{CC} = MAX., V_{IN} = 2.4 V		5
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at C_n			200	µA	V_{CC} = MAX., V_{IN} = 2.4 V		6
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at A_1, A_2, B_1, B_2, A_c, or B_c			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at A* or B*			–2.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at C_n			–8.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{OS}	Output Short Circuit Current at Σ or $\overline{\Sigma}$ (Note 3)	–20		–57	mA	9380/5480	V_{CC} = MAX.	7
		–18		–57	mA	9380/7480		
	Output Short Circuit Current at $\overline{C_{n+1}}$ (Note 3)	–20		–70	mA	9380/5480	V_{CC} = MAX.	7
		–18		–70	mA	9380/7480		
I_{CC}	Supply Current		21	31	mA	9380/5480	V_{CC} = MAX.	8
			21	35	mA	9380/7480		

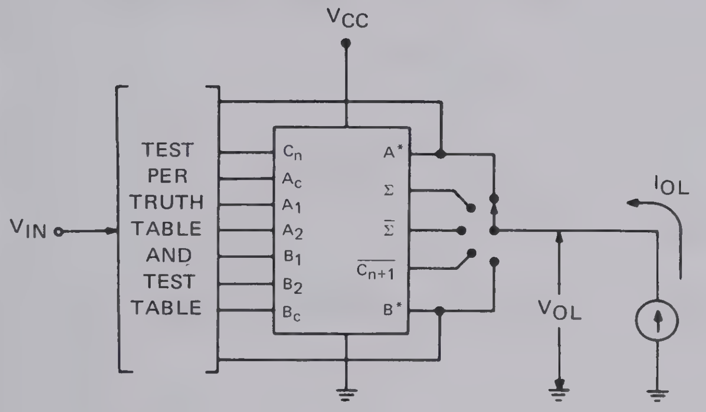
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	FIGURE A TEST NO.
t_{PLH}	(C_n to $\overline{C_{n+1}}$)		13	17	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 780\Omega$	1
t_{PHL}			8.0	12			2
t_{PLH}	(B_c to $\overline{C_{n+1}}$)		18	25	ns		3
t_{PHL}			38	55			4
t_{PLH}	(A_c to Σ)		52	70	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 400\Omega$	5
t_{PHL}			62	80			6
t_{PLH}	(B_c to $\overline{\Sigma}$)		38	55	ns		7
t_{PHL}			56	75			8
t_{PLH}	(A_1 to A^*)		48	65	ns	$V_{CC} = 5.0$ V $C_L = 15$ pF	9
t_{PHL}			17	25			10
t_{PLH}	(B_1 to B^*)		48	65	ns		11
t_{PHL}			17	25			12

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



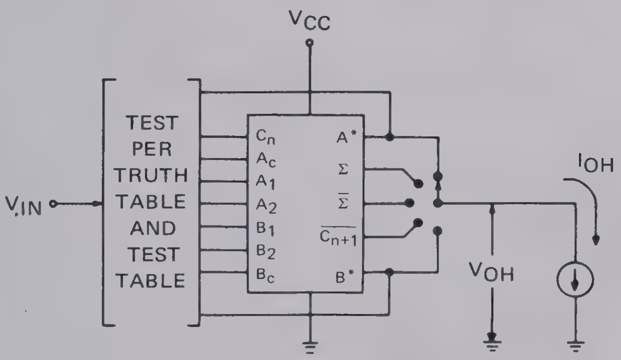
V_{CC}
TEST PER TRUTH TABLE AND TEST TABLE
V_{IN}
C_n
A_c
A_1
A_2
B_1
B_2
B_c
A^*
Σ
$\overline{\Sigma}$
$\overline{C_{n+1}}$
B^*
I_{OL}
V_{OL}

TEST TABLE

Output Under Test	I_{OL} (Min)
Σ or $\overline{\Sigma}$	16 mA
$\overline{C_{n+1}}$	8 mA
A^* or B^*	4.8 mA

1. Each input or output is tested separately.
2. When A^* is tested A_1 and A_2 are at GND. When B^* is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 is tested, A^* or B^* respectively, is open.

Fig. 1



V_{CC}
TEST PER TRUTH TABLE AND TEST TABLE
V_{IN}
C_n
A_c
A_1
A_2
B_1
B_2
B_c
A^*
Σ
$\overline{\Sigma}$
$\overline{C_{n+1}}$
B^*
I_{OH}
V_{OH}

TEST TABLE

Output Under Test	I_{OH} (Min)
Σ or $\overline{\Sigma}$	–400 μA
$\overline{C_{n+1}}$	–200 μA
A^* or B^*	–120 μA

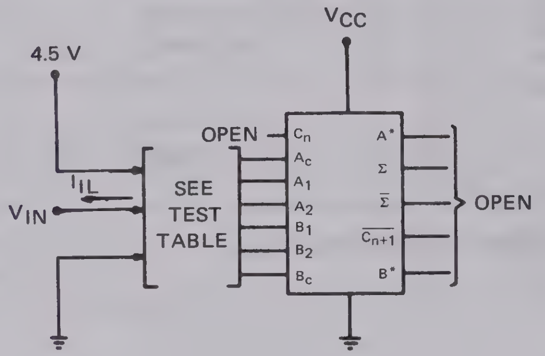
1. Each input or output is tested separately.
2. When A^* is tested A_1 and A_2 are at GND. When B^* is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 are tested A or B, respectively, is open.

Fig. 2

* Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (continued)

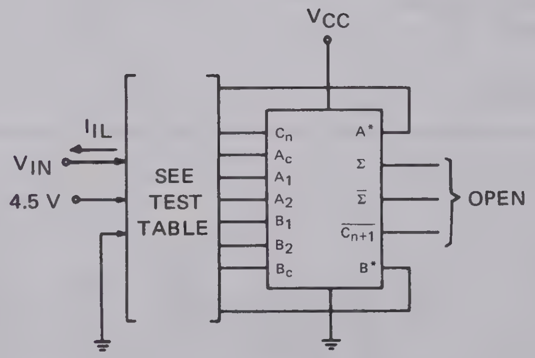

VCC
4.5 V
OPEN
I_{IL}
V_{IN}
SEE TEST TABLE
C_n
A_c
A_1
A_2
B_1
B_2
B_c
A*
Σ
$\overline{\Sigma}$
$\overline{C_{n+1}}$
B*
OPEN

TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	GND
A_1	A_2	None
A_2	A_1	None
B_1	B_2	None
B_2	B_1	None
A_c	None	A_1 and A_2
B_c	None	B_1 and B_2

1. Each input is tested separately.

Fig. 3


VCC
I_{IL}
V_{IN}
4.5 V
SEE TEST TABLE
C_n
A_c
A_1
A_2
B_1
B_2
B_c
A*
Σ
$\overline{\Sigma}$
$\overline{C_{n+1}}$
B*
OPEN

TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	GND
A*	A_c	A_1 and A_2
B*	B_c	B_1 and B_2
C_n	None	None

Unused inputs are open.

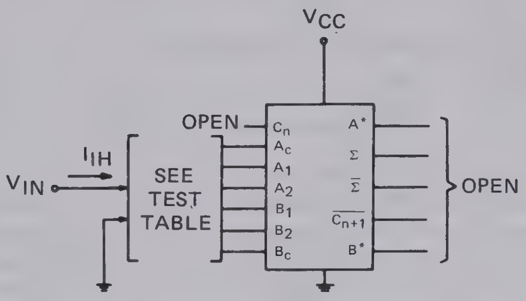
1. Each input is tested separately.

Fig. 4

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (continued)



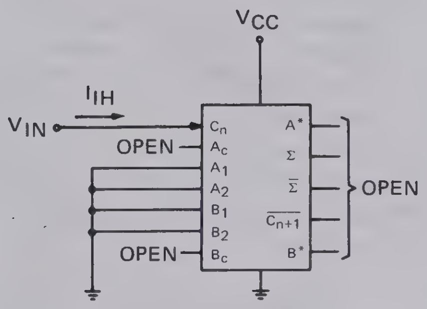
V_{CC}
OPEN
I_{IH}
V_{IN}
SEE TEST TABLE
C_n
A_c
A_1
A_2
B_1
B_2
B_c
A^*
Σ
$\overline{\Sigma}$
$\overline{C_{n+1}}$
B^*
OPEN

TEST TABLE

Apply V_{IN} (Test I_{IH})	GND
A_1	A_2
A_2	A_1
B_1	B_2
B_2	B_1
A_c	A^*
B_c	B^*

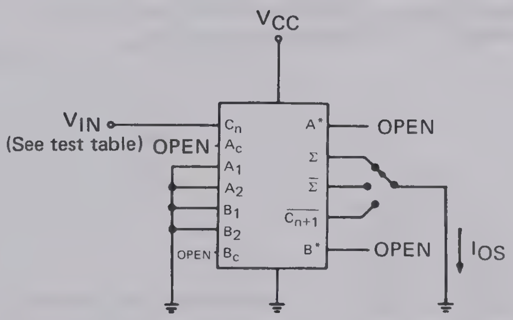
1. Each input is tested separately.

Fig. 5



V_{CC}
I_{IH}
V_{IN}
OPEN
OPEN
C_n
A_c
A_1
A_2
B_1
B_2
B_c
A^*
Σ
$\overline{\Sigma}$
$\overline{C_{n+1}}$
B^*
OPEN

Fig. 6



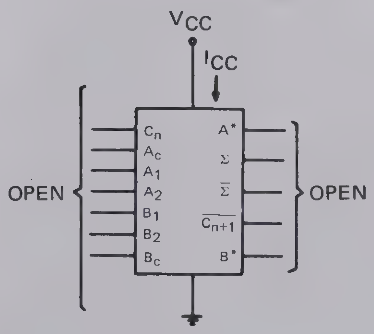
V_{CC}
V_{IN}
(See test table)
OPEN
OPEN
C_n
A_c
A_1
A_2
B_1
B_2
B_c
A^*
Σ
$\overline{\Sigma}$
$\overline{C_{n+1}}$
B^*
OPEN
OPEN
I_{OS}

1. Each output is tested separately.

TEST TABLE

Output Under Test	V_{IN} Value
Σ	V_{CC}
$\overline{\Sigma}$ or $\overline{C_{n+1}}$	GND

Fig. 7



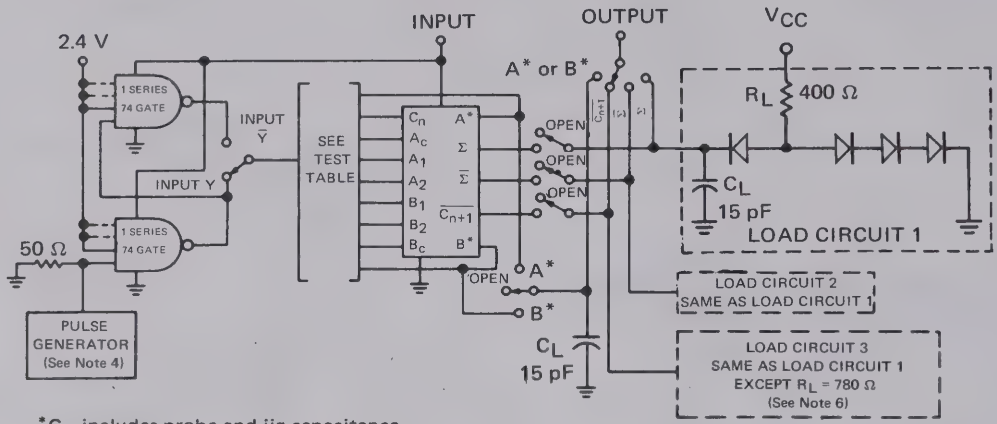
V_{CC}
I_{CC}
OPEN
C_n
A_c
A_1
A_2
B_1
B_2
B_c
A^*
Σ
$\overline{\Sigma}$
$\overline{C_{n+1}}$
B^*
OPEN

Fig. 8

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS

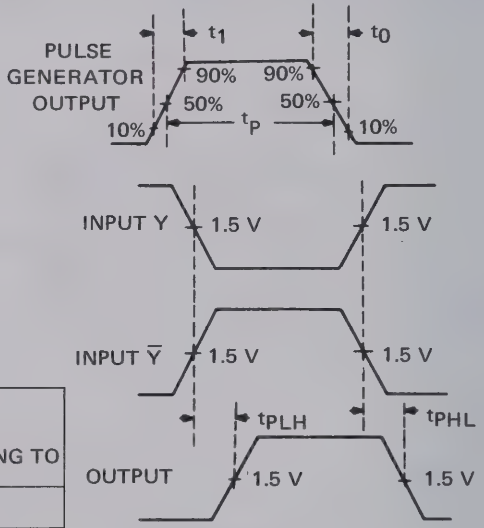

2.4 V
INPUT
OUTPUT
V_{CC}
1 SERIES 74 GATE
1 SERIES 74 GATE
INPUT $\overline{Y}$
INPUT Y
SEE TEST TABLE
C_n
A_c
A_1
A_2
B_1
B_2
B_c
A*
Σ
$\overline{\Sigma}$
$\overline{C_{n+1}}$
B*
A* or B*
OPEN
OPEN
OPEN
OPEN
A*
B*
R_L 400 Ω
C_L 15 pF
LOAD CIRCUIT 1
LOAD CIRCUIT 2 SAME AS LOAD CIRCUIT 1
LOAD CIRCUIT 3 SAME AS LOAD CIRCUIT 1 EXCEPT R_L = 780 Ω (See Note 6)
C_L 15 pF
50 Ω
PULSE GENERATOR (See Note 4)

*C_L includes probe and jig capacitance.

NOTES:

1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 15$ ns, t_p = 0.5 µs, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
5. Inputs and outputs not otherwise specified are open.
6. Load circuit 2 simulates output load of 5.

TEST CIRCUIT


t_1
t_0
PULSE GENERATOR OUTPUT
90%
90%
50%
50%
10%
10%
t_p
INPUT Y
1.5 V
1.5 V
INPUT $\overline{Y}$
1.5 V
1.5 V
t_{PLH}
t_{PHL}
OUTPUT
1.5 V
1.5 V

VOLTAGE WAVEFORMS

TEST TABLE (SEE NOTE 5)

TEST NO.	OUTPUT UNDER TEST	APPLY INPUT $\overline{Y}$ TO	APPLY INPUT Y TO	APPLY +2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
3	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
4	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
5	Σ	A_c	None	C_n	A_1, B_1	$\overline{\Sigma}$ (N = 10)
						Σ (N = 10)
						$\overline{C_{n+1}}$ (N = 5)
6	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10)
						$\overline{\Sigma}$ (N = 10)
						$\overline{C_{n+1}}$ (N = 5)
7	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
8	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
9	A*	None	A_1	A_2	None	A* (C_L = 15 pF)
10	A*	None	A_1	A_2	None	A* (C_L = 15 pF)
11	B*	None	B_1	B_2	None	B* (C_L = 15 pF)
12	B*	None	B_1	B_2	None	B* (C_L = 15 pF)

Fig. A — SWITCHING TIMES

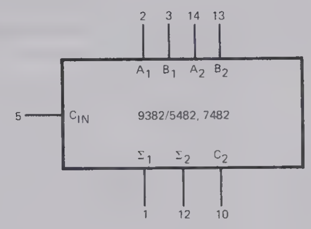
TTL/MSI 9382/5482, 7482
2-BIT FULL ADDER

DESCRIPTION – The TTL/MSI 9382/5482,7482 is a Full Adder which performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium to high speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilized high speed, high fan out TTL. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

PIN NAMES		LOADING
A_1,B_1	Data Inputs	4 U.L.
A_2,B_2	Data Inputs	1 U.L.
C_{IN}	Carry Input	4 U.L.
Σ_1	Sum Output Bit 1	10 U.L.
Σ_2	Sum Output Bit 2	10 U.L.
C_2	Carry Output Bit 2	5 U.L.

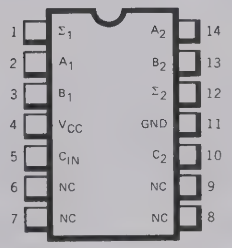
1 Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW

LOGIC SYMBOL

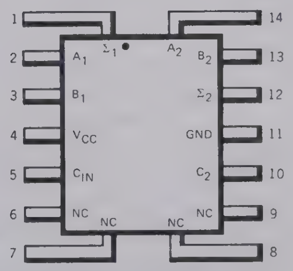

2
3
14
13
A1
B1
A2
B2
5
CIN
9382/5482, 7482
Σ1
Σ2
C2
1
12
10

V_{CC} = Pin 4
GND = Pin 11
NC = Pin 6, 7, 8, 9

CONNECTION DIAGRAM DIP (TOP VIEW)

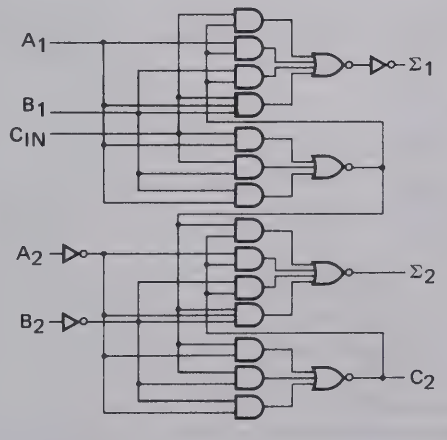

1
2
3
4
5
6
7
Σ1
A1
B1
VCC
CIN
NC
NC
A2
B2
Σ2
GND
C2
NC
NC
14
13
12
11
10
9
8

FLATPAK (TOP VIEW)


1
2
3
4
5
6
7
A1
Σ1
B1
VCC
CIN
NC
NC
A2
B2
Σ2
GND
C2
NC
NC
14
13
12
11
10
9
8

Positive logic: See truth table
NC – No internal connection

LOGIC DIAGRAM


A1
B1
CIN
A2
B2
Σ1
Σ2
C2

TRUTH TABLE

INPUT				OUTPUT					
				WHEN C_{IN} = 0			WHEN C_{IN} = 1		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9382XM/5482XM			9382XC/7482XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Output	C_2			5.0			5.0	
	Σ_1 or Σ_2			10			10	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}		1 & 2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −400 μA		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at A_1, B_1 or C_{IN}			160	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at A_2 or B_2			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at A_1, B_1 or C_{IN}			−6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at A_2 or B_2			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
I_{OS}	Output Short Circuit Current at Σ_1 or Σ_2 (Note 3)	−20		−55	mA	9382/5482	V_{CC} = MAX.	4
		−18		−55	mA	9382/7482		
	Output Short Circuit Current at C_2 (Note 3)	−20		−70	mA	9382/5482	V_{CC} = MAX.	4
		−18		−70	mA	9382/7482		
I_{CC}	Supply Current		35	50	mA	9382/5482	V_{CC} = MAX.	3
			35	58	mA	9382/7482		

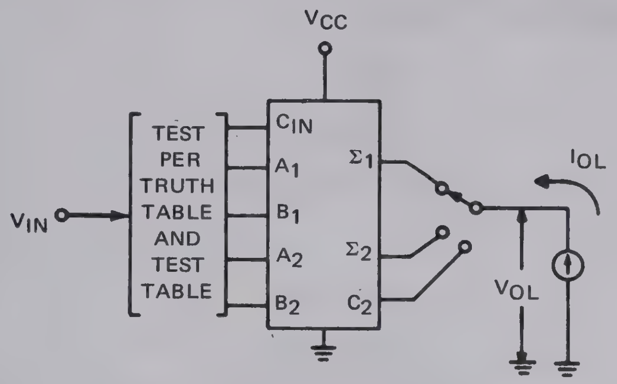
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	FIGURE A TEST NO.
		MIN.	TYP.	MAX.			
t_{PLH}	C_{IN} to Σ_1			34	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	1
t_{PHL}				40			2
t_{PLH}	B_2 to Σ_2			40	ns		3
t_{PHL}				35			4
t_{PLH}	C_{IN} to Σ_2			38	ns		5
t_{PHL}				42			6
t_{PLH}	C_{IN} to C_2		17	27	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 780Ω	7
t_{PHL}			12	19			8

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

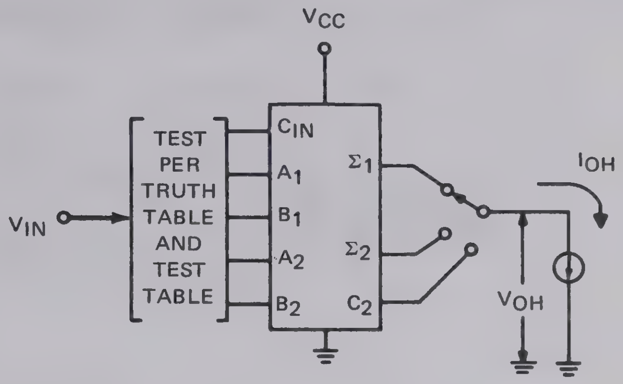

VCC
TEST PER TRUTH TABLE AND TEST TABLE
VIN
CIN
A1
B1
A2
B2
Σ1
Σ2
C2
IOL
VOL

1. Each input or output is tested separately.

TEST TABLE

OUTPUT UNDER TEST	I_{OL}
Σ_1 or Σ_2	16 mA
C_2	8 mA

Fig. 1

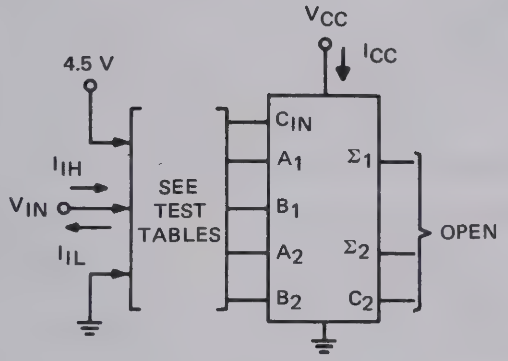

VCC
TEST PER TRUTH TABLE AND TEST TABLE
VIN
CIN
A1
B1
A2
B2
Σ1
Σ2
C2
IOH
VOH

1. Each input or output is tested separately.

TEST TABLE

OUTPUT UNDER TEST	I_{OH}
Σ_1 or Σ_2	–400 µA
C_2	–200 µA

Fig. 2


VCC
ICC
4.5 V
IIH
VIN
IIL
SEE TEST TABLES
CIN
A1
B1
A2
B2
Σ1
Σ2
C2
OPEN

I_{IL} TEST TABLE

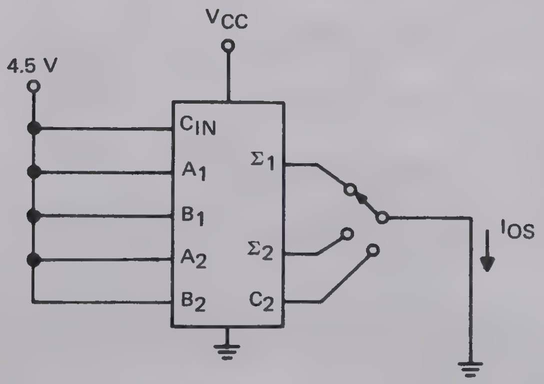
APPLY V_{IN} TEST I_{IN}	APPLY 4.5 V
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None

I_{IH} TEST TABLE

APPLY V_{IN} TEST I_{IN}	GND
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, and C_{IN}; and ground B_1 and B_2.

Fig. 3


VCC
4.5 V
CIN
A1
B1
A2
B2
Σ1
Σ2
C2
IOS

1. Each output is tested separately.

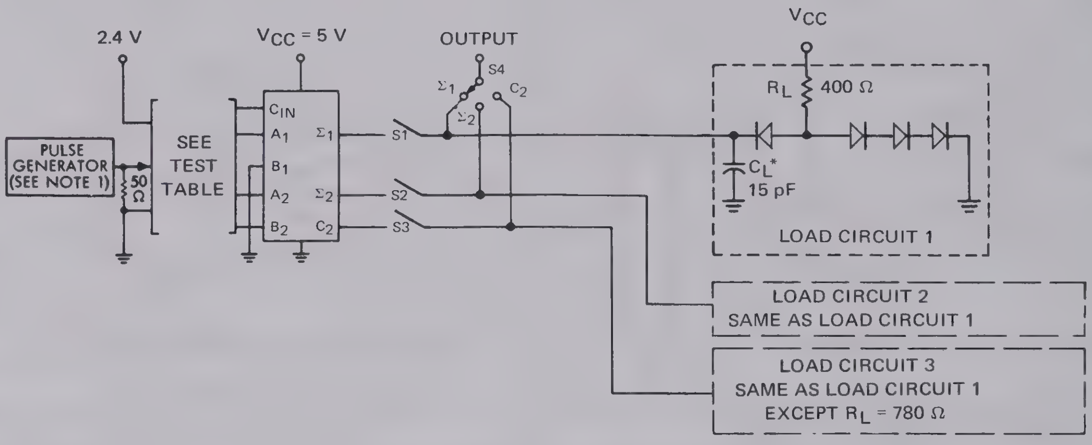
Fig. 4

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

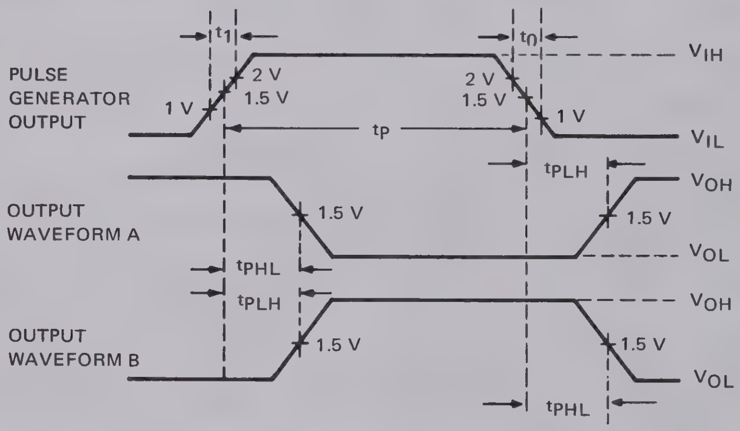
SWITCHING CHARACTERISTICS

TEST CIRCUIT


2.4 V
V_{CC} = 5 V
OUTPUT
V_{CC}
PULSE GENERATOR (SEE NOTE 1)
50 Ω
SEE TEST TABLE
C_{IN}
A_1
B_1
A_2
B_2
Σ_1
Σ_2
C_2
S1
S2
S3
S4
R_L 400 Ω
C_L*
15 pF
LOAD CIRCUIT 1
LOAD CIRCUIT 2
SAME AS LOAD CIRCUIT 1
LOAD CIRCUIT 3
SAME AS LOAD CIRCUIT 1
EXCEPT R_L = 780 Ω

*C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS


PULSE GENERATOR OUTPUT
OUTPUT WAVEFORM A
OUTPUT WAVEFORM B
t_1
t_0
V_{IH}
V_{IL}
2 V
1.5 V
1 V
t_p
t_{PLH}
t_{PHL}
V_{OH}
V_{OL}
1.5 V

SWITCHING TIMES TEST TABLE (SEE NOTE 5)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S4)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3
1	t_{PLH}	C_{IN}	Σ_1 (WAVEFORM A)	A_1	A_2, B_1, B_2	CLOSED	OPEN	OPEN
2	t_{PHL}							
3	t_{PLH}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2 and C_{IN}	OPEN	CLOSED	OPEN
4	t_{PHL}							
5	t_{PLH}	C_{IN}	Σ_2 (WAVEFORM A)	A_1, A_2	B_1, B_2	OPEN	CLOSED	CLOSED
6	t_{PHL}							
7	t_{PLH}	C_{IN}	C_2 (WAVEFORM B)	A_1, A_2	B_1, B_2	OPEN	OPEN	CLOSED
8	t_{PHL}							

NOTES:

1. The generator has the following characteristics: $V_{IH} \geqslant 2.4$ V, $V_{IL} \leqslant 0.4$ V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200 ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. Inputs and outputs not otherwise specified are open.

Fig. A — SWITCHING TIMES

TTL/MSI 9383/5483, 7483

4-BIT BINARY FULL ADDER

DESCRIPTION – The TTL/MSI 9383/5483,7483 is a Full Adder which performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium to high speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilized high speed, high fan out TTL. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

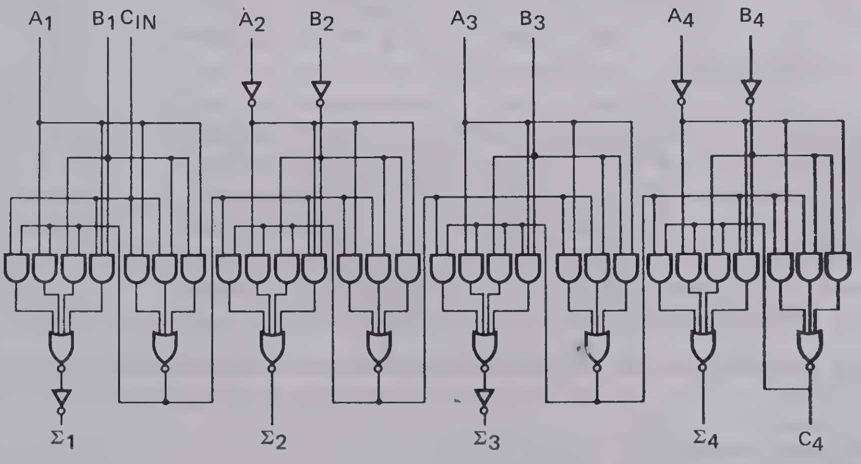
Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

PIN NAMES		LOADING
A_1,B_1,A_3,B_3	Data Inputs	4 U.L.
A_2,B_2,A_4,B_4	Data Inputs	1 U.L.
C_{IN}	Carry Input	4 U.L.
$\Sigma_1,\Sigma_2,\Sigma_3,\Sigma_4$	Sum Outputs	10 U.L.
C_4	Carry Out Bit 4	5 U.L.

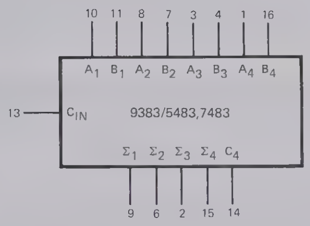
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM



A1
B1
CIN
A2
B2
A3
B3
A4
B4
Σ1
Σ2
Σ3
Σ4
C4

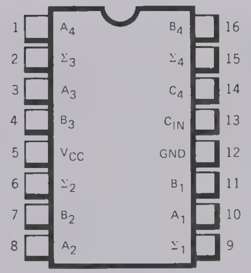
LOGIC SYMBOL



10
11
8
7
3
4
1
16
A1
B1
A2
B2
A3
B3
A4
B4
13
CIN
9383/5483,7483
Σ1
Σ2
Σ3
Σ4
C4
9
6
2
15
14

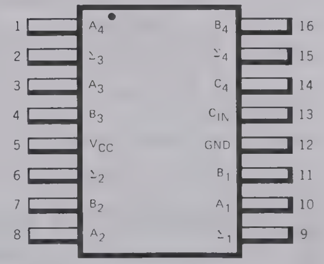
V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



1
A4
2
Σ3
3
A3
4
B3
5
VCC
6
Σ2
7
B2
8
A2
16
B4
15
Σ4
14
C4
13
CIN
12
GND
11
B1
10
A1
9
Σ1

FLATPAK (TOP VIEW)



1
A4
2
Σ3
3
A3
4
B3
5
VCC
6
Σ2
7
B2
8
A2
16
B4
15
Σ4
14
C4
13
CIN
12
GND
11
B1
10
A1
9
Σ1

Positive logic: See truth table

TRUTH TABLE (See Note 1)

INPUT				OUTPUT					
				WHEN $C_{IN} = 0$ / WHEN $C_2 = 0$			WHEN $C_{IN} = 1$ / WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_3	C_2 / C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE:
1. Input conditions at A_1, A_2, B_1, B_2 and C_{IN} are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4 and C_4.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9383XM/5483XM			9383XC/7483XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Outputs	C_4,			5.0			5.0	U. L.
	Σ_1, Σ_2, Σ_3 or Σ_4			10			10	U. L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}		1 & 2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = See Fig.2		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = See Fig.1		1
I_{IH}	Input HIGH Current at A_1, A_3, B_1, B_3 or C_{IN}			160	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at A_2, A_4, B_2 or B_4			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at A_1, A_3, B_1, B_3, or C_{IN}			−6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at A_2, A_4, B_2 or B_4			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
I_{OS}	Output Short Circuit Current at Σ_1, Σ_2, Σ_3 or Σ_4 (Note 3)	−20		−55	mA	9383/5483	V_{CC} = MAX.	4
		−18		−55	mA	9383/7483		
	Output Short Circuit Current at C_4 (Note 3)	−20		−70	mA	9383/5483	V_{CC} = MAX.	4
		−18		−70	mA	9383/7483		
I_{CC}	Supply Current		78	110	mA	9383/5483	V_{CC} = MAX.	3
			78	128	mA	9383/7483		

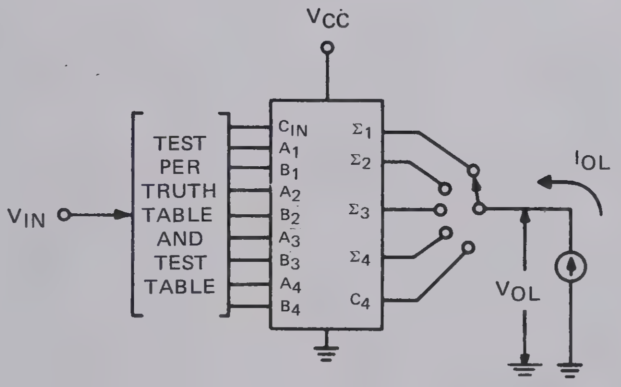
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	FIGURE A TEST NO.
t_{PLH}	C_{IN} to Σ_1			34	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	1
t_{PHL}				40			2
t_{PLH}	C_{IN} to Σ_2			38	ns		3
t_{PHL}				42			4
t_{PLH}	C_{IN} to Σ_3			50	ns		5
t_{PHL}				60			6
t_{PLH}	C_{IN} to Σ_4			55	ns		7
t_{PHL}				55			8
t_{PLH}	C_{IN} to C_4		35	48	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 780Ω	9
t_{PHL}			22	32			10
t_{PLH}	A_2 or B_2 to Σ_2			40	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	11 & 13
t_{PHL}				35			12 & 14
t_{PLH}	A_4 or B_4 to Σ_4			40	ns		15 & 17
t_{PHL}				35			16 & 18

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT*



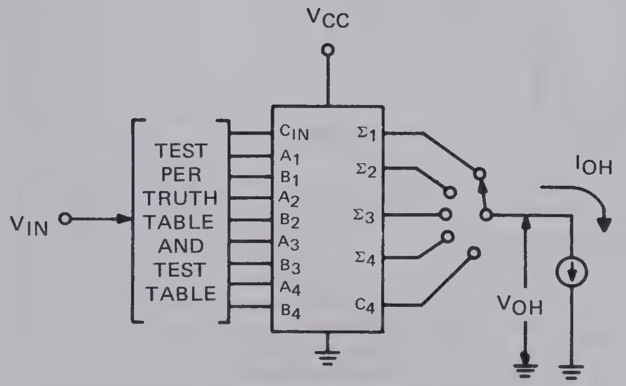
V_{CC}
TEST PER TRUTH TABLE AND TEST TABLE
V_{IN}
C_{IN}
A_1
B_1
A_2
B_2
A_3
B_3
A_4
B_4
Σ_1
Σ_2
Σ_3
Σ_4
C_4
I_{OL}
V_{OL}

TEST TABLE

OUTPUT UNDER TEST	I_{OL}
Σ_1, Σ_2, Σ_3, or Σ_4	16 mA
C_4	8 mA

1. Each input or output is tested separately.

Fig. 1



V_{CC}
TEST PER TRUTH TABLE AND TEST TABLE
V_{IN}
C_{IN}
A_1
B_1
A_2
B_2
A_3
B_3
A_4
B_4
Σ_1
Σ_2
Σ_3
Σ_4
C_4
I_{OH}
V_{OH}

TEST TABLE

OUTPUT UNDER TEST	I_{OH}
Σ_1, Σ_2, Σ_3, or Σ_4	–400 μA
C_4	–200 μA

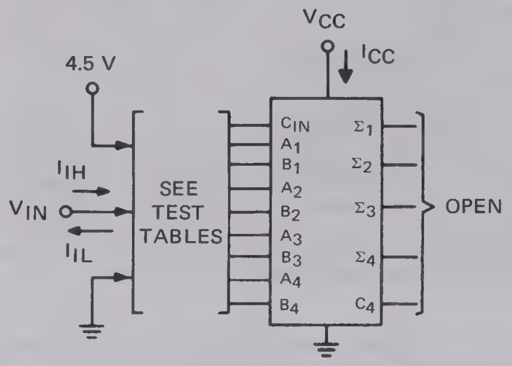
1. Each input or output is tested separately.

Fig. 2

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (continued)


4.5 V
V_{CC}
I_{CC}
I_{IH}
V_{IN}
I_{IL}
SEE TEST TABLES
C_{IN}
A_1
B_1
A_2
B_2
A_3
B_3
A_4
B_4
Σ_1
Σ_2
Σ_3
Σ_4
C_4
OPEN

I_{IL} TEST TABLE

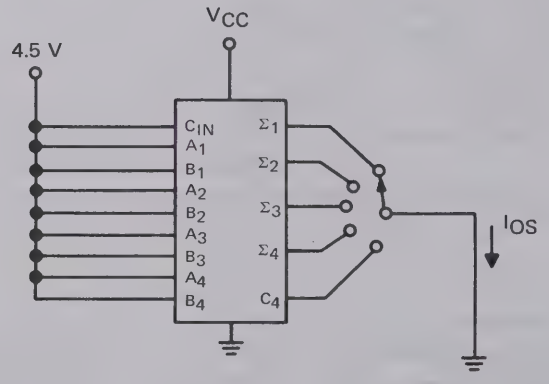
APPLY V_{IN} TEST I_{IN}	APPLY 4.5 V
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

I_{IH} TEST TABLE

APPLY V_{IN} TEST I_{IN}	GND
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, A_3, A_4, and C_{IN}; and ground B_1, B_2, B_3, and B_4.

Fig. 3


4.5 V
V_{CC}
C_{IN}
A_1
B_1
A_2
B_2
A_3
B_3
A_4
B_4
Σ_1
Σ_2
Σ_3
Σ_4
C_4
I_{OS}

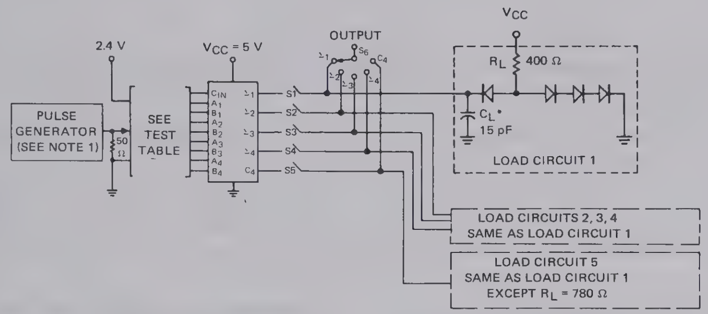
1. Each output is tested separately.

Fig. 4

*Arrows indicate actual direction of current flow.

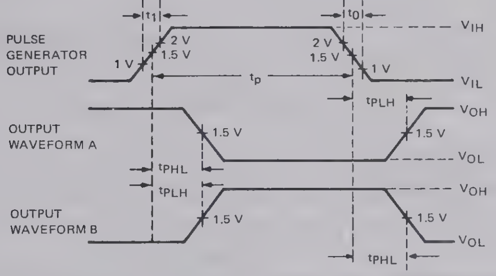
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS


2.4 V
PULSE GENERATOR (SEE NOTE 1)
50 Ω
SEE TEST TABLE
$V_{CC} = 5$ V
C_{IN}
A_1
B_1
A_2
B_2
A_3
B_3
A_4
B_4
Σ_1
Σ_2
Σ_3
Σ_4
C_4
S1
S2
S3
S4
S5
OUTPUT
S6
V_{CC}
R_L 400 Ω
C_L* 15 pF
LOAD CIRCUIT 1
LOAD CIRCUITS 2, 3, 4 SAME AS LOAD CIRCUIT 1
LOAD CIRCUIT 5 SAME AS LOAD CIRCUIT 1 EXCEPT $R_L = 780$ Ω

*C_L includes probe and jig capacitance.

TEST CIRCUIT


t_1
t_0
V_{IH}
PULSE GENERATOR OUTPUT
2 V
1.5 V
1 V
t_p
V_{IL}
t_{PLH}
V_{OH}
OUTPUT WAVEFORM A
1.5 V
V_{OL}
t_{PHL}
t_{PLH}
OUTPUT WAVEFORM B
t_{PHL}

VOLTAGE WAVEFORMS

TEST TABLE (SEE NOTE 5)

TEST NO.	PARA-METER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{PLH}	C_{IN}	Σ_1 (WAVEFORM A)	A_1	B_1, A_2, and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
2	t_{PHL}									
3	t_{PLH}	C_{IN}	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
4	t_{PHL}									
5	t_{PLH}	C_{IN}	Σ_3 (WAVEFORM A)	A_1, A_2, and A_3	B_1, B_2, and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
6	t_{PHL}									
7	t_{PLH}	C_{IN}	Σ_4 (WAVEFORM A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
8	t_{PHL}									
9	t_{PLH}	C_{IN}	C_4 (WAVEFORM B)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
10	t_{PHL}									
11	t_{PLH}	A_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2, and C_{IN}	OPEN	CLOSED	OPEN	OPEN	OPEN
12	t_{PHL}									
13	t_{PLH}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2, and C_{IN}	OPEN	CLOSED	OPEN	OPEN	OPEN
14	t_{PHL}									
15	t_{PLH}	A_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
16	t_{PHL}									
17	t_{PLH}	B_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN
18	t_{PHL}									

NOTES:

1. Pulse generator output pulse characteristics: $V_{IH} \leqslant 2.4$ V, $V_{IL} \leqslant 0.4$ V, $t_1 = 8$ to 15 ns, $t_0 = 3$ to 5 ns, PRR = 1 MHz, $t_p = 200$ ns, and $Z_{out} \approx 50$ Ω.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. Inputs and outputs not otherwise specified are open.

Fig. A – SWITCHING TIMES

TTL/MSI 9386

4-BIT QUAD EXCLUSIVE-NOR

DESCRIPTION — The 9386 consists of four independent Exclusive-NOR gates with open collector outputs. Single 1-bit comparisons may be made with each gate, or multiple bit comparisons may be made by connecting the outputs of the four gates together. Typical power dissipation is 170 mW.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

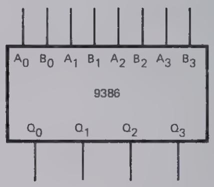
PIN NAMES		**LOADING**
A_0 to A_3, B_0 to B_3	Inputs	2.0 U.L.
Q_0 to Q_3	Outputs	15 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

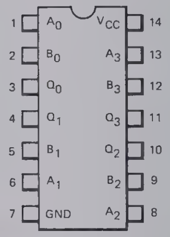
TRUTH TABLE

INPUTS A	INPUTS B	OUTPUT Q
L	L	H
H	L	L
L	H	L
H	H	H

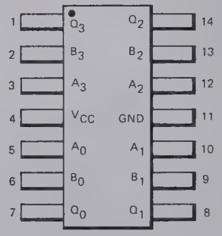
LOGIC SYMBOL


A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3
9386
Q_0 Q_1 Q_2 Q_3

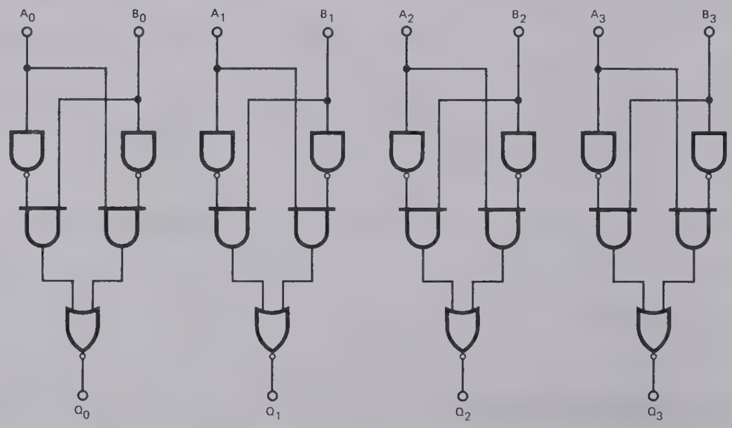
CONNECTION DIAGRAM
DIP (TOP VIEW)


1 A_0
2 B_0
3 Q_0
4 Q_1
5 B_1
6 A_1
7 GND
14 V_{CC}
13 A_3
12 B_3
11 Q_3
10 Q_2
9 B_2
8 A_2

FLATPAK (TOP VIEW)


1 Q_3
2 B_3
3 A_3
4 V_{CC}
5 A_0
6 B_0
7 Q_0
14 Q_2
13 B_2
12 A_2
11 GND
10 A_1
9 B_1
8 Q_1

LOGIC DIAGRAM


A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3
Q_0 Q_1 Q_2 Q_3

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9386XM			9386XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	CONDITIONS
			MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
I_{CEX}	Output HIGH Leakage Current				150	µA	V_{CC} = MIN., V_{IN} = V_{IH} V_{OUT} = 4.5 V
V_{OL}	Output LOW Voltage				0.4	Volts	V_{CC} = MIN., $V_{IN}(A)$ = 2.0 V, $V_{IN}(B)$ = 0.8 V, I_{OL} = 25 mA (Note 3)
I_{IH}	Input HIGH Current				80	µA	V_{CC} = MAX., $V_{IN}(A)$ = $V_{IN}(B)$ = 4.5 V (Note 4)
I_{IL}	Input LOW Current		–0.1		–3.2	mA	V_{CC} = MAX., $V_{IN}(A)$ = $V_{IN}(B)$ = 0.4 V (Note 5)
I_{CC}	Supply Current			32	47.5	mA	V_{CC} = 5.25 V, $V_{IN}(A)$ = $V_{IN}(B)$ = 0.4 V
V_{LV}	Input Latch Voltage	A Input	5.5			Volts	$I_{IN(A)}$ = 10 mA, $V_{IN(B)}$ = 0 V
		B Input	5.5			Volts	$V_{IN(A)}$ = 0 V, $I_{IN(B)}$ = 10 mA (Note 6)

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		18	25	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay Input to Output		18	25	ns	

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

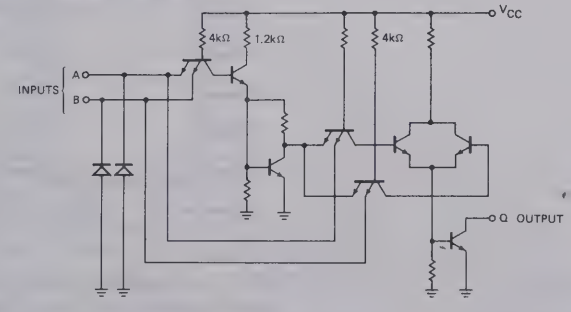
(3) Output sink current is supplied through a resistor to V_{CC}.

(4) A and B are tested separately. When A is 4.5 V, B is 0 V, and vice versa.

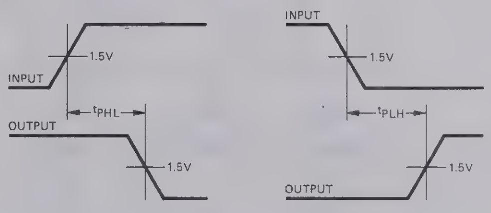
(5) A and B are tested separately. When A is 0.4 V, B is 5.25 V, and vice versa.

(6) This test guarantees operation free of input latch-up over the specified operating supply voltage range.

SCHEMATIC DIAGRAMS



SWITCHING CHARACTERISTICS



TTL/MSI 93H87/54H87, 74H87

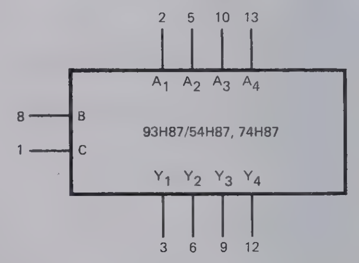
HIGH SPEED 4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT

DESCRIPTION — The 93H87/54H87, 74H87 will perform four functions; use of the B and C control inputs determine the function performed. A 4-bit binary number (A) can be transferred to the output (Y) in either true or complementary form. In addition the control inputs can also set all outputs to LOW or HIGH independent of the state of the data inputs.

PIN NAMES		**LOADING**
A_1, A_2, A_3, A_4	Data Inputs	1.0 U.L.
B, C	Control Inputs	1.0 U.L.
Y_1, Y_2, Y_3, Y_4	Outputs	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL

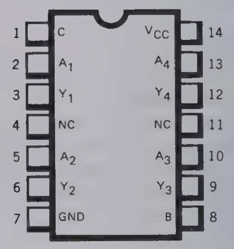

2
5
10
13
A_1 A_2 A_3 A_4
8
B
1
C
93H87/54H87, 74H87
Y_1 Y_2 Y_3 Y_4
3
6
9
12

V_{CC} = PIN 14
GND = PIN 7

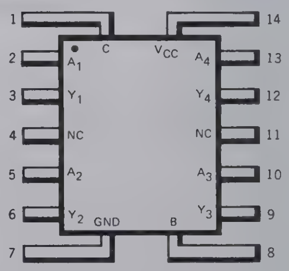
TRUTH TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y_1	Y_2	Y_3	Y_4
L	L	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$
L	H	A_1	A_2	A_3	A_4
H	L	H	H	H	H
H	H	L	L	L	L

CONNECTION DIAGRAM
DIP (TOP VIEW)

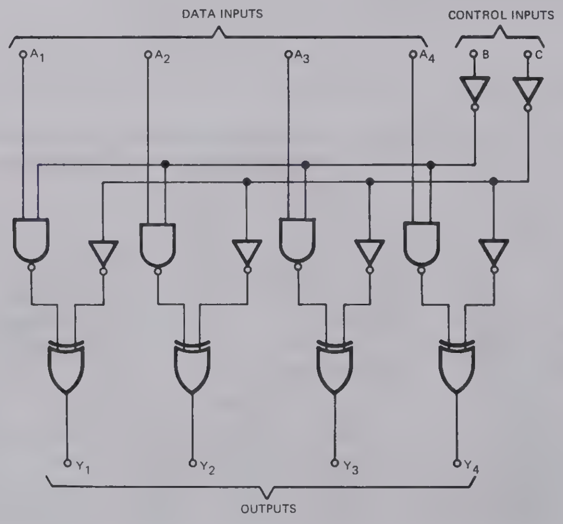

1 C
2 A_1
3 Y_1
4 NC
5 A_2
6 Y_2
7 GND
V_{CC} 14
A_4 13
Y_4 12
NC 11
A_3 10
Y_3 9
B 8

FLATPAK (TOP VIEW)


1
2 A_1
3 Y_1
4 NC
5 A_2
6 Y_2
7
C
V_{CC}
GND
B
14
A_4 13
Y_4 12
NC 11
A_3 10
Y_3 9
8

NC — No Internal Connection
Positive Logic: See Truth Table

LOGIC DIAGRAM


DATA INPUTS
CONTROL INPUTS
A_1
A_2
A_3
A_4
B
C
Y_1
Y_2
Y_3
Y_4
OUTPUTS

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either input voltage or input current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93H87XM/54H87XM			93H87XC/74H87XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	LOW Level			10			10	U.L.
	HIGH Level			20			20	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage	1
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −1.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	1
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V Each Input	2
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			−2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input	3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX., V_{OUT} = 0 V	4
I_{CC}	Supply Current		54	78	mA	93H87/54H87 V_{CC} = MAX.	5
			54	89	mA	93H87/74H87	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output (Data Inputs to Outputs)		14	20	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280 Ω	A
t_{PHL}	Turn On Delay Input to Output (Data Inputs to Outputs)		13	19	ns		
t_{PLH}	Turn Off Delay Input to Output (Control Inputs to Outputs)		17	25	ns		
t_{PHL}	Turn On Delay Input to Output (Control Inputs to Outputs)		17	25	ns		

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.

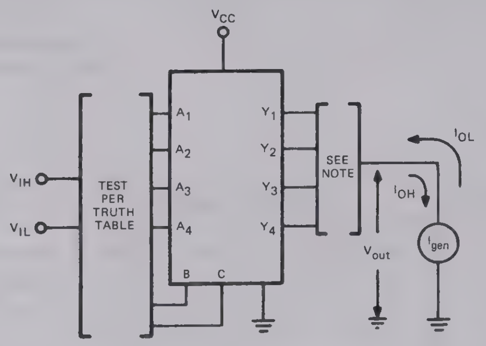
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time.

(4) These voltage values are with respect to network ground terminal.

PARAMETER MEASUREMENT INFORMATION

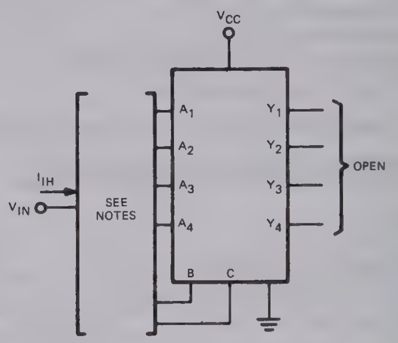
DC TEST CIRCUITS*



V_{CC}
V_{IH}
V_{IL}
TEST PER TRUTH TABLE
A_1
A_2
A_3
A_4
Y_1
Y_2
Y_3
Y_4
B
C
SEE NOTE
I_{OL}
I_{OH}
V_{out}
I_{gen}

1. Each output is tested separately.

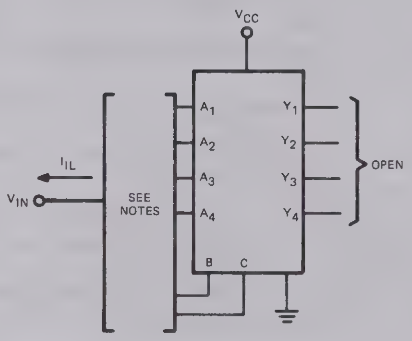
Fig. 1



V_{CC}
I_{IH}
V_{IN}
SEE NOTES
A_1
A_2
A_3
A_4
Y_1
Y_2
Y_3
Y_4
B
C
OPEN

1. Each input is tested separately.
2. When testing A_1, A_2, A_3 or A_4 input B is at 4.5 V.

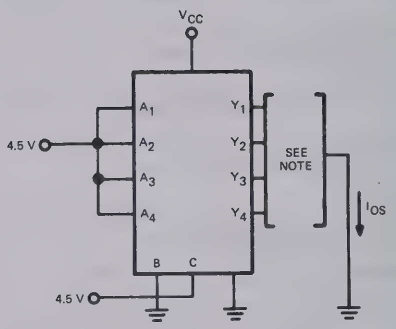
Fig. 2



V_{CC}
I_{IL}
V_{IN}
SEE NOTES
A_1
A_2
A_3
A_4
Y_1
Y_2
Y_3
Y_4
B
C
OPEN

1. Each input is tested separately.
2. When testing A_1, A_2, A_3 or A_4 input B is grounded.

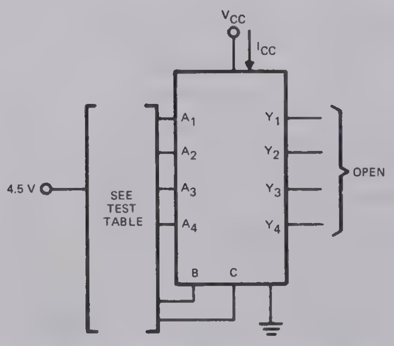
Fig. 3



V_{CC}
4.5 V
A_1
A_2
A_3
A_4
Y_1
Y_2
Y_3
Y_4
B
C
4.5 V
SEE NOTE
I_{OS}

1. Each output is tested separately.

Fig. 4



V_{CC}
I_{CC}
4.5 V
SEE TEST TABLE
A_1
A_2
A_3
A_4
Y_1
Y_2
Y_3
Y_4
B
C
OPEN

TEST TABLE

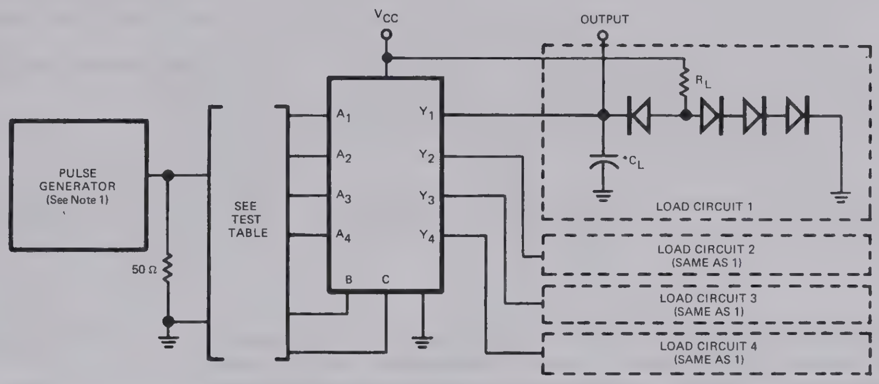
TEST NO.	APPLY 4.5 V	GROUND
1	A_1, A_2, A_3, A_4	B,C,
2	B, C	A_1, A_2, A_3, A_4

Fig. 5

*Arrows indicate actual direction of current flow.

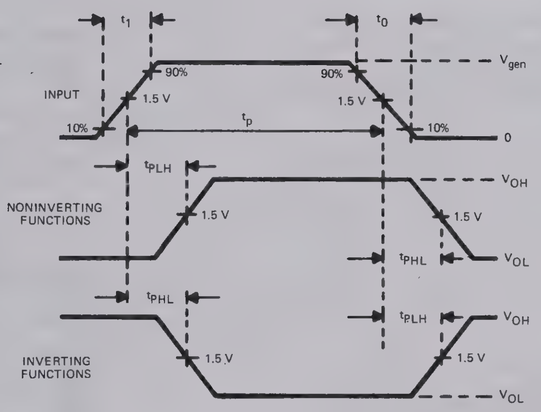
PARAMETER MEASUREMENT INFORMATION (cont'd)

SWITCHING CHARACTERISTICS


V_{CC}
OUTPUT
R_L
*C_L
PULSE GENERATOR (See Note 1)
50 Ω
SEE TEST TABLE
A1
A2
A3
A4
Y1
Y2
Y3
Y4
B
C
LOAD CIRCUIT 1
LOAD CIRCUIT 2 (SAME AS 1)
LOAD CIRCUIT 3 (SAME AS 1)
LOAD CIRCUIT 4 (SAME AS 1)

*C_L includes probe and jig capacitance.

TEST CIRCUIT


t1
t0
Vgen
90%
1.5 V
INPUT
10%
tp
0
tPLH
NONINVERTING FUNCTIONS
1.5 V
VOH
VOL
tPHL
tPHL
INVERTING FUNCTIONS
tPLH
VOH
VOL

VOLTAGE WAVEFORMS

TEST TABLE (See Note 2)

GND	INPUT	OUTPUT
B, C	A1	Y1
B, C	A2	Y2
B, C	A3	Y3
B, C	A4	Y4
C	B	Y1
C	B	Y2
C	B	Y3
C	B	Y4
B	C	Y1
B	C	Y2
B	C	Y3
B	C	Y4

NOTES:

1. The pulse generator has the following characteristics: $V_{gen} = 3$ V, $t_1 = t_0 = 7$ ns, $t_p = 500$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
2. Inputs not specified are open.

Fig. A – SWITCHING TIMES

TTL/MSI 9390/5490, 7490
DECADE COUNTER

DESCRIPTION — The TTL/MSI 9390/5490, 7490 is a Decade Counter which consists of four dual rank, master slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Count inputs are inhibited, and all outputs are returned to logical zero or a binary coded decimal (BCD) count of 9 through gated direct reset lines. The output from flip-flop A is not internally connected to the succeeding stages, therefore the count may be separated into these independent count modes:

A. If used as a binary coded decimal decade counter, the $\overline{CP}_{BD}$ input must be externally connected to the Q_A output. The $\overline{CP}_A$ input receives the incoming count, and a count sequence is obtained in accordance with the BCD count for nine's complement decimal application.

B. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the Q_D output must be externally connected to the $\overline{CP}_A$ input. The input count is then applied at the $\overline{CP}_{BD}$ input and a divide-by-ten square wave is obtained at output Q_A.

C. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The $\overline{CP}_{BD}$ input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

PIN NAMES		LOADING
R_0	Reset-Zero Inputs	1 U.L.
R_9	Reset-Nine Inputs	1 U.L.
$\overline{CP}_A$	Clock Input	2 U.L.
$\overline{CP}_{BD}$	Clock Input	4 U.L.
Q_A, Q_B, Q_C, Q_D	Outputs	10 U.L.

1 Unit Load (U.L.) = 40µA HIGH/1.6mA LOW.

TRUTH TABLES

BCD COUNT SEQUENCE (Note 1)

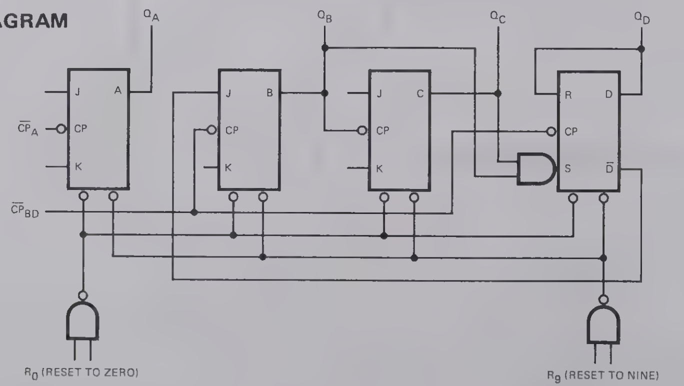
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

RESET/COUNT (see Note 2)

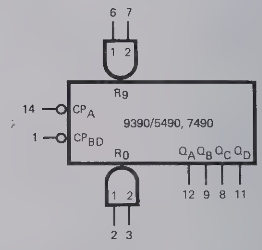
RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D Q_C Q_B Q_A
H	H	L	X	L L L L
H	H	X	L	L L L L
X	X	H	H	H L L H
X	L	X	L	COUNT
L	X	L	X	COUNT
L	X	X	L	COUNT
X	L	L	X	COUNT

NOTES:
1. Output Q_A connected to input CP_{BD} for BCD count.
2. X indicates that either a HIGH level or a LOW level may be present.

LOGIC DIAGRAM

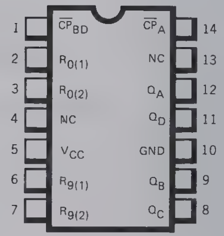

Q_A
Q_B
Q_C
Q_D
J
A
CP
K
$\overline{CP}_A$
J
B
CP
K
J
C
CP
K
R
D
CP
S
$\overline{D}$
$\overline{CP}_{BD}$
R_0 (RESET TO ZERO)
R_9 (RESET TO NINE)

LOGIC SYMBOL

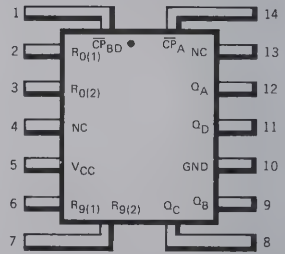

6 7
1 2
R_9
14
CP_A
1
CP_{BD}
9390/5490, 7490
R_0
Q_A Q_B Q_C Q_D
1 2
12 9 8 11
2 3

V_{CC} = Pin 5
GND = Pin 10
NC = Pin 4, 13

CONNECTION DIAGRAM
DIP (TOP VIEW)


1
$\overline{CP}_{BD}$
$\overline{CP}_A$
14
2
$R_{0(1)}$
NC
13
3
$R_{0(2)}$
Q_A
12
4
NC
Q_D
11
5
V_{CC}
GND
10
6
$R_{9(1)}$
Q_B
9
7
$R_{9(2)}$
Q_C
8

FLAT PAK (TOP VIEW)


1
14
2
$R_{0(1)}$
$\overline{CP}_{BD}$
$\overline{CP}_A$
NC
13
3
$R_{0(2)}$
Q_A
12
4
NC
Q_D
11
5
V_{CC}
GND
10
6
$R_{9(1)}$
$R_{9(2)}$
Q_C
Q_B
9
7
8

Positive logic: See Truth Table.
NC — No internal connection.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9390XM/5490XM			9390XC/7490XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N (Note 5)			10			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			50			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Input $\overline{CP}_A$			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Input $\overline{CP}_{BD}$			160	µA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Input $\overline{CP}_A$			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Input $\overline{CP}_{BD}$			−6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9390/5490	V_{CC} = MAX.	5
		−18		−57	mA	9390/7490		
I_{CC}	Supply Current		32	46	mA	9390/5490	V_{CC} = MAX.	3
			32	53	mA	9390/7490		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Frequency of Input Count Pulse	10	18		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	
t_{PLH}	Turn Off Delay from Input Count Pulse to Output Q_C		60	100	ns		A
t_{PHL}	Turn On Delay from Input Count Pulse to Output Q_C		60	100	ns		A

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

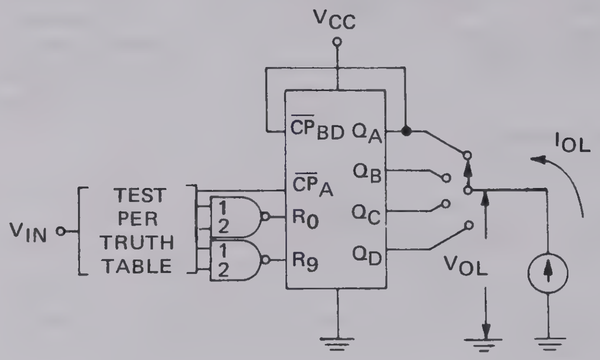
(3) Not more than one output should be shorted at a time.

(4) These voltage values are with respect to network ground terminal.

(5) Fan out from output Q_A to input $\overline{CP}_{BD}$ and to 10 additional series 54/74 loads is permitted.

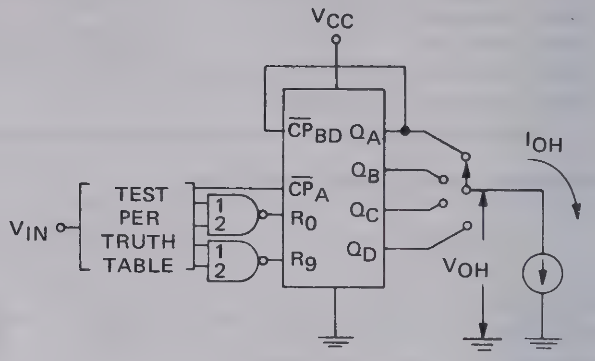
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT*


VCC
CPBD
QA
QB
QC
QD
CPA
R0
R9
1
2
1
2
VIN
TEST PER TRUTH TABLE
IOL
VOL

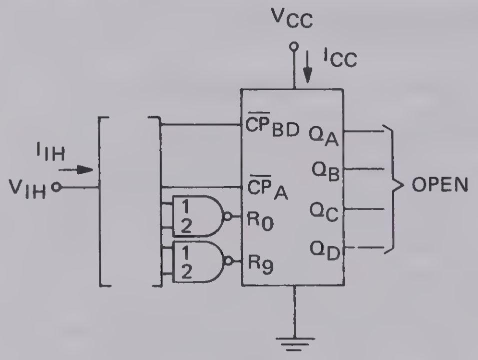
1. Each output is tested in the LOW level state.

Fig. 1


VCC
CPBD
QA
QB
QC
QD
CPA
R0
R9
1
2
1
2
VIN
TEST PER TRUTH TABLE
IOH
VOH

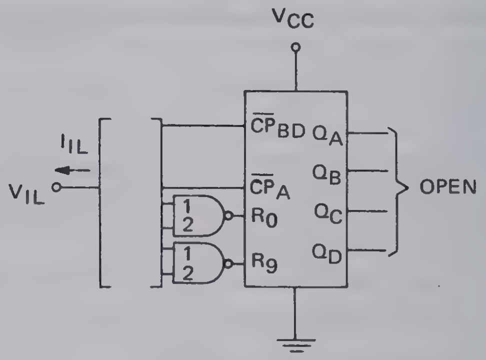
1. Each output is tested in the HIGH level state.

Fig. 2


VCC
ICC
IIH
VIH
CPBD
QA
QB
QC
QD
CPA
R0
R9
1
2
1
2
OPEN

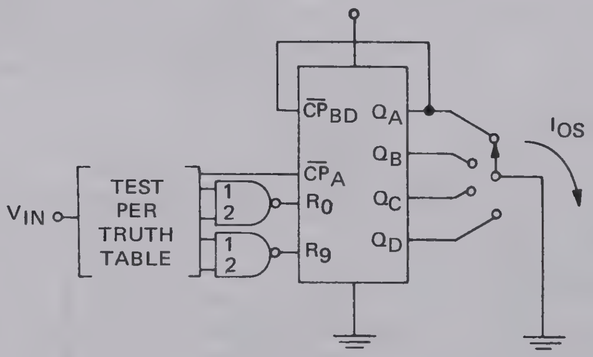
1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ ground $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ ground $R_{0(1)}$ or $R_{9(1)}$.
4. When testing I_{CC} reset all outputs to LOW level, ground all inputs, then measure I_{CC}.

Fig. 3


VCC
IIL
VIL
CPBD
QA
QB
QC
QD
CPA
R0
R9
1
2
1
2
OPEN

1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ apply 4.5 V to $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ apply 4.5 V to $R_{0(1)}$ or $R_{9(1)}$.

Fig. 4


CPBD
QA
QB
QC
QD
CPA
R0
R9
1
2
1
2
VIN
TEST PER TRUTH TABLE
IOS

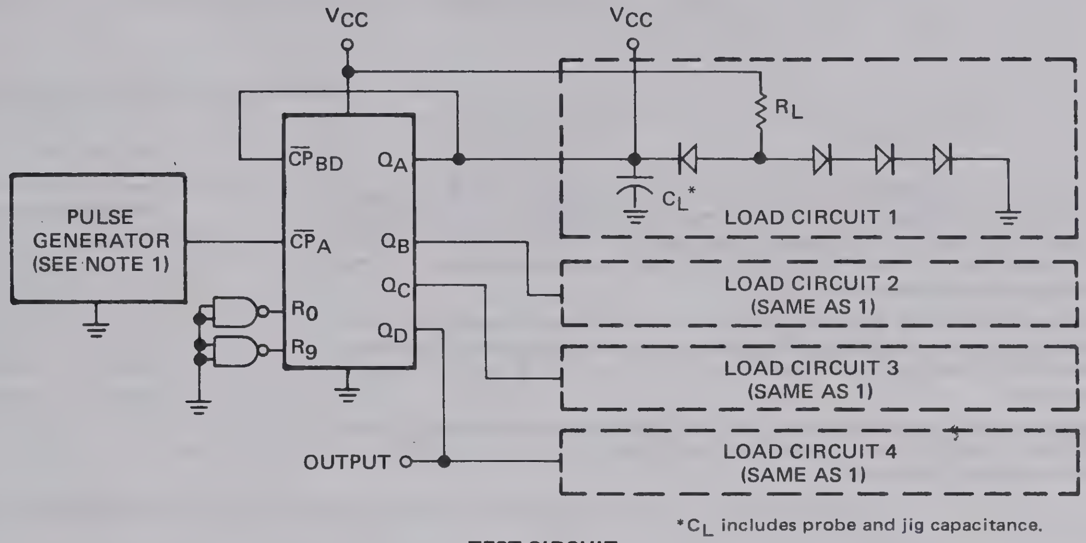
1. Each output is tested in the HIGH level state.

Fig. 5

*Arrows indicate actual direction of current flow.

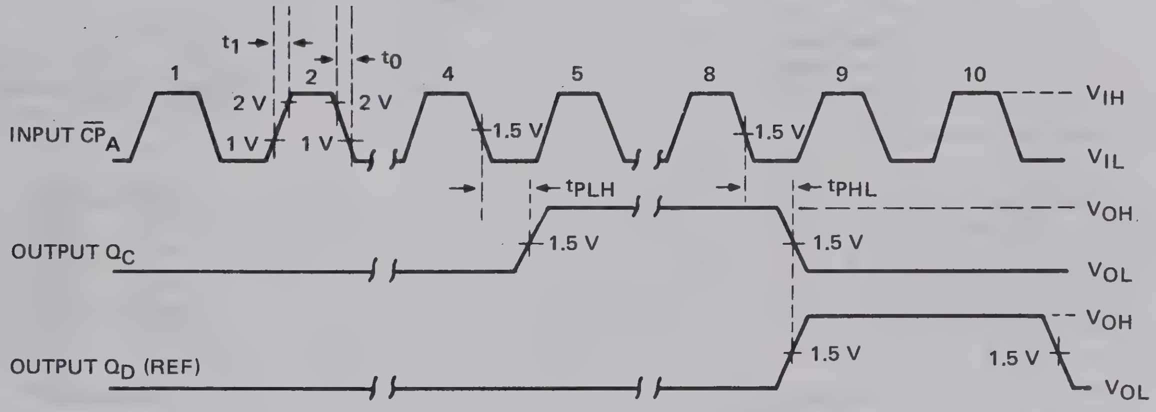
PARAMETER MEASUREMENT INFORMATION (Con't.)

SWITCHING CHARACTERISTICS


VCC
VCC
RL
$\overline{CP}_{BD}$
Q_A
PULSE GENERATOR (SEE NOTE 1)
$\overline{CP}_A$
Q_B
Q_C
R_0
R_9
Q_D
C_L*
LOAD CIRCUIT 1
LOAD CIRCUIT 2 (SAME AS 1)
LOAD CIRCUIT 3 (SAME AS 1)
LOAD CIRCUIT 4 (SAME AS 1)
OUTPUT

*C_L includes probe and jig capacitance.

TEST CIRCUIT


t_1
t_0
1
2
4
5
8
9
10
2 V
2 V
1 V
1 V
1.5 V
1.5 V
V_{IH}
V_{IL}
INPUT $\overline{CP}_A$
t_{PLH}
t_{PHL}
V_{OH}
V_{OL}
OUTPUT Q_C
1.5 V
1.5 V
V_{OH}
V_{OL}
OUTPUT Q_D (REF)
1.5 V
1.5 V

VOLTAGE WAVEFORMS

NOTES:

1. The pulse generator has the following characteristics: $V_{gen} = 3$ V, $t_0 = t_1 \leqslant 15$ ns, $t_p = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation Delay = $\frac{t_{PHL} + t_{PLH}}{2}$
3. Voltage values are with respect to ground terminal.

Fig. A — SWITCHING TIMES

TTL/MSI 9391/5491, 7491

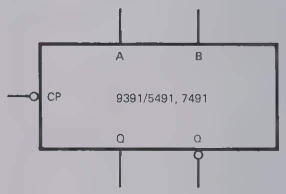
8-BIT SHIFT REGISTER

DESCRIPTION — The TTL/MSI 9391/5491, 7491 is a serial-in, serial-out, 8-Bit Shift Register utilizing TTL technology. It is composed of eight RS master/slave flip-flops, input gating, and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1.0V. Power dissipation is typically 175 mW; a full fan out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with other edge-triggered synchronous functions.

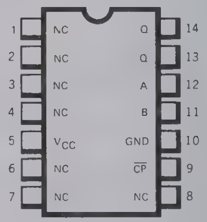
LOGIC SYMBOL


A
B
CP
9391/5491, 7491
Q
Q

PIN NAMES		LOADING
A, B	Data Inputs	1 U.L.
Q, $\overline{Q}$	Data Output	10 U.L.
$\overline{CP}$	Clock Input	1 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

CONNECTION DIAGRAM DIP (TOP VIEW)

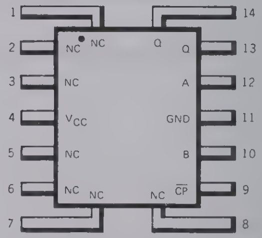

1 NC
2 NC
3 NC
4 NC
5 V_{CC}
6 NC
7 NC
8 NC
9 $\overline{CP}$
10 GND
11 B
12 A
13 Q
14 Q

TRUTH TABLE

t_n		t_{n+8}
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:
t_n = Bit time before clock pulse.
t_{n+8} = Bit time after 8 clock pulses.

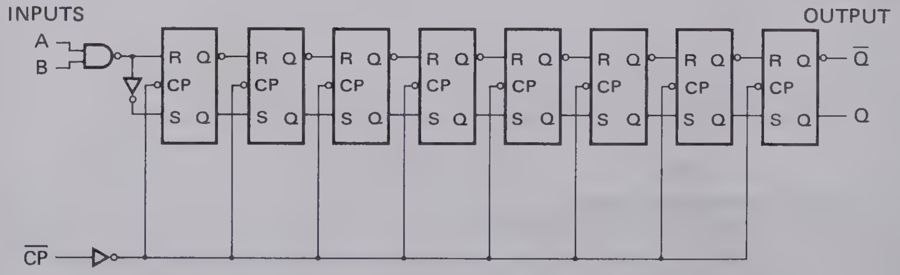
FLATPAK (TOP VIEW)


1
2 NC NC
3 NC
4 V_{CC}
5 NC
6 NC NC
7
8
9 NC $\overline{CP}$
10 B
11 GND
12 A
13 Q Q
14

NC—No Internal Connection

Positive logic: See truth table.

LOGIC DIAGRAM


INPUTS
A
B
R Q
CP
S Q
OUTPUT
$\overline{Q}$
Q
$\overline{CP}$

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9391XM/5491XM			9391XC/7491XC			UNITS
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Outputs			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. A)	25			25			ns
Input Setup Time, t_{setup} (See Fig. A)	25			25			ns
Input Hold Time, t_{hold} (See Fig. A)	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}		2
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., $I_{OH} = -0.4$ mA		1
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., $I_{OL} = 16$ mA		2
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., $V_{IN} = 2.4$ V		4
				1.0	mA	V_{CC} = MAX., $V_{IN} = 5.5$ V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., $V_{IN} = 0.4$V		3
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9391/5491	V_{CC} = MAX.	5
		−18		−57	mA	9391/7491	$V_{OUT} = 0$V	
I_{CC}	Supply Current		35	50	mA	9391/5491	V_{CC} = MAX.	6
			35	58	mA	9391/7491	$V_{IN} = 4.5$ V	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	10	18		MHz	$V_{CC} = 5.0$ V	
t_{PLH}	Turn Off Delay from Clock to Output		24	40	ns	$C_L = 15$ pF	A
t_{PHL}	Turn On Delay from Clock to Output		27	40	ns	$R_L = 400\Omega$	A

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.

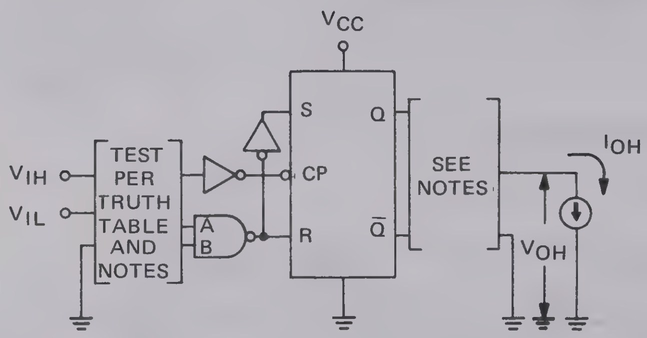
(2) Typical limits are at $V_{CC} = 5.0$ V, 25°C.

(3) Not more than one output should be shorted at a time.

(4) These voltage values are with respect to network ground terminal.

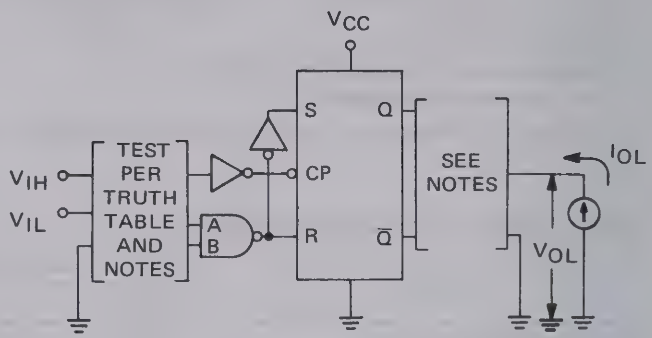
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*


V_{CC}
V_{IH}
V_{IL}
TEST PER TRUTH TABLE AND NOTES
A
B
S
CP
R
Q
$\overline{Q}$
SEE NOTES
I_{OH}
V_{OH}

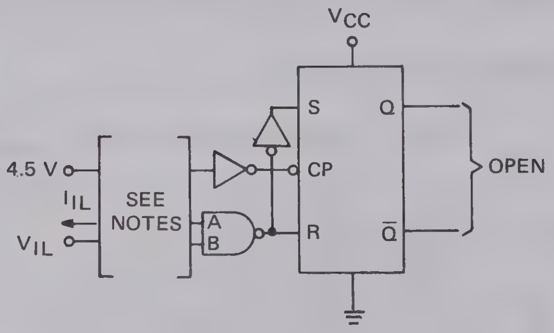
1. Each output is tested separately.
2. When testing V_{OH} and I_{OH} ground all inputs and the unused output, then measure parameters specified.

Fig. 1


V_{CC}
V_{IH}
V_{IL}
TEST PER TRUTH TABLE AND NOTES
A
B
S
CP
R
Q
$\overline{Q}$
SEE NOTES
I_{OL}
V_{OL}

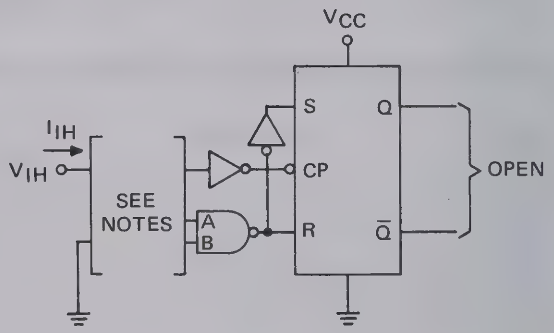
1. Each output is tested separately.
2. When testing V_{OL} and I_{OL} ground all inputs. Apply a momentary ground to the output to be tested then measure parameters specified.

Fig. 2


V_{CC}
4.5 V
I_{IL}
V_{IL}
SEE NOTES
A
B
S
CP
R
Q
$\overline{Q}$
OPEN

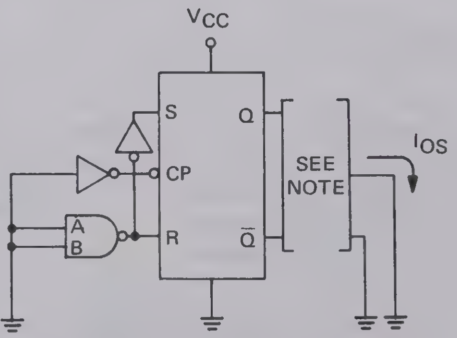
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

Fig. 3


V_{CC}
I_{IH}
V_{IH}
SEE NOTES
A
B
S
CP
R
Q
$\overline{Q}$
OPEN

1. When testing input A ground input B.
2. When testing input B ground input A.

Fig. 4


V_{CC}
A
B
S
CP
R
Q
$\overline{Q}$
SEE NOTE
I_{OS}

1. Ground the unused output then measure parameter specified.

Fig. 5

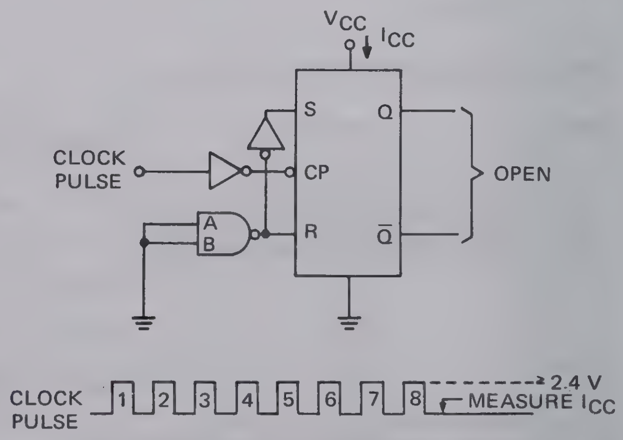
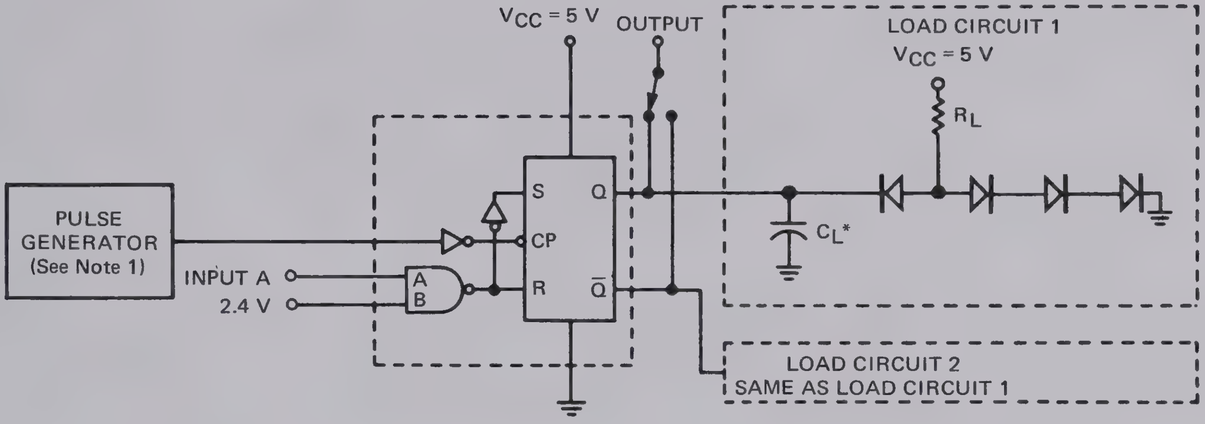

V_{CC}
I_{CC}
CLOCK PULSE
A
B
S
CP
R
Q
$\overline{Q}$
OPEN
CLOCK PULSE
1
2
3
4
5
6
7
8
≥ 2.4 V
MEASURE I_{CC}

Fig. 6

*Arrows indicate actual direction of current flow.

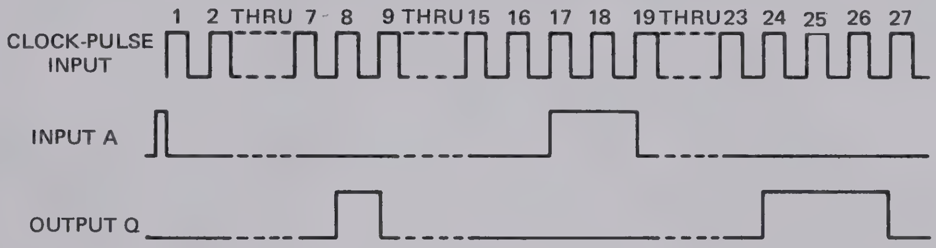
PARAMETER MEASUREMENT INFORMATION (Con't)

SWITCHING CHARACTERISTICS

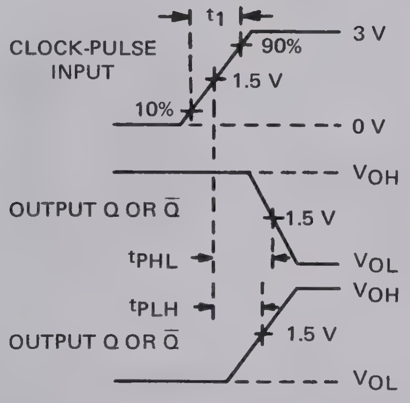

VCC = 5 V
OUTPUT
LOAD CIRCUIT 1
VCC = 5 V
RL
PULSE GENERATOR (See Note 1)
INPUT A
2.4 V
A
B
S
CP
R
Q
Q̄
CL*
LOAD CIRCUIT 2
SAME AS LOAD CIRCUIT 1

*C_L includes probe and jig capacitance

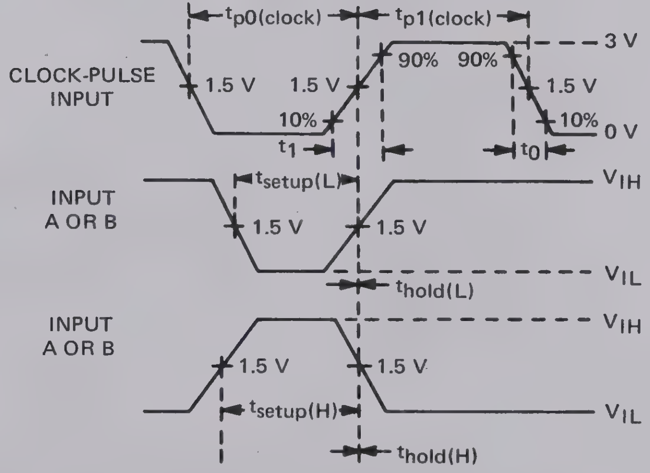
TEST CIRCUIT


1
2 THRU 7
8
9 THRU 15
16
17
18
19 THRU 23
24
25
26
27
CLOCK-PULSE INPUT
INPUT A
OUTPUT Q

TYPICAL INPUT/OUTPUT WAVEFORMS


t1
CLOCK-PULSE INPUT
90%
1.5 V
10%
3 V
0 V
VOH
OUTPUT Q OR Q̄
1.5 V
tPHL
VOL
tPLH
VOH
OUTPUT Q OR Q̄
1.5 V
VOL

PROPAGATION DELAY TIME VOLTAGE WAVEFORM


tp0(clock)
tp1(clock)
3 V
CLOCK-PULSE INPUT
1.5 V
1.5 V
90%
90%
1.5 V
10%
10%
0 V
t1
t0
tsetup(L)
INPUT A OR B
1.5 V
1.5 V
VIH
VIL
thold(L)
INPUT A OR B
1.5 V
1.5 V
VIH
VIL
tsetup(H)
thold(H)

SWITCHING TIME VOLTAGE WAVEFORM

NOTES:
1. The generator has the following characteristics: $V_{IL} \leq 0.3$ V, $V_{IH} \geq 2.4$V, $t_1 = t_0 = 10$ ns, $t_{p1(clock)} = 500$ ns, $t_{p0(clock)} = 500$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
2. Each output is tested separately.
3. Voltage values are with respect to network ground terminal.

Fig. A 9391/5491, 7491 SWITCHING TIMES

TTL/MSI 9392/5492, 7492
DIVIDE-BY-TWELVE COUNTER
(DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

DESCRIPTION — The TTL/MSI 9392/5492, 7492 is a 4-Bit Binary Counter consisting of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A grated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a LOW level. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

A. When used as a divide-by-twelve counter, output Q_A must be externally connected to input $\overline{CP}_{BC}$. The input count pulses are applied to input $\overline{CP}_A$. Simultaneous divisions of 2, 6 and 12 are performed at the Q_A, Q_C and Q_D outputs as shown in the truth table.

B. When used as a divide-by-six counter, the input count pulses are applied to input $\overline{CP}_{BC}$. Simultaneously, frequency divisions of 3 and 6 are available at the Q_C and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

These circuits are completely compatible with TTL and DTL logic families.

PIN NAMES		LOADING
R_0	Reset-Zero Inputs	1 U.L.
$\overline{CP}_A$	Clock Input	2 U.L.
$\overline{CP}_{BC}$	Clock Input	4 U.L.
Q_A, Q_B, Q_C, Q_D	Count Outputs	10 U.L.

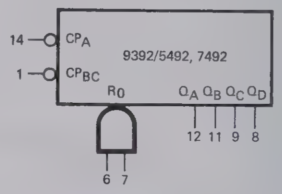
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

TRUTH TABLE
(See Notes 1, 2 and 3)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

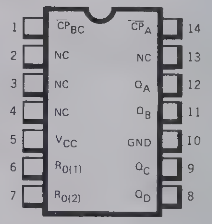
NOTES:
1. Output Q_A connected to input $\overline{CP}_{BC}$.
2. To reset all outputs to LOW level both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at HIGH level state.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a LOW level to count.

LOGIC SYMBOL

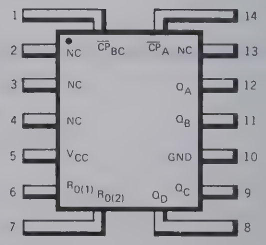

14
$\overline{CP}_A$
1
$\overline{CP}_{BC}$
9392/5492, 7492
R_0
Q_A Q_B Q_C Q_D
12 11 9 8
6 7

V_{CC} = Pin 5
GND = Pin 10
N.C. = Pins 2, 3, 4, 13

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 $\overline{CP}_{BC}$
2 NC
3 NC
4 NC
5 V_{CC}
6 $R_{0(1)}$
7 $R_{0(2)}$
14 $\overline{CP}_A$
13 NC
12 Q_A
11 Q_B
10 GND
9 Q_C
8 Q_D

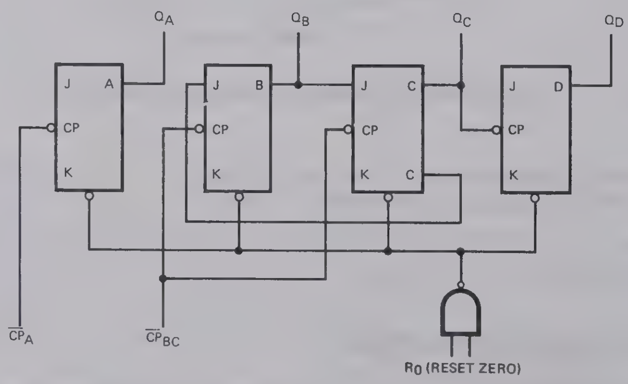
FLATPAK (TOP VIEW)


1
2 NC
3 NC
4 NC
5 V_{CC}
6 $R_{0(1)}$ $R_{0(2)}$
7
14
13 $\overline{CP}_{BC}$ $\overline{CP}_A$ NC
12 Q_A
11 Q_B
10 GND
9 Q_D Q_C
8

Positive logic: See truth table.

NC — No internal connection.

LOGIC DIAGRAM


Q_A
Q_B
Q_C
Q_D
J A CP K
J B CP K
J C CP K C
J D CP K
$\overline{CP}_A$
$\overline{CP}_{BC}$
R_0 (RESET ZERO)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9392XM/5492XM			9392XC/7492XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N (Note 5)			10			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			50			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}	2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA	2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	1
I_{IH}	Input HIGH Current at $R_{0(1)}$ or $R_{0(2)}$ Inputs			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Input $\overline{CP}_A$			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Input $\overline{CP}_{BC}$			160	µA	V_{CC} = MAX., V_{IN} = 2.4 V	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at $R_{0(1)}$ or $R_{0(2)}$ Inputs			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	4
	Input LOW Current at Input $\overline{CP}_A$			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	4
	Input LOW Current at Input $\overline{CP}_{BC}$			−6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V	4
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9392/5492 V_{CC} = MAX.	5
		−18		−57	mA	9392/7492 V_{OUT} = 0 V	
I_{CC}	Supply Current		31	44	mA	9392/5492 V_{CC} = MAX.	3
			31	51	mA	9392/7492 V_{IN} = 4.5 V	

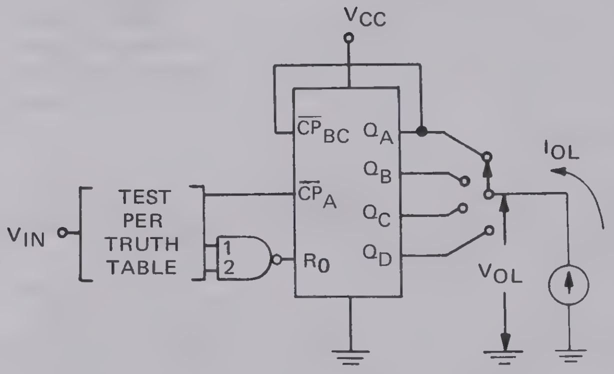
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Frequency of Input Count Pulse	10	18		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	
t_{PLH}	Turn Off Delay from Input Count Pulse to Output Q_D		60	100	ns		A
t_{PHL}	Turn On Delay from Input Count Pulse to Output Q_D		60	100	ns		A

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.
(5) Fan-out from output Q_A to input $\overline{CP}_{BC}$ and to 10 additional series 54/74 loads is permitted.

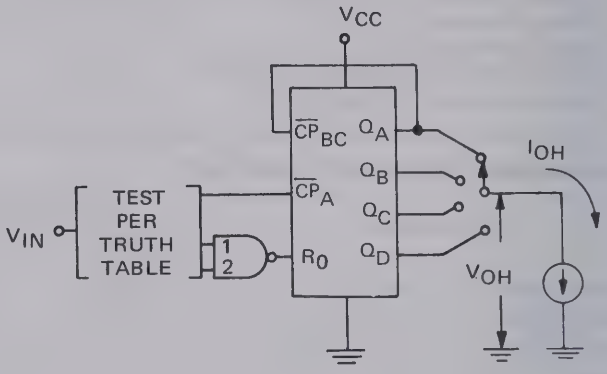
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT*


VCC
CPBC
QA
QB
QC
QD
CPA
R0
1
2
TEST
PER
TRUTH
TABLE
VIN
IOL
VOL

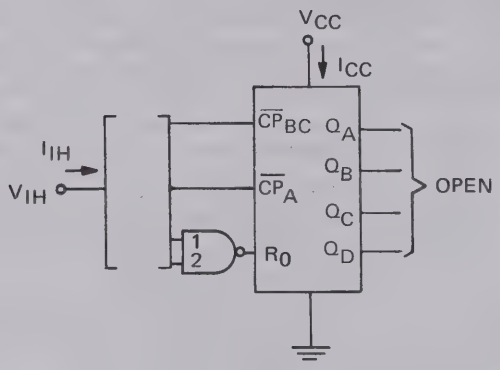
1. Each output is tested in the LOW level state.

Fig. 1


VCC
CPBC
QA
QB
QC
QD
CPA
R0
1
2
TEST
PER
TRUTH
TABLE
VIN
IOH
VOH

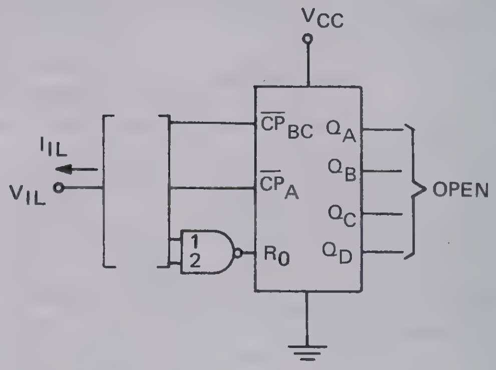
1. Each output is tested in the HIGH level state.

Fig. 2


VCC
ICC
IIH
VIH
CPBC
QA
QB
QC
QD
CPA
R0
1
2
OPEN

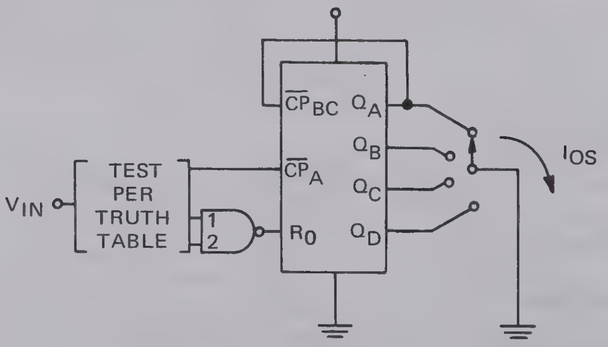
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} reset all outputs to LOW level, ground all inputs, then measure I_{CC}.

Fig. 3


VCC
IIL
VIL
CPBC
QA
QB
QC
QD
CPA
R0
1
2
OPEN

1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

Fig. 4


CPBC
QA
QB
QC
QD
CPA
R0
1
2
TEST
PER
TRUTH
TABLE
VIN
IOS

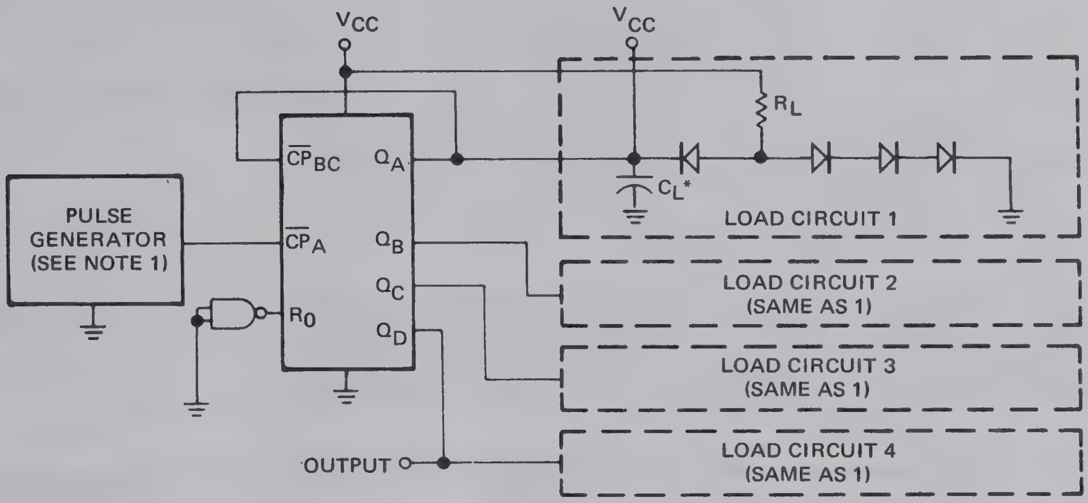
1. Each output is tested in the HIGH level state.

Fig. 5

*Arrows indicate actual direction of current flow.

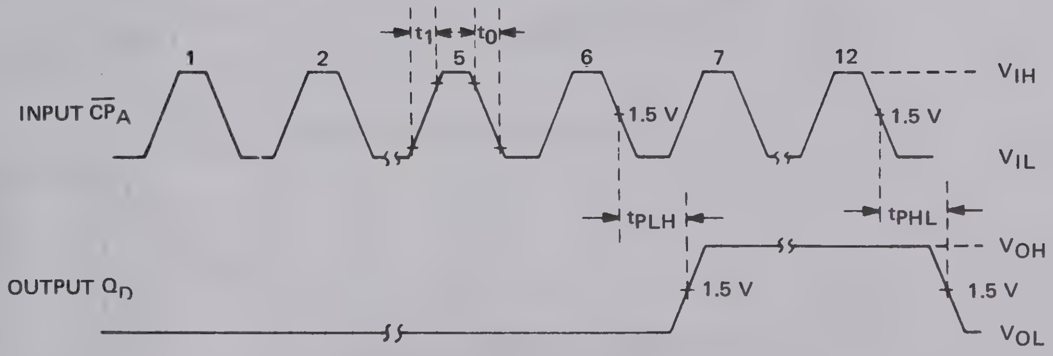
PARAMETER MEASUREMENT INFORMATION (Con't.)

SWITCHING CHARACTERISTICS


VCC
VCC
RL
CPBC
QA
CL*
LOAD CIRCUIT 1
PULSE GENERATOR (SEE NOTE 1)
CPA
QB
QC
QD
R0
LOAD CIRCUIT 2 (SAME AS 1)
LOAD CIRCUIT 3 (SAME AS 1)
LOAD CIRCUIT 4 (SAME AS 1)
OUTPUT

*C_L includes probe and jig capacitance

TEST CIRCUIT


t1
t0
1
2
5
6
7
12
VIH
INPUT CPA
1.5 V
1.5 V
VIL
tPLH
tPHL
VOH
OUTPUT QD
1.5 V
1.5 V
VOL

VOLTAGE WAVEFORMS

NOTES:

1. The pulse generator has the following characteristics: $V_{gen} = 3$ V, $t_0 = t_1 \leqslant 15$ ns, $t_p = 0.5$ μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation delay $= \dfrac{t_{PHL} + t_{PLH}}{2}$
3. Voltage values are with respect to ground terminal.

Fig. A – SWITCHING TIMES

TTL/MSI 9393/5493, 7493
4-BIT BINARY COUNTER

DESCRIPTION – The TTL/MSI 9393/5493, 7493 is a 4-Bit Binary Counter consisting of four master/slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a LOW level. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output Q_A must be externally connected to input $\overline{CP}_B$. The input count pulses are applied to input $\overline{CP}_A$. Simultaneously divisions of 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input $\overline{CP}_B$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with TTL and DTL logic families.

PIN NAMES		LOADING
R_0	Reset-Zero Input	1 U.L.
$\overline{CP}_A$	Clock (Active LOW going edge) Input	2 U.L.
$\overline{CP}_B$	Clock (Active LOW going edge) Input	2 U.L.
Q_A, Q_B, Q_C, Q_D	Outputs	10 U.L.

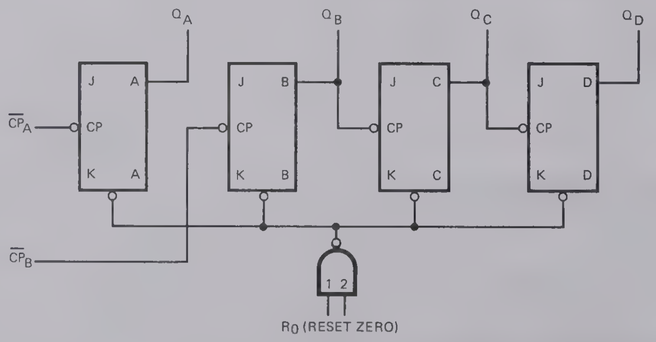
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE (See Notes 1, 2 and 3)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

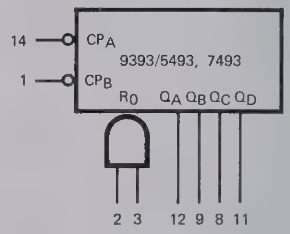
NOTES:
1. Output Q_A connected to input $\overline{CP}_B$.
2. To reset all outputs to LOW level both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at HIGH level state.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a LOW level to count.

LOGIC DIAGRAM



QA
QB
QC
QD
J
A
B
C
D
CP
K
CPA
CPB
1 2
R0 (RESET ZERO)

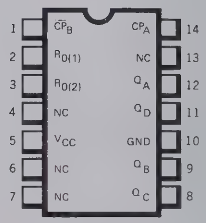
LOGIC SYMBOL



14
1
CPA
CPB
9393/5493, 7493
R0
QA QB QC QD
2 3
12 9 8 11

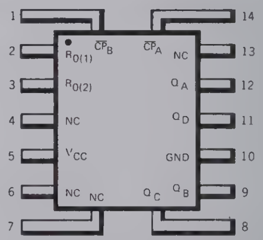
V_{CC} = Pin 5
GND = Pin 10
N.C. = Pins 4, 6, 7, 13

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 CPB
2 R0(1)
3 R0(2)
4 NC
5 VCC
6 NC
7 NC
14 CPA
13 NC
12 QA
11 QD
10 GND
9 QB
8 QC

FLATPAK (TOP VIEW)



1 CPB
2 R0(1)
3 R0(2)
4 NC
5 VCC
6 NC
7 NC
14 CPA
13 NC
12 QA
11 QD
10 GND
9 QB
8 QC

NC – No Internal Connection
Positive logic: See Truth Table

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9393XM/5493XM			9393XC/7493XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N (Note 5)			10			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			50			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts			1
V_{IL}	Input LOW Voltage			0.8	Volts			2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at $R_{0(1)}$ or $R_{0(2)}$ Inputs			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Inputs $\overline{CP}_A$ or $\overline{CP}_B$			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at $R_{0(1)}$ or $R_{0(2)}$ Inputs			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Inputs $\overline{CP}_A$ or $\overline{CP}_B$			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9393/5493	V_{CC} = MAX.	5
		−18		−57	mA	9393/7493	V_{OUT} = 0 V	
I_{CC}	Supply Current		32	46	mA	9393/5493	V_{CC} = MAX.	3
			32	53	mA	9393/7493	V_{IN} = 4.5 V	

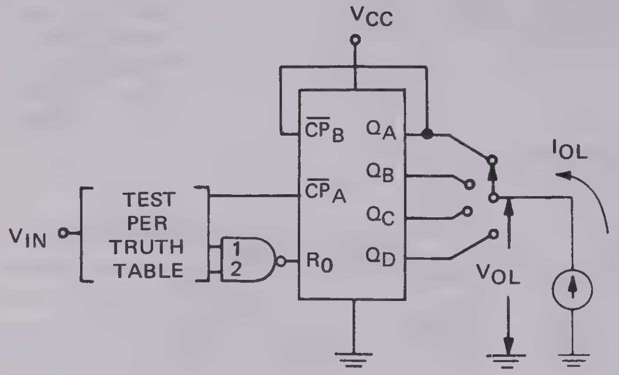
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Frequency of Input Count Pulse	10	18		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	
t_{PLH}	Turn Off Delay from Input Count Pulse to Output Q_D		75	135	ns		A
t_{PHL}	Turn On Delay from Input Count Pulse to Output Q_D		75	135	ns		A

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.
(5) Fan-out from output Q_A to input $\overline{CP}_B$ and to 10 additional series 54/74 loads is permitted.

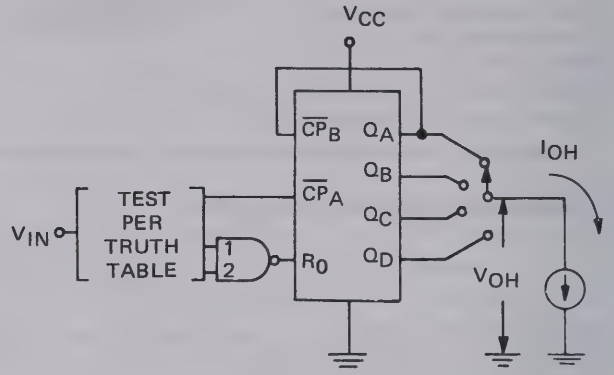
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*


V_{CC}
$\overline{CP}_B$
Q_A
Q_B
$\overline{CP}_A$
Q_C
R_0
Q_D
I_{OL}
V_{IN}
TEST PER TRUTH TABLE
1
2
V_{OL}

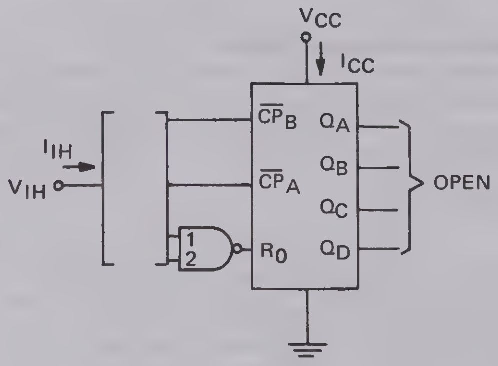
1. Each output is tested in the LOW level state.

Fig. 1


V_{CC}
$\overline{CP}_B$
Q_A
Q_B
$\overline{CP}_A$
Q_C
R_0
Q_D
I_{OH}
V_{IN}
TEST PER TRUTH TABLE
1
2
V_{OH}

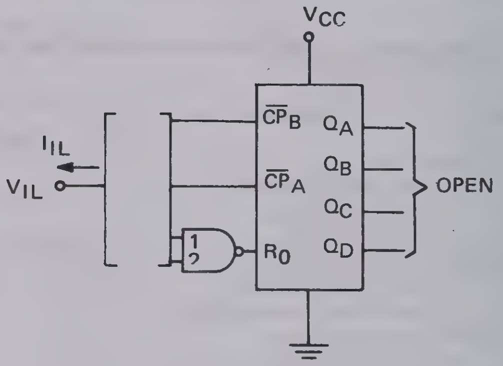
1. Each output is tested in the HIGH level state.

Fig. 2


V_{CC}
I_{CC}
$\overline{CP}_B$
Q_A
I_{IH}
Q_B
V_{IH}
$\overline{CP}_A$
OPEN
Q_C
1
2
R_0
Q_D

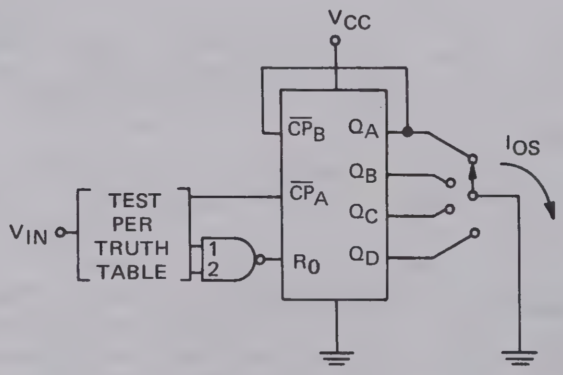
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} all inputs and outputs are open.

Fig. 3


V_{CC}
$\overline{CP}_B$
Q_A
I_{IL}
Q_B
V_{IL}
$\overline{CP}_A$
OPEN
Q_C
1
2
R_0
Q_D

1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

Fig. 4


V_{CC}
$\overline{CP}_B$
Q_A
I_{OS}
Q_B
$\overline{CP}_A$
Q_C
V_{IN}
TEST PER TRUTH TABLE
1
2
R_0
Q_D

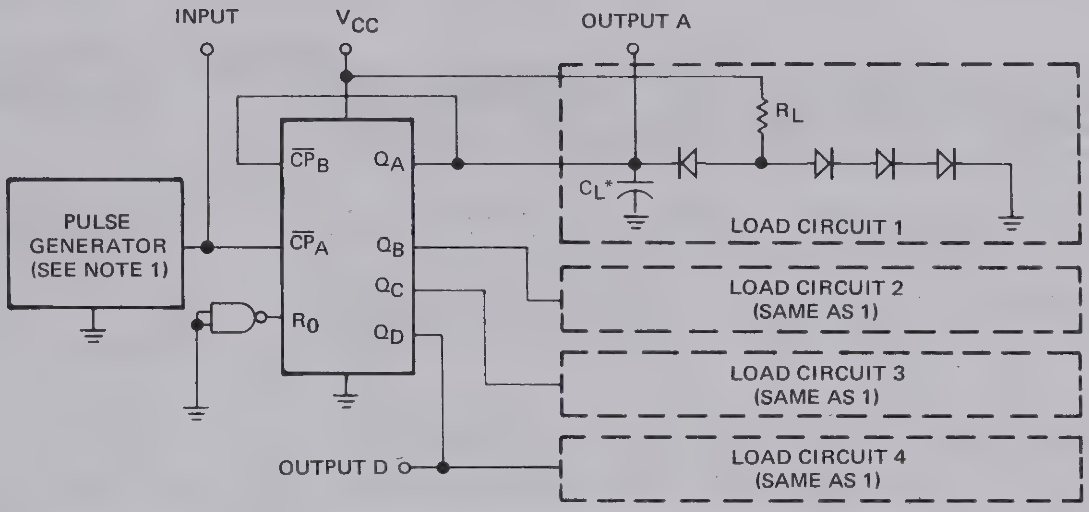
1. Each output is tested in the HIGH level state.

Fig. 5

*Arrows indicate actual direction of current flow.

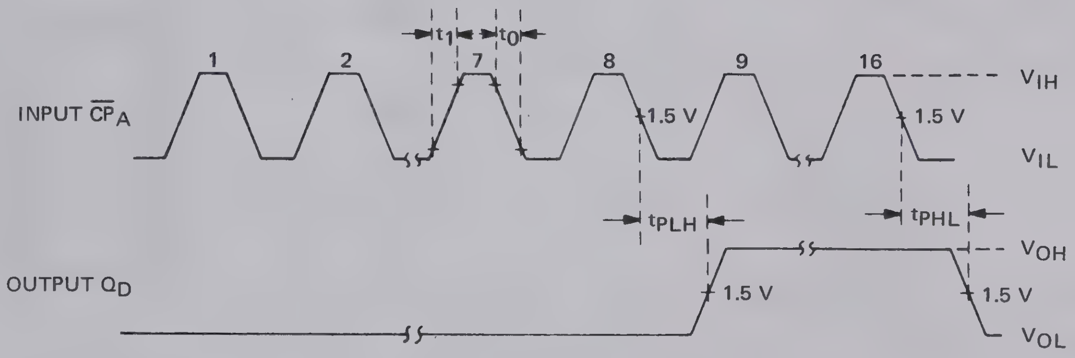
PARAMETER MEASUREMENT INFORMATION (con't.)

SWITCHING CHARACTERISTICS


INPUT
V_{CC}
OUTPUT A
R_L
$\overline{CP}_B$
Q_A
PULSE GENERATOR (SEE NOTE 1)
$\overline{CP}_A$
Q_B
Q_C
R_0
Q_D
C_L*
LOAD CIRCUIT 1
LOAD CIRCUIT 2 (SAME AS 1)
LOAD CIRCUIT 3 (SAME AS 1)
LOAD CIRCUIT 4 (SAME AS 1)
OUTPUT D

*C_L includes probe and jig capacitance

TEST CIRCUIT


t_1
t_0
1
2
7
8
9
16
V_{IH}
INPUT $\overline{CP}_A$
1.5 V
1.5 V
V_{IL}
t_{PLH}
t_{PHL}
V_{OH}
OUTPUT Q_D
1.5 V
1.5 V
V_{OL}

VOLTAGE WAVEFORMS

1. The pulse generator has the following characteristics: $V_{gen} = 3$ V, $t_0 = t_1 \leqslant 15$ ns, $t_p = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation delay = $\dfrac{t_{PHL} + t_{PLH}}{2}$
3. Voltage values are with respect to ground terminal.

Fig. A — SWITCHING TIMES

TTL/MSI 9394/5494, 7494
4-BIT SHIFT REGISTER

DESCRIPTION – The TTL/MSI 9394/5494, 7494 is composed of four RS master/slave flip-flops, four AND-OR-INVERT gates and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the LOW state by applying a HIGH level voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the HIGH state from either of two preset input sources. Preset inputs P_{1A} through P_{1D} are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a LOW level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs P_{2A} through P_{2D} are active.

Transfer of information to the outputs occurs when the clock input goes from a LOW to a HIGH level. Since the flip-flops are RS master/slave circuits, the proper information must appear at the RS inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining RS inputs. The clear input, preset 1, and preset 2 must be at a LOW state when clocking occurs.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

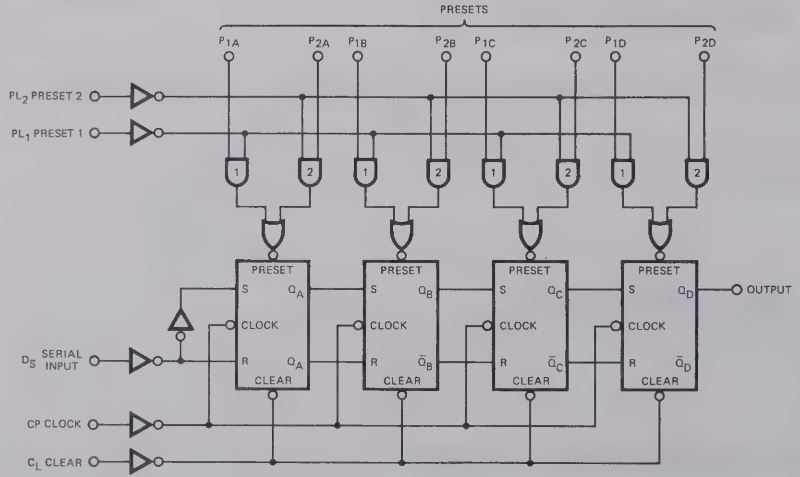
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

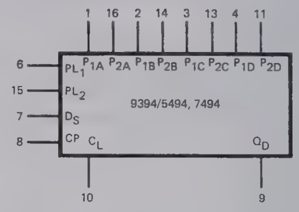
PIN NAMES		LOADING
$P_{1A} - P_{2D}$	Preset Inputs	1 U.L.
PL_1	Preset 1 Input	4 U.L.
PL_2	Preset 2 Input	4 U.L.
D_S	Serial Data Inputs	1 U.L.
CP	Clock Input	1 U.L.
C_L	Clear Input	1 U.L.
Q_D	Serial Data Output	10 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

LOGIC DIAGRAM

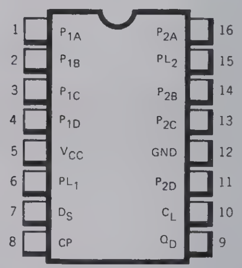

PRESETS
P1A
P2A
P1B
P2B
P1C
P2C
P1D
P2D
PL2 PRESET 2
PL1 PRESET 1
1
2
PRESET
S
QA
QB
QC
QD
CLOCK
R
CLEAR
OUTPUT
DS SERIAL INPUT
CP CLOCK
CL CLEAR

LOGIC SYMBOL

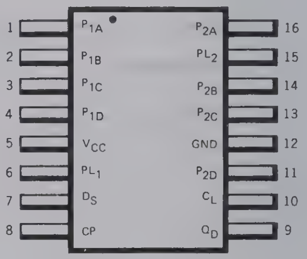

1
16
2
14
3
13
4
11
6
15
7
8
PL1
P1A
P2A
P1B
P2B
P1C
P2C
P1D
P2D
PL2
9394/5494, 7494
DS
CP
CL
QD
10
9

V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 P1A
2 P1B
3 P1C
4 P1D
5 VCC
6 PL1
7 DS
8 CP
16 P2A
15 PL2
14 P2B
13 P2C
12 GND
11 P2D
10 CL
9 QD

FLAT PAK (TOP VIEW)


1 P1A
2 P1B
3 P1C
4 P1D
5 VCC
6 PL1
7 DS
8 CP
16 P2A
15 PL2
14 P2B
13 P2C
12 GND
11 P2D
10 CL
9 QD

Positive Logic: HIGH input to clear sets Q_A, Q_B, Q_C and Q_D to LOW level.

TRUTH TABLE

CLOCK INPUT	CLEAR INPUT	COMMON PRESETS		BIT PRESETS		Q_D
		1	2	1A–1D	2A–2D	
X	H	L	L	Inhibit	Inhibit	L
X	X	H	L	Active	Inhibit	Follows 1D
X	X	L	H	Inhibit	Active	Follows 2D
Active	L	L	L	Inhibit	Inhibit	Follows Serial Input by 4 Bits

Common Presets (PL_1, PL_2) not activated (H) simultaneously X-either H or L.

States of internal Flip-Flops Q_A, Q_B, Q_C, will follow either 1A – 1C or 2A – 2C depending upon common preset condition.

Serial input is overridden except when clocking.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9394XM/5494XM			9394XC/7494XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.5	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out from Output				10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$		35			35			ns
Width of Preset Pulse, $t_{p(preset)}$		30			30			ns
Width of Clear Pulse, $t_{p(clear)}$		30			30			ns
Serial Input Setup Time,	t_{setup} (HIGH)	35			35			ns
	t_{setup} (LOW)	25			25			ns
Serial Input Hold Time, t_{hold}		0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}	
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	
I_{IH}	Input HIGH Current at Any Input Except Preset 1 and Preset 2			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset 1 and Preset 2			160	µA	V_{CC} = MAX., V_{IN} = 2.4 V	
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at Any Input Except Preset 1 and Preset 2			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
	Input LOW Current at Preset 1 and Preset 2			–6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9394/5494	V_{CC} = MAX., V_{OUT} = 0 V
		–18		–57	mA	9394/7494	
I_{CC}	Supply Current		35	50	mA	9394/5494	V_{CC} = MAX.
			35	58	mA	9394/7494	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Clock Frequency	10			MHz	
t_{PLH}	Turn Off Delay Clock to Output		25	40	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω
t_{PHL}	Turn On Delay Clock to Output		25	40	ns	
t_{PLH}	Turn Off Delay Preset to Output			35	ns	
t_{PHL}	Turn On Delay Clear to Output			40	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.

TTL/MSI 9395/5495, 7495

4-BIT RIGHT-SHIFT, LEFT-SHIFT REGISTER

DESCRIPTION – The TTL/MSI 9395/5495, 7495 Shift Register is composed of four RS master/slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate and six inverters-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logic input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

When a LOW level is applied to the mode control input, the number 1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the RS inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

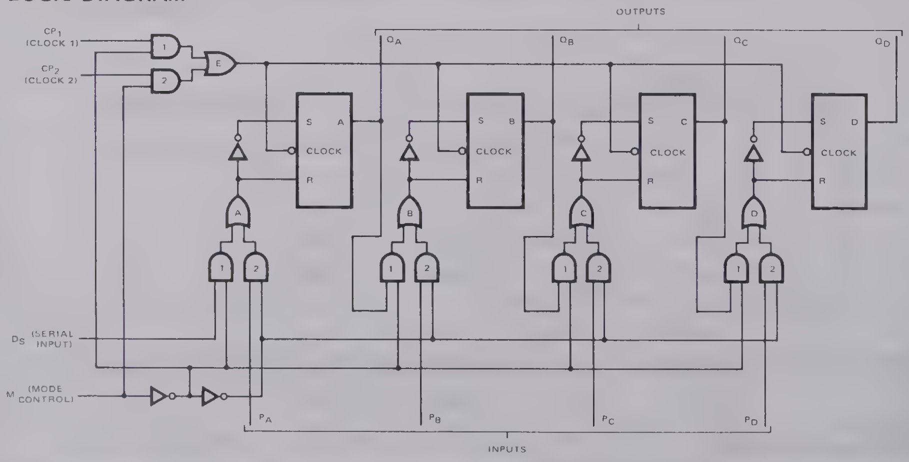
When a HIGH level is applied to the mode control input, the number 1 AND gates are inhibited (decoupling the outputs from the succeeding RS inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a HIGH to a LOW level.

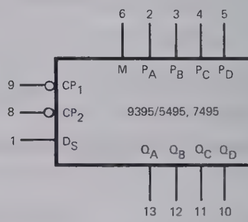
PIN NAMES		LOADING
$\overline{CP}_1$	Clock 1 Input	1 U.L.
$\overline{CP}_2$	Clock 2 Input	1 U.L.
M	Mode Control Input	2 U.L.
P_A, P_B, P_C, P_D	Parallel Data Inputs	1 U.L.
Q_A, Q_B, Q_C, Q_D	Parallel Data Outputs	10 U.L.
D_S	Serial Data Input	1 U.L.

1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW

LOGIC DIAGRAM

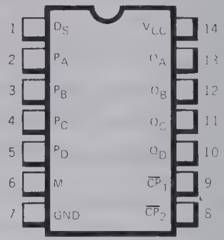

OUTPUTS
CP1 (CLOCK 1)
CP2 (CLOCK 2)
1
2
E
QA
QB
QC
QD
S A CLOCK R
S B CLOCK R
S C CLOCK R
S D CLOCK R
A
B
C
D
DS (SERIAL INPUT)
M (MODE CONTROL)
PA
PB
PC
PD
INPUTS

LOGIC SYMBOL

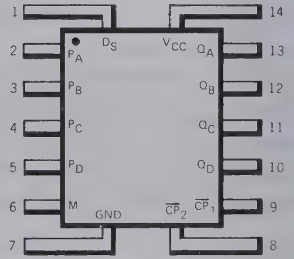

6 2 3 4 5
M PA PB PC PD
9 CP1
8 CP2
1 DS
9395/5495, 7495
QA QB QC QD
13 12 11 10

V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 DS
2 PA
3 PB
4 PC
5 PD
6 M
7 GND
14 VCC
13 QA
12 QB
11 QC
10 QD
9 CP1
8 CP2

FLATPAK(TOP VIEW)


1 DS
2 PA
3 PB
4 PC
5 PD
6 M
7 GND
14 VCC
13 QA
12 QB
11 QC
10 QD
9 CP1
8 CP2

Positive logic:
Mode control = LOW for right shift
Mode control = HIGH for left shift or parallel load

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9395XM/5495XM MIN	TYP	MAX	9395XC/7495XC MIN	TYP	MAX	UNITS
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output	HIGH Level			20			20	U.L.
	LOW Level			10			10	
Width of Clock Pulse $t_{p(clock)}$ (See Fig. A)		20	10		15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Fig. A)		10			10			ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Fig. A)		0			0			ns
LOW Level Setup Time Required at Mode Control (t_1 in Fig. B) (With Respect to Clock 1 Input)		15			15			ns
HIGH Level Setup Time Required at Mode Control (t_2 in Fig. B) (With Respect to Clock 2 Input)		15			15			ns
LOW Level Setup Time Required at Mode Control (t_3 in Fig. B) (With Respect to Clock 2 Input)		5.0			5.0			ns
HIGH Level Setup Time Required at Mode Control (t_4 in Fig. B) (With Respect to Clock 1 Input)		5.0			5.0			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 2)	MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}	1 & 3
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}	2 & 4
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = -0.8 mA	1 & 3
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	2 & 4
I_{IH}	Input HIGH Current at Any Input Except Mode Control			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	6
				1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	
	Input HIGH Current at Mode Control			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V	6
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at Any Input Except Mode Control			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	5
	Input LOW Current at Mode Control			-3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	5
I_{OS}	Output Short Circuit Current (Note 3)	-18		-57	mA	V_{CC} = MAX.	7
I_{CC}	Supply Current	39		63	mA	V_{CC} = MAX.	8

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time.

(4) Voltage values are with respect to network ground terminal.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
f_{max}	Maximum Clock Frequency	25	36		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 400\Omega$	A
t_{PLH}	Turn Off Delay Clock 1 or Clock 2 to Outputs		18	27	ns		A
t_{PHL}	Turn On Delay Clock 1 or Clock 2 to Outputs		21	32	ns		A

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

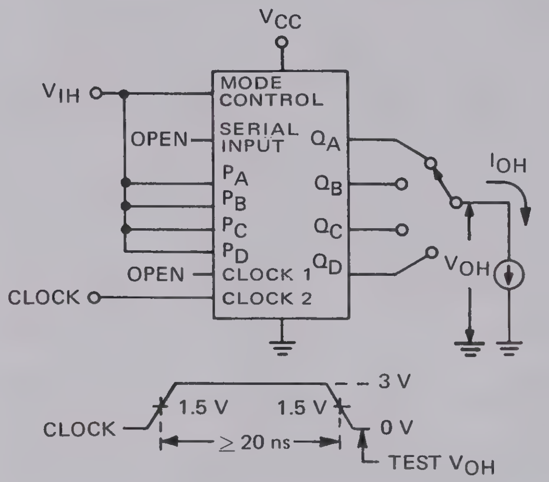

VCC
VIH
MODE CONTROL
OPEN
SERIAL INPUT
QA
PA
PB
PC
PD
QB
QC
QD
IOH
VOH
OPEN
CLOCK 1
CLOCK
CLOCK 2
3 V
1.5 V
1.5 V
0 V
≥ 20 ns
TEST VOH

Fig. 1

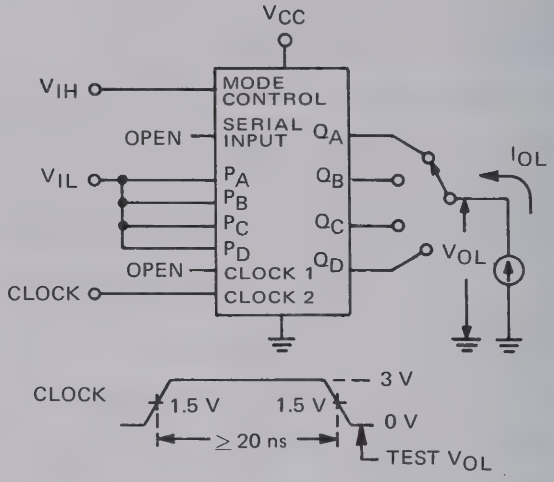

VCC
VIH
MODE CONTROL
OPEN
SERIAL INPUT
QA
VIL
PA
PB
PC
PD
QB
QC
QD
IOL
VOL
OPEN
CLOCK 1
CLOCK
CLOCK 2
3 V
1.5 V
1.5 V
0 V
≥ 20 ns
TEST VOL

Fig. 2

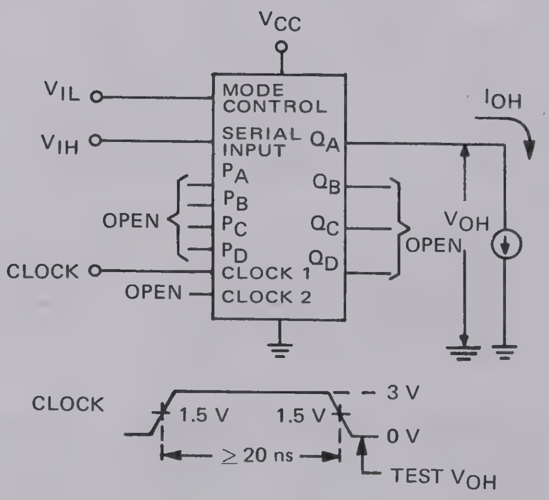

VCC
VIL
MODE CONTROL
VIH
SERIAL INPUT
QA
IOH
PA
PB
PC
PD
QB
QC
QD
OPEN
VOH
OPEN
CLOCK
CLOCK 1
OPEN
CLOCK 2
3 V
1.5 V
1.5 V
0 V
≥ 20 ns
TEST VOH

Fig. 3

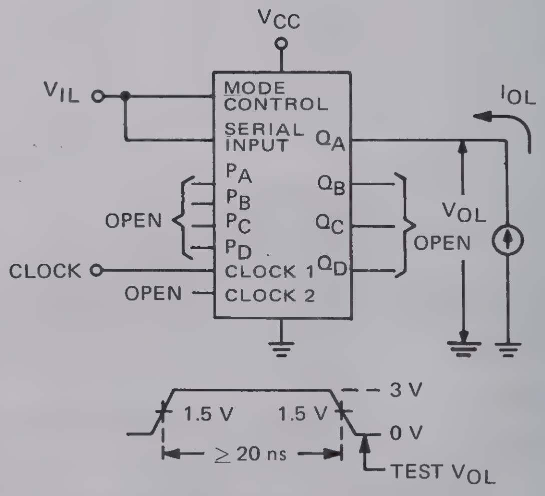
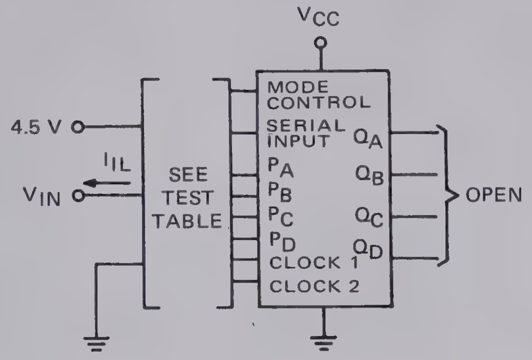

VCC
VIL
MODE CONTROL
SERIAL INPUT
QA
IOL
PA
PB
PC
PD
QB
QC
QD
OPEN
VOL
OPEN
CLOCK
CLOCK 1
OPEN
CLOCK 2
3 V
1.5 V
1.5 V
0 V
≥ 20 ns
TEST VOL

Fig. 4

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION (con't.)

DC TEST CIRCUITS*(Continued)

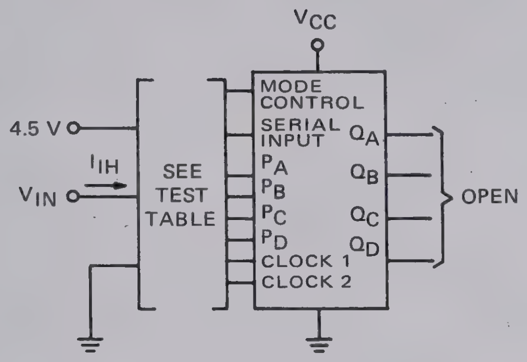

VCC
MODE CONTROL
SERIAL INPUT
PA
PB
PC
PD
CLOCK 1
CLOCK 2
QA
QB
QC
QD
OPEN
4.5 V
IIL
VIN
SEE TEST TABLE

TEST TABLE

Test	Apply 4.5 V	Apply GND
Mode Control	Clock 2	None
Serial Input	None	Mode Control
Input P_A	Mode Control	None
Input P_B	Mode Control	None
Input P_C	Mode Control	None
Input P_D	Mode Control	None
Clock 1	None	Mode Control
Clock 2	Mode Control	None

1. Each Input is tested separately.

Fig. 5


VCC
MODE CONTROL
SERIAL INPUT
PA
PB
PC
PD
CLOCK 1
CLOCK 2
QA
QB
QC
QD
OPEN
4.5 V
IIH
VIN
SEE TEST TABLE

TEST TABLE

Test	Apply 4.5 V	Apply GND
Mode Control	None	Clock 2
Serial Input	Mode Control	None
Input P_A	None	Mode Control
Input P_B	None	Mode Control
Input P_C	None	Mode Control
Input P_D	None	Mode Control
Clock 1	Mode Control	None
Clock 2	None	Mode Control

Fig. 6

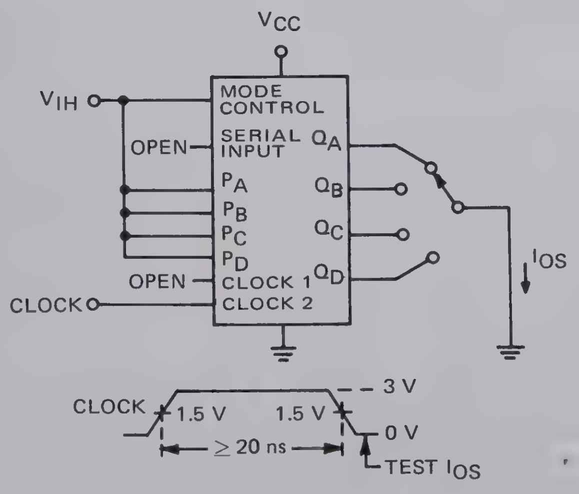

VCC
VIH
OPEN
MODE CONTROL
SERIAL INPUT
PA
PB
PC
PD
CLOCK 1
CLOCK 2
QA
QB
QC
QD
IOS
OPEN
CLOCK
CLOCK
1.5 V
1.5 V
3 V
0 V
≥ 20 ns
TEST IOS

Fig. 7

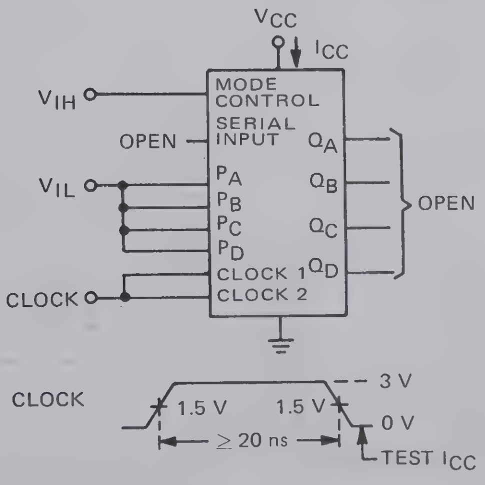
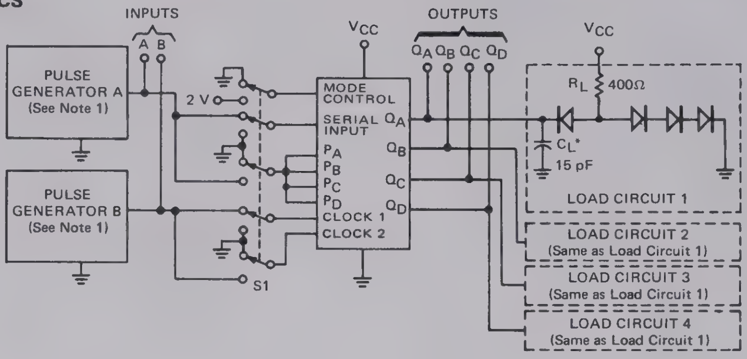

VCC
ICC
VIH
OPEN
VIL
CLOCK
MODE CONTROL
SERIAL INPUT
PA
PB
PC
PD
CLOCK 1
CLOCK 2
QA
QB
QC
QD
OPEN
CLOCK
1.5 V
1.5 V
3 V
0 V
≥ 20 ns
TEST ICC

Fig. 8

*Arrows indicate actual direction of current flow.

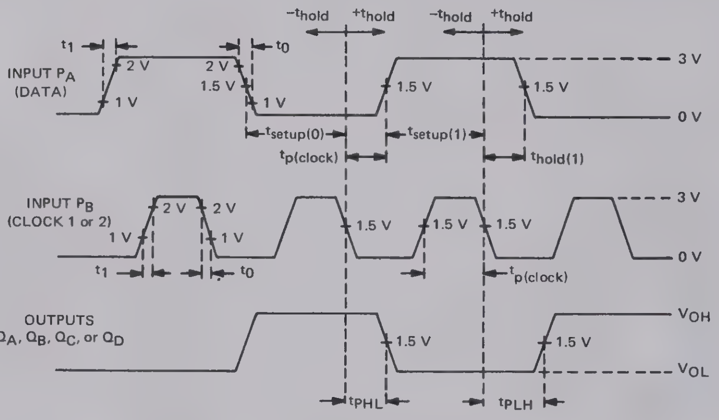
PARAMETER MEASUREMENT INFORMATION (con't.)

SWITCHING CHARACTERISTICS


INPUTS
A B
PULSE GENERATOR A (See Note 1)
PULSE GENERATOR B (See Note 1)
2 V
S1
VCC
MODE CONTROL
SERIAL INPUT
PA
PB
PC
PD
CLOCK 1
CLOCK 2
QA
QB
QC
QD
OUTPUTS
QA QB QC QD
VCC
RL 400Ω
CL* 15 pF
LOAD CIRCUIT 1
LOAD CIRCUIT 2 (Same as Load Circuit 1)
LOAD CIRCUIT 3 (Same as Load Circuit 1)
LOAD CIRCUIT 4 (Same as Load Circuit 1)

*C_L includes probe and jig capacitance.

TEST CIRCUIT

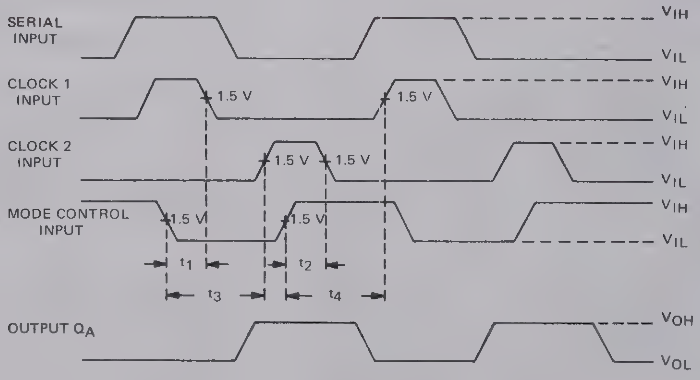

$-t_{hold}$
$+t_{hold}$
t_1
t_0
INPUT PA (DATA)
2 V
1.5 V
1 V
3 V
0 V
$t_{setup(0)}$
$t_{setup(1)}$
$t_{p(clock)}$
$t_{hold(1)}$
INPUT PB (CLOCK 1 or 2)
OUTPUTS QA, QB, QC, or QD
VOH
VOL
t_{PHL}
t_{PLH}

VOLTAGE WAVEFORMS

NOTES:

1. The pulse generators having the following characteristics: $V_{gen} = 3$ V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \approx 50\Omega$. For pulse generator A: $t_p \geq 20$ ns and PRR = 500 kHz. For pulse generator B: $t_p \geq 15$ ns and PRR = 1 MHz. When testing f_{max} vary PRR.
2. Voltage values are with respect to network ground terminal.

Fig. A SWITCHING TIMES


SERIAL INPUT
CLOCK 1 INPUT
CLOCK 2 INPUT
MODE CONTROL INPUT
OUTPUT QA
1.5 V
VIH
VIL
VOH
VOL
t_1
t_2
t_3
t_4

Note: Input P_A is at V_{IL}.

Fig. B RECOMMENDED MODE CONTROL SETUP TIMES

TTL/MSI 9396/5496, 7496

5–BIT SHIFT REGISTER

DESCRIPTION – The TTL/MSI 9396/5496, 7496 5-Bit Shift Register consists of five RS master/slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the LOW state by applying a low level voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the HIGH state by applying a high level voltage to both the preset input of the specific flip-flop and the common preset input. The parallel enable input is provided to allow setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a LOW level to a HIGH level. Since the flip-flops are RS master/slave circuits, the proper information must appear at the RS inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining RS inputs. The clear input must be at a HIGH level and the preset input must be at a LOW level when clocking occurs.

PIN NAMES		**LOADING**
PL	Parallel Load Input	5 U.L.
P_A, P_B, P_C, P_D, P_E	Parallel Data Inputs	1 U.L.
D_S	Serial Data Input	1 U.L.
CP	Clock Input	1 U.L.
$\overline{C}_L$	Clear Input	1 U.L.
Q_A, Q_B, Q_C, Q_D, Q_E	Parallel Data Outputs	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

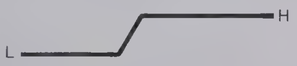
TRUTH TABLE

PRESET COMMON	PRESET BIT	$\overline{\text{CLEAR}}$	SERIAL INPUT	CLOCK	OUTPUT	
L	X	L	X	X	L	Clear all output to logical "L".
H	H	H	X	X	H	Preset outputs to 1 input
H	L	H	X	X	L	bit configuration.
L	X	H	H	enable	H	Serial input shift right.
L	X	H	L	enable	L	Serial-to-parallel conversion.

NOTES:

(a) After loading data, set clear to "H" and preset to "L" clock to give parallel to serial conversion.

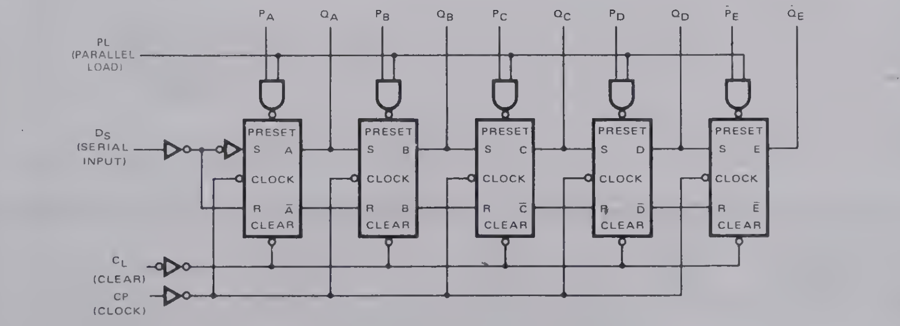
(b) Information transferred on rising edge of clock pulse.



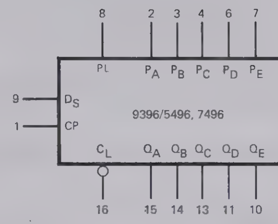
(c) Do not enable preset and clear simultaneously.
Preset – "H" Clear – "L" = undefined output. Dependent upon which enable is removed first.

(d) X Either logical "L" or logical "H".

LOGIC DIAGRAM

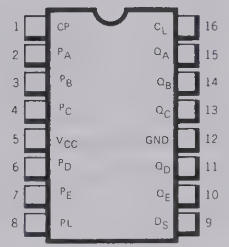

PA
QA
PB
QB
PC
QC
PD
QD
PE
QE
PL (PARALLEL LOAD)
DS (SERIAL INPUT)
PRESET
S
A
B
C
D
E
CLOCK
R
CLEAR
CL (CLEAR)
CP (CLOCK)

LOGIC SYMBOL

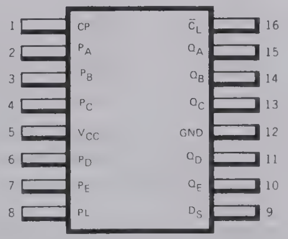

8
2
3
4
6
7
PL
PA
PB
PC
PD
PE
9
DS
1
CP
9396/5496, 7496
CL
QA
QB
QC
QD
QE
16
15
14
13
11
10

V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)


1
CP
2
PA
3
PB
4
PC
5
VCC
6
PD
7
PE
8
PL
16
CL
15
QA
14
QB
13
QC
12
GND
11
QD
10
QE
9
DS

FLATPAK (TOP VIEW)


1
CP
2
PA
3
PB
4
PC
5
VCC
6
PD
7
PE
8
PL
16
CL
15
QA
14
QB
13
QC
12
GND
11
QD
10
QE
9
DS

Positive Logic: LOW input at clear sets all outputs to LOW level.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9396XM/5496XM			9396XC/7496XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Width of Clock Pulse, $t_{p(clock)}$	35			35			ns
Width of Preset Pulse, $t_{p(preset)}$	30			30			ns
Width of Clear Pulse, $t_{p(clear)}$	30			30			ns
Serial Input Setup Time, t_{setup}	30			30			ns
Serial Input Hold Time, t_{hold}	0			0			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}	
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., $I_{OH} = -0.4$ mA	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., $I_{OL} = 16$ mA	
I_{IH}	Input HIGH Current at Any Input Except Parallel Load			40	µA	V_{CC} = MAX., $V_{IN} = 2.4$ V	
				1.0	mA	V_{CC} = MAX., $V_{IN} = 5.5$ V	
	Input HIGH Current at Parallel Load			200	µA	V_{CC} = MAX., $V_{IN} = 2.4$ V	
				1.0	mA	V_{CC} = MAX., $V_{IN} = 5.5$ V	
I_{IL}	Input LOW Current at Any Input Except Parallel Load			−1.6	mA	V_{CC} = MAX., $V_{IN} = 0.4$ V	
	Input LOW Current at Parallel Load			−8.0	mA	V_{CC} = MAX., $V_{IN} = 0.4$ V	
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9396/5496	V_{CC} = MAX. $V_{OUT} = 0$ V
		−18		−57	mA	9396/7496	
I_{CC}	Supply Current		48	68	mA	9396/5496	V_{CC} = MAX.
			48	79	mA	9396/7496	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Clock Frequency	10			MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 400\Omega$
t_{PLH}	Turn Off Delay Clock to Output		25	40	ns	
t_{PHL}	Turn On Delay Clock to Output		25	40	ns	
t_{PLH}	Turn Off Delay Preset or Parallel Load to Output		28	35	ns	
t_{PHL}	Turn On Delay Clear to Output			55	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at $V_{CC} = 5.0$ V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) This voltage value is with respect to network ground terminal.

TTL/MSI 93141/74141

1-OF-10 DECODER/DRIVER (NIXIE)

TO BE ANNOUNCED

DESCRIPTION — The 93141/74141 is a BCD-to-Decimal Decoder Driver that is designed to take a 4-bit BCD code input and drive cold-cathode indicator tubes. This decoder utilizes design improvements that minimize switching transients in order to maintain a stable display.

The segments and numeric designations chosen to represent the decimal numbers are shown below. For binary inputs 10 through 15, the outputs are off. These invalid codes can be used in blanking leading or trailing-edge zeros in a display.

The ten high performance, NPN output transistors have a maximum reverse current of 50μA at 55V. Typical power dissipation is 55 mW.

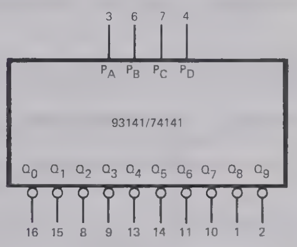
PIN NAMES		LOADING
P_A	Address Input	1 U.L.
P_B, P_C, P_D	Address Input	2 U.L.
$\overline{Q}_0$ to $\overline{Q}_9$	Outputs	*

*See output characteristics.

Max. Current Into Output During "ON" state	7 mA
Output Leakage at 55 V	50 μA

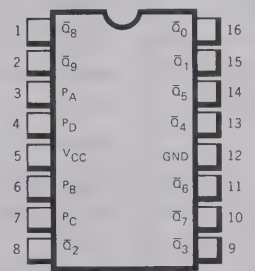
1 U.L. = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL


3 6 7 4
P_A P_B P_C P_D
93141/74141
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
16 15 8 9 13 14 11 10 1 2

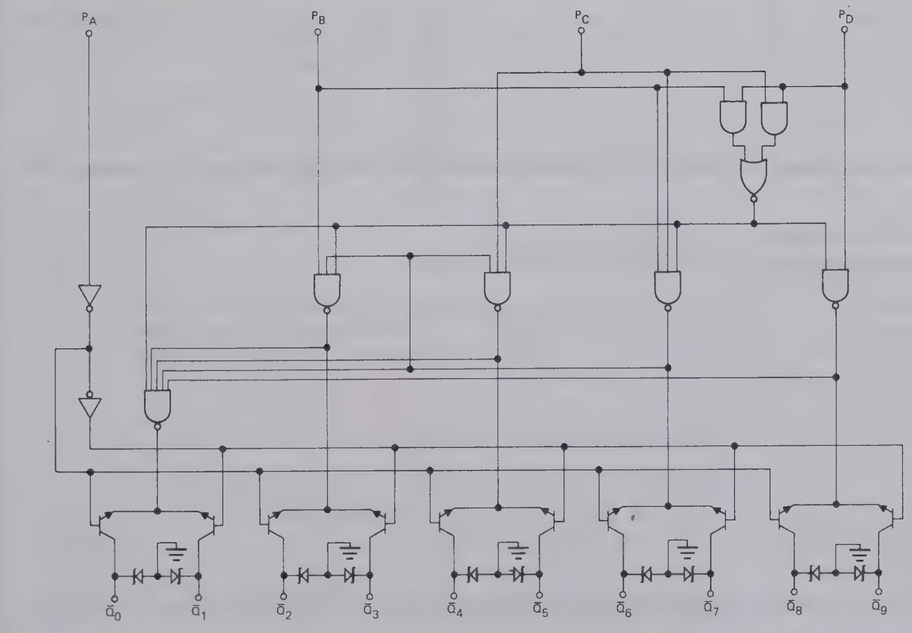
V_{CC} = PIN 5
GND = PIN 12

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 $\overline{Q}_8$
2 $\overline{Q}_9$
3 P_A
4 P_D
5 V_{CC}
6 P_B
7 P_C
8 $\overline{Q}_2$
16 $\overline{Q}_0$
15 $\overline{Q}_1$
14 $\overline{Q}_5$
13 $\overline{Q}_4$
12 GND
11 $\overline{Q}_6$
10 $\overline{Q}_7$
9 $\overline{Q}_3$

Positive Logic: See Truth Table

LOGIC DIAGRAM


P_A
P_B
P_C
P_D
$\overline{Q}_0$
$\overline{Q}_1$
$\overline{Q}_2$
$\overline{Q}_3$
$\overline{Q}_4$
$\overline{Q}_5$
$\overline{Q}_6$
$\overline{Q}_7$
$\overline{Q}_8$
$\overline{Q}_9$

TRUTH TABLE

INPUT				OUTPUT
P_D	P_C	P_B	P_A	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = HIGH level,
L = LOW level.
†All other outputs are off

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	0°C to 70°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	93141XC/74141XC			UNITS
	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 3)	4.75	5.0	5.75	Volts
Operating Free Air Temperature Range	0	25	70	°C
Output Voltage (See Notes 3 & 4)			65	V

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	1 & 2
V_{OL}	Output LOW Voltage			2.5	Volts	V_{CC} = MIN., I_{OL} = 7.0 mA	1
V_{OH}	Output HIGH Voltage for input counts 0 thru 9	60			Volts	V_{CC} = MAX., I_{OH} = 0.5 mA	2
I_{OH}	Output HIGH Current			50	µA	V_{CC} = MAX., V_{OUT} = 55 V	2
	Output HIGH Current for input counts 10 thru 15			5.0	µA	V_{CC} = MAX., V_{OUT} = 30 V	2
I_{IH}	Input HIGH Current at P_A			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at P_B, P_C, or P_D			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current Into P_A			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	4
	Input LOW Current Into P_B, P_C, or P_D			-3.2	mA		
I_{CC}	Supply Current		16	25	mA	V_{CC} = MAX.	3

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

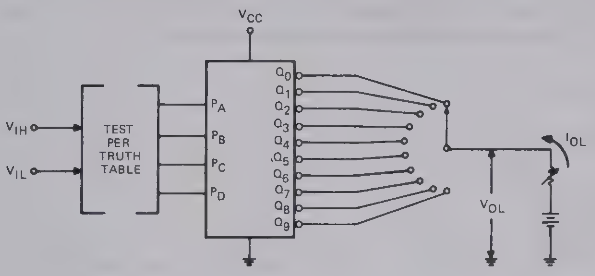
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Voltage values are with respect to network ground terminal.

(4) This is the maximum voltage which should be applied to any output when it is in the off state.

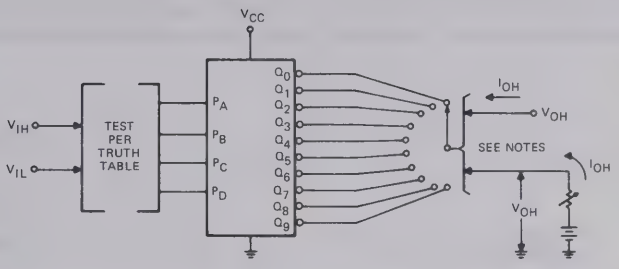
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*


VCC
VIH
VIL
TEST PER TRUTH TABLE
PA
PB
PC
PD
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
VOL
IOL

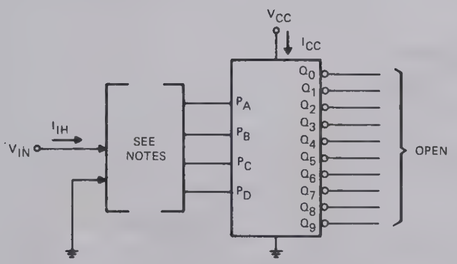
Each output is tested separately.

Fig. 1 V_{IH}, V_{IL}, V_{OL}


VCC
VIH
VIL
TEST PER TRUTH TABLE
PA
PB
PC
PD
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
IOH
VOH
SEE NOTES
IOH
VOH

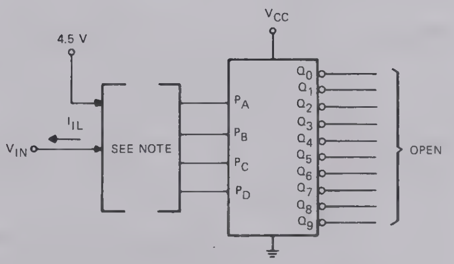
1. Each output is tested separately.
2. V_{OH} is tested at I_{OH} = 0.5 mA and I_{OH} is tested at V_{OH} = 55 V for all inputs counts. I_{OH} is tested also at V_{OH} = 30 V for input counts 10 through 15.

Fig. 2 V_{IH}, V_{IL}, I_{OH}, V_{OH}


VCC
ICC
IIH
VIN
SEE NOTES
PA
PB
PC
PD
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
OPEN

1. When testing I_{IH}, each input is tested separately with all other inputs grounded.
2. When testing I_{CC}, all inputs are grounded.

Fig. 3 I_{IH}, I_{CC}


VCC
4.5 V
IIL
VIN
SEE NOTE
PA
PB
PC
PD
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
OPEN

Each input is tested separately, with all other inputs at 4.5 V.

Fig. 4 I_{IL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

APPLICATIONS

GENERAL — When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.

DRIVING INDICATOR TUBES — As shown in Figure 5, the 93141/74141 requires no external components for driving cold-cathode indicator tubes. The versatility here is limited only by the system capability to control the data inputs.

A suggested method for blanking extraneous zeros is shown in Figure 6. Any input count above decimal 9 may be used for blanking. In the following application decimal 12 is used. When the most significant bit (MSB) or the least significant bit (LSB) is decimal 0(0000), that indicator is blanked while decimal 12 (binary 1100) is applied to the 93141/74141 inputs causing all the outputs to be off. If the MSB or LSB is decimal 0 and being blanked, this signal is gated with and blanks the next smaller digit. This scheme is easily expandable to n digits.

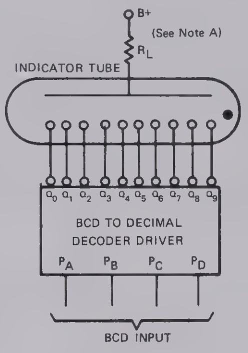
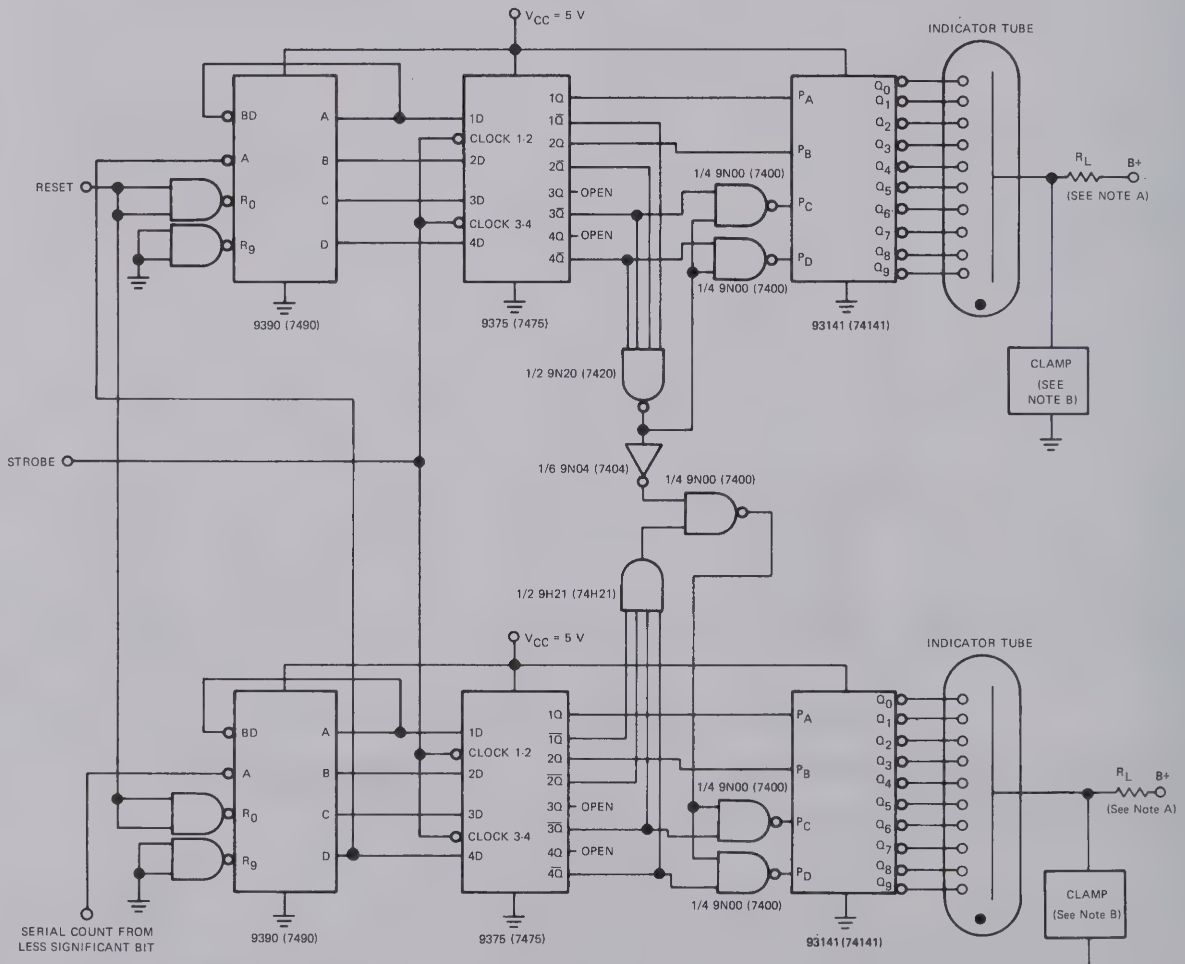

B+
(See Note A)
R_L
INDICATOR TUBE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
BCD TO DECIMAL
DECODER DRIVER
PA PB PC PD
BCD INPUT

Fig. 5


VCC = 5 V
INDICATOR TUBE
BD
A
R0
R9
B
C
D
RESET
1D
CLOCK 1·2
2D
3D
CLOCK 3·4
4D
1Q
1Q̄
2Q
2Q̄
3Q
3Q̄
4Q
4Q̄
OPEN
OPEN
PA
PB
PC
PD
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
R_L
B+
(SEE NOTE A)
1/4 9N00 (7400)
1/4 9N00 (7400)
9390 (7490)
9375 (7475)
93141 (74141)
CLAMP (SEE NOTE B)
1/2 9N20 (7420)
STROBE
1/6 9N04 (7404)
1/4 9N00 (7400)
1/2 9H21 (74H21)
VCC = 5 V
INDICATOR TUBE
1/4 9N00 (7400)
1/4 9N00 (7400)
R_L B+
(See Note A)
CLAMP (See Note B)
SERIAL COUNT FROM LESS SIGNIFICANT BIT
9390 (7490)
9375 (7475)
93141 (74141)

NOTES:

A. Values for B+ and R_L are as specified by the tube manufacturer.

B. Blanking is assured only if the anode of the indicator tube is clamped at 150 volts maximum.

Fig. 6

TTL/MSI 93150/54150, 74150
93151/54151, 74151 • 93152/54152, 74152
16-INPUT AND 8-INPUT MULTIPLEXER

DESCRIPTION – The 93150/54150, 74150 is a 16-Input Multiplexer which features active LOW strobe and internal select decoding. A HIGH at the strobe input forces the output HIGH regardless of input conditions.

The 93151/54151, 74151 is an 8-Input Multiplexer with active LOW strobe, internal select decoding and complementary outputs.

The 93152/54152, 74152 is an 8-Input Multiplexer with internal select decoding and a single inverted output.

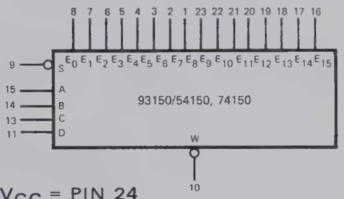
In each of the multiplexers data is routed from a particular input to the output according to the binary code applied to the select inputs.

Typical power dissipations are: 93150/54150, 74150 — 200 mW; 93151/54151, 74151 — 145 mW; 93152/54152, 74152 — 130 mW.

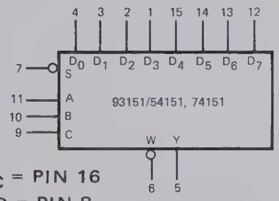
PIN NAMES		LOADING
E_0 to E_{15}	Data Inputs	1 U.L.
D_0 to D_7	Data inputs	1 U.L.
$\overline{S}$	Strobe (Enable) Input	1 U.L.
A, B, C, D	Data Select Inputs	1 U.L.
$\overline{W}$	Data Output	10 U.L.
Y	Data Output	10 U.L.

NOTE: 1 U.L. = 40 µA HIGH/1.6 mA LOW.

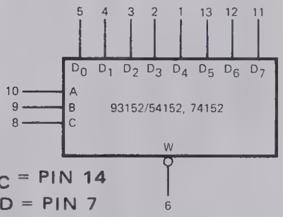
LOGIC SYMBOLS


8 7 6 5 4 3 2 1 23 22 21 20 19 18 17 16
S E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15
9
15 A
14 B
13 C
11 D
93150/54150, 74150
W
10

V_{CC} = PIN 24
GND = PIN 12

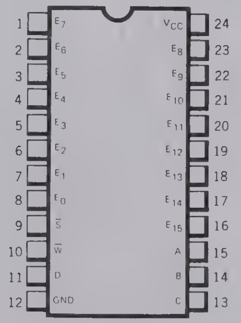

4 3 2 1 15 14 13 12
S D0 D1 D2 D3 D4 D5 D6 D7
7
11 A
10 B
9 C
93151/54151, 74151
W Y
6 5

V_{CC} = PIN 16
GND = PIN 8

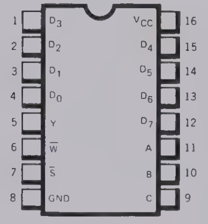

5 4 3 2 1 13 12 11
D0 D1 D2 D3 D4 D5 D6 D7
10 A
9 B
8 C
93152/54152, 74152
W
6

V_{CC} = PIN 14
GND = PIN 7

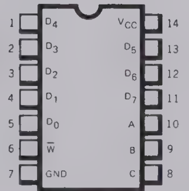
CONNECTION DIAGRAMS
DIP (TOP VIEWS)*


1 E7
2 E6
3 E5
4 E4
5 E3
6 E2
7 E1
8 E0
9 S
10 W
11 D
12 GND
24 VCC
23 E8
22 E9
21 E10
20 E11
19 E12
18 E13
17 E14
16 E15
15 A
14 B
13 C

93150/54150, 74150


1 D3
2 D2
3 D1
4 D0
5 Y
6 W
7 S
8 GND
16 VCC
15 D4
14 D5
13 D6
12 D7
11 A
10 B
9 C

93151/54151, 74151

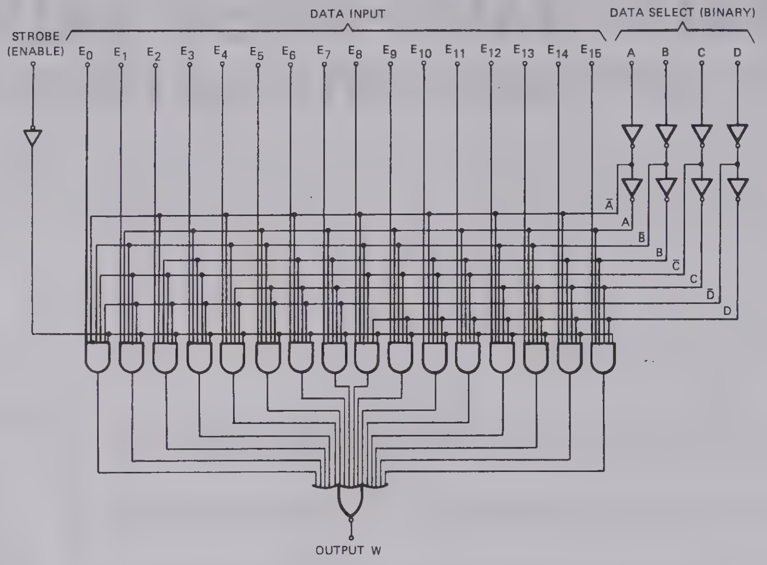

1 D4
2 D3
3 D2
4 D1
5 D0
6 W
7 GND
14 VCC
13 D5
12 D6
11 D7
10 A
9 B
8 C

93152/54152, 74152

*Pin assignments for these circuits are the same for all packages.

LOGIC DIAGRAMS

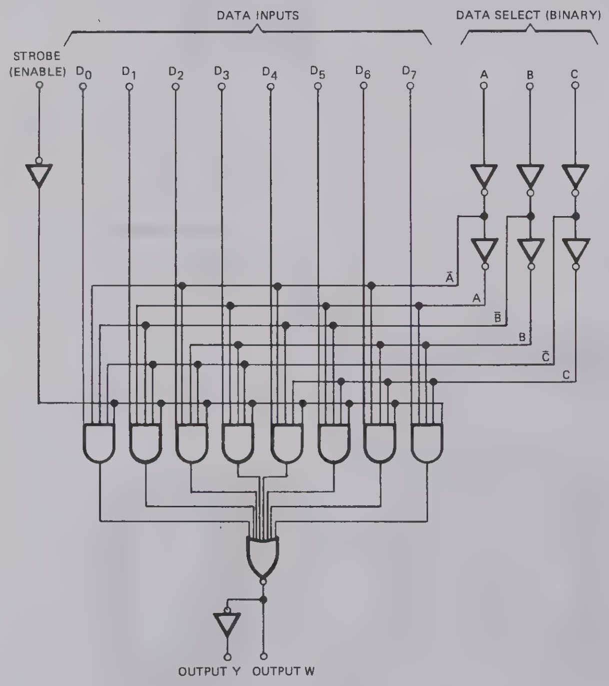
93150/54150, 74150


DATA INPUT
DATA SELECT (BINARY)
STROBE (ENABLE)
E0
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
A
B
C
D
Ā
A
B̄
B
C̄
C
D̄
D
OUTPUT W

Positive Logic

$$W = S(\bar{A}\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7$$
$$+ \bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

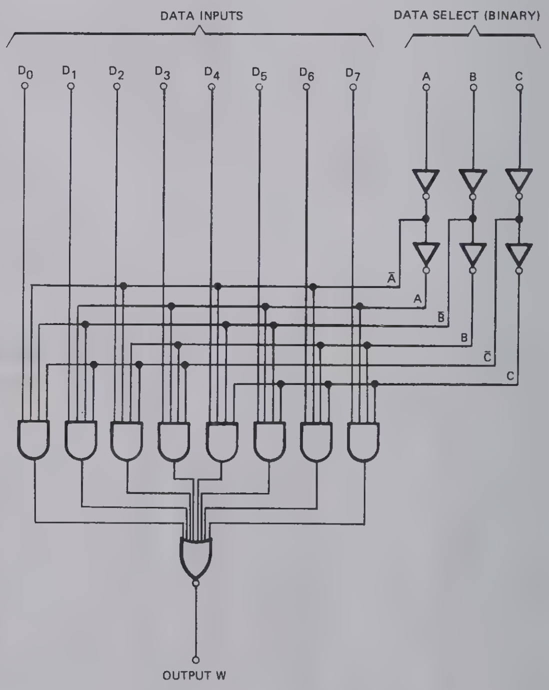
93151/54151, 74151


DATA INPUTS
DATA SELECT (BINARY)
STROBE (ENABLE)
D0
D1
D2
D3
D4
D5
D6
D7
A
B
C
Ā
A
B̄
B
C̄
C
OUTPUT Y
OUTPUT W

Positive Logic

$$Y = \bar{S}(\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + \bar{A}B\bar{C}D_2 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4$$
$$+ A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7) \quad W = \bar{Y}$$

93152/54152, 74152


DATA INPUTS
DATA SELECT (BINARY)
D0
D1
D2
D3
D4
D5
D6
D7
A
B
C
Ā
A
B̄
B
C̄
C
OUTPUT W

Positive Logic

$$W = (\bar{A}B\bar{C}D_0 + A\bar{B}\bar{C}D_1 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5$$
$$+ \bar{A}BCD_6 + ABCD_7)$$

TRUTH TABLES

93150/54150, 74150

INPUTS																					OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L

When used to indicate an input condition, X = LOGICAL H or LOGICAL L.

93151/54151, 74151 AND 93152/54152, 74152

INPUTS											OUTPUTS	
C	B	A	STROBE(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	H	X	X	X	X	X	X	X	X	L	H
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L

NOTES:
1. 54151, 74151 only.
2. When used to indicate an input, X = irrelevant.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93150XM/54150XM 93151XM/54151XM 93152XM/54152XM			93150XC/74150XC 93151XC/74151XC 93152XC/74152XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	LOW Level			10			10	U.L.
	HIGH Level			20			20	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage	2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	1 & 2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	1 & 2
I_{IH}	Input HIGH Current (Each Input)			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current (Each Input)			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	3
I_{OS}	Output Short Circuit Current (Note 3)	-20		-55	mA	93150/54150, 93151/54151, 93152/54152, V_{CC}=MAX.,V_{out}=0V	4
		-18		-55	mA	93150/74150, 93151/74151, 93152/74152, V_{CC}=MAX.,V_{out}=0V	
I_{CC}	Supply Current		40	68	mA	93150/54150, 74150 V_{CC} = MAX. V_{IN} = 4.5 V	5
			29	48	mA	93151/54151, 74151	
			26	43	mA	93152/54152, 74152	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PHL} t_{PLH}	A, B, or C Input to Y Output, 4 Levels		20 35	30 52	ns ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400 Ω	A
t_{PHL} t_{PLH}	A, B, C, or D Input to W Output, 3 Levels		22 22	33 35	ns ns		
t_{PHL} t_{PLH}	Strobe Input to Y Output		19 35	30 52	ns ns		
t_{PHL} t_{PLH}	Strobe Input to W Output		21 15.5	30 24	ns ns		
t_{PHL} t_{PLH}	D_0 thru D_7 Input to Y Output		16 19	24 29	ns ns		
t_{PHL} t_{PLH}	E_0 thru E_{15}, D_0 thru D_7 Input to W Output		8.5 13	14 20	ns ns		

NOTES:

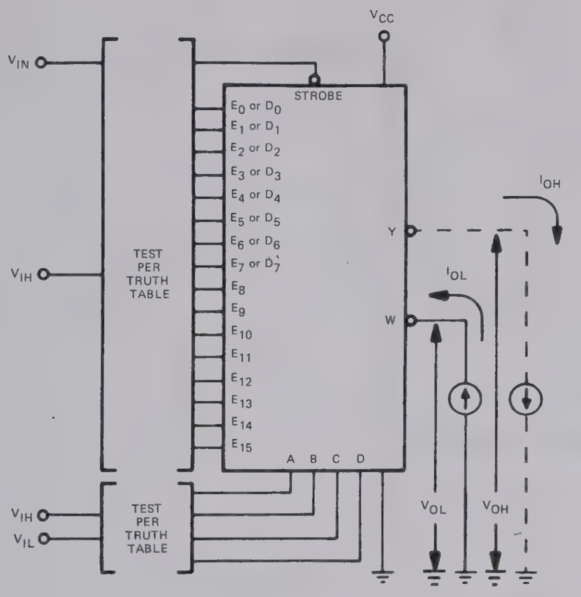
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommmended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output of the 93151/54151, 74151 should be shorted at a time.

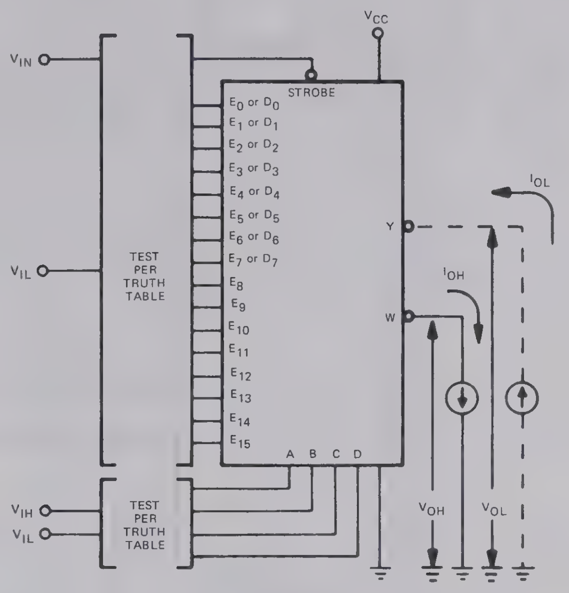
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*


V_{CC}
V_{IN}
V_{IH}
V_{IH}
V_{IL}
TEST PER TRUTH TABLE
TEST PER TRUTH TABLE
STROBE
E_0 or D_0
E_1 or D_1
E_2 or D_2
E_3 or D_3
E_4 or D_4
E_5 or D_5
E_6 or D_6
E_7 or D_7
E_8
E_9
E_{10}
E_{11}
E_{12}
E_{13}
E_{14}
E_{15}
A B C D
Y
W
I_{OH}
I_{OL}
V_{OL}
V_{OH}

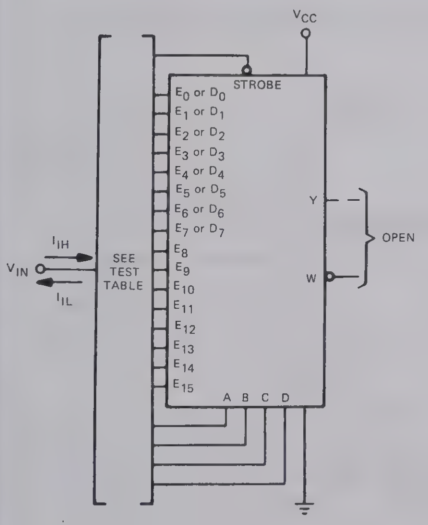
1. V_{IL} is applied to STROBE; 8-4-2-1 code is applied to A, B, C, D; and input/output condition is tested for each step of the code.
2. V_{IH} is applied to STROBE at which time V_{OL} is measured at Y and V_{OH} is measured at W.

Fig. 1


V_{CC}
V_{IN}
V_{IL}
V_{IH}
V_{IL}
TEST PER TRUTH TABLE
TEST PER TRUTH TABLE
STROBE
E_0 or D_0
E_1 or D_1
E_2 or D_2
E_3 or D_3
E_4 or D_4
E_5 or D_5
E_6 or D_6
E_7 or D_7
E_8
E_9
E_{10}
E_{11}
E_{12}
E_{13}
E_{14}
E_{15}
A B C D
Y
W
I_{OL}
I_{OH}
V_{OH}
V_{OL}

1. V_{IL} is applied to STROBE; 8-4-2-1 is applied to A, B, C, D; and input/output condition is tested for each step of the code.

Fig. 2


V_{CC}
V_{IN}
I_{IH}
I_{IL}
SEE TEST TABLE
STROBE
E_0 or D_0
E_1 or D_1
E_2 or D_2
E_3 or D_3
E_4 or D_4
E_5 or D_5
E_6 or D_6
E_7 or D_7
E_8
E_9
E_{10}
E_{11}
E_{12}
E_{13}
E_{14}
E_{15}
A B C D
Y
W
OPEN

INPUT CONDITIONS				TEST	
A	B	C	D	I_{IL}	I_{IH}
L	L	L	L	E_0 or D_0	E_{15} or D_7
H	L	L	L	E_1 or D_1	E_{14} or D_6
L	H	L	L	E_2 or D_2	E_{13} or D_5
H	H	L	L	E_3 or D_3	E_{12} or D_4
L	L	H	L	E_4 or D_4	E_{11} or D_3
H	L	H	L	E_5 or D_5	E_{10} or D_2
L	H	H	L	E_6 or D_6	E_9 or D_1
H	H	H	L	E_7 or D_7	E_8 or D_0
L	L	L	H	E_8	E_7
H	L	L	H	E_9	E_6
L	H	L	H	E_{10}	E_5
H	H	L	H	E_{11}	E_4

INPUT CONDITIONS				TEST	
A	B	C	D	I_{IL}	I_{IH}
L	L	H	H	E_{12}	E_3
H	L	H	H	E_{13}	E_2
L	H	H	H	E_{14}	E_1
H	H	H	H	E_{15}	E_0
L				A	
	L			B	
		L		C	
			L	D	
H					A
	H				B
		H			C
			H		D

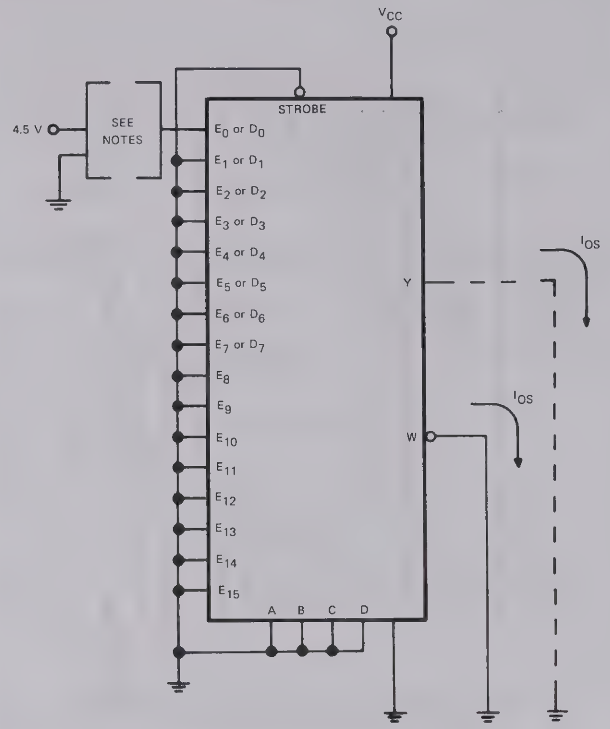
1. When testing strobe input, all other inputs are open.

Fig. 3

*Arrows indicate actual direction of current flow. Tests as shown, are for the 93150/54150, 74150. Identical tests as applicable are performed for the 93151/54151, 74151 and 93152/54152, 74152.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)


V_{CC}
4.5 V
SEE NOTES
STROBE
E_0 or D_0
E_1 or D_1
E_2 or D_2
E_3 or D_3
E_4 or D_4
E_5 or D_5
E_6 or D_6
E_7 or D_7
E_8
E_9
E_{10}
E_{11}
E_{12}
E_{13}
E_{14}
E_{15}
A
B
C
D
Y
W
I_{OS}
I_{OS}

1. When testing W output, apply GND to D_0 and E_0 input.
2. When testing Y output of 93151/54151, 74151 apply 4.5 V to D_0 and measure I_{OS}.

Fig. 4

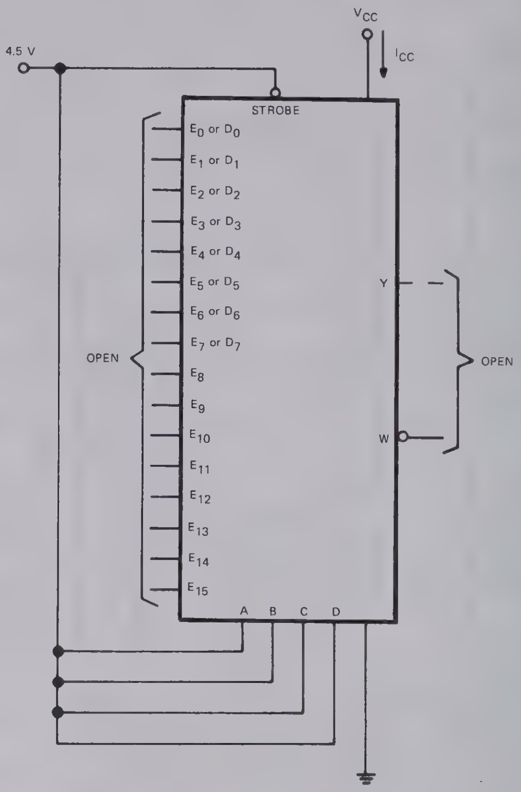
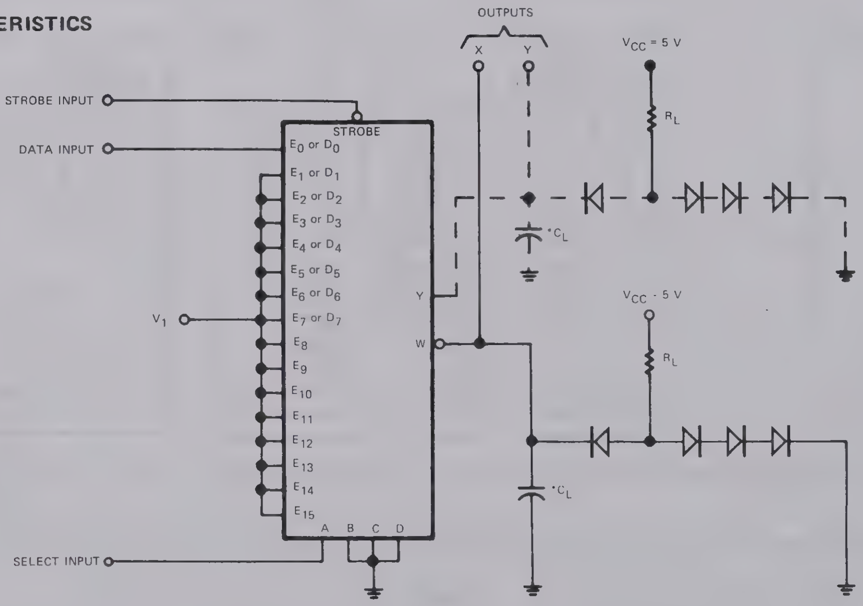

V_{CC}
I_{CC}
4.5 V
STROBE
E_0 or D_0
E_1 or D_1
E_2 or D_2
E_3 or D_3
E_4 or D_4
E_5 or D_5
E_6 or D_6
E_7 or D_7
E_8
E_9
E_{10}
E_{11}
E_{12}
E_{13}
E_{14}
E_{15}
OPEN
Y
W
OPEN
A
B
C
D

Fig. 5

*Arrows indicate actual direction of current flow. Tests as shown, are for the 93150/54150, 74150. Identical tests as applicable are performed for the 93151/54151, 74151 and 93152/54152, 74152.

SWITCHING CHARACTERISTICS

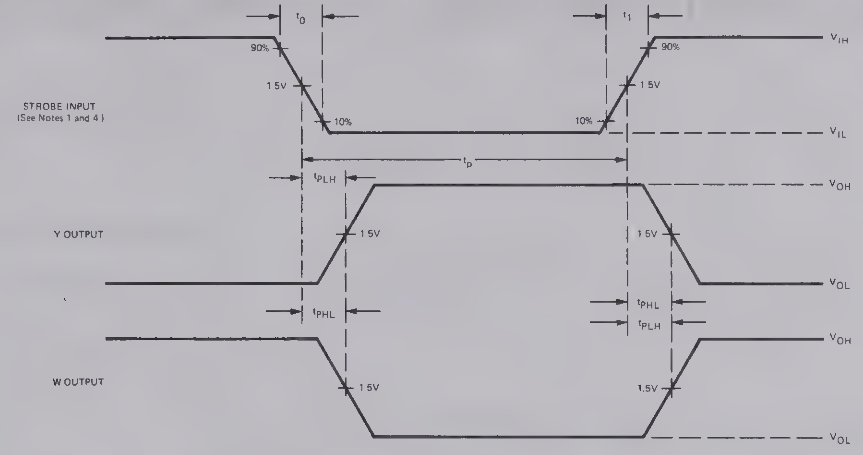

OUTPUTS
X
Y
V_{CC} = 5 V
R_L
STROBE INPUT
DATA INPUT
STROBE
E_0 or D_0
E_1 or D_1
E_2 or D_2
E_3 or D_3
E_4 or D_4
E_5 or D_5
E_6 or D_6
E_7 or D_7
E_8
E_9
E_{10}
E_{11}
E_{12}
E_{13}
E_{14}
E_{15}
V_1
Y
W
*C_L
V_{CC} - 5 V
R_L
*C_L
A
B
C
D
SELECT INPUT

*C_L Includes probe and jig capacitance.

Fig. A SWITCHING TIMES

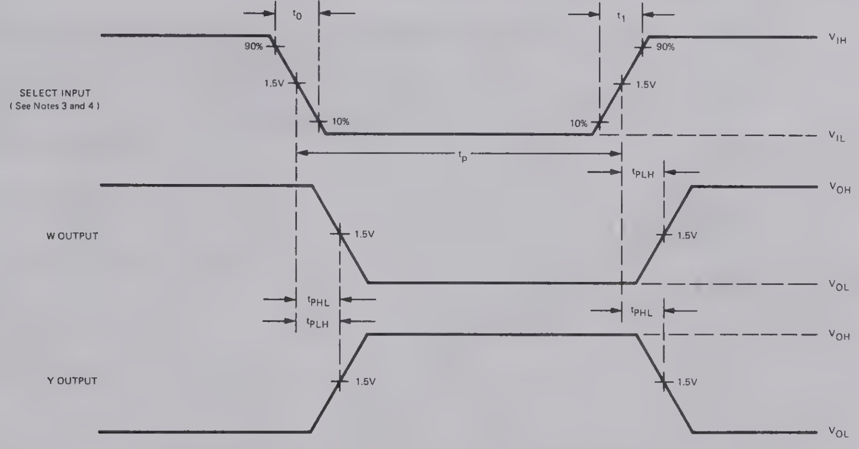
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (cont'd)



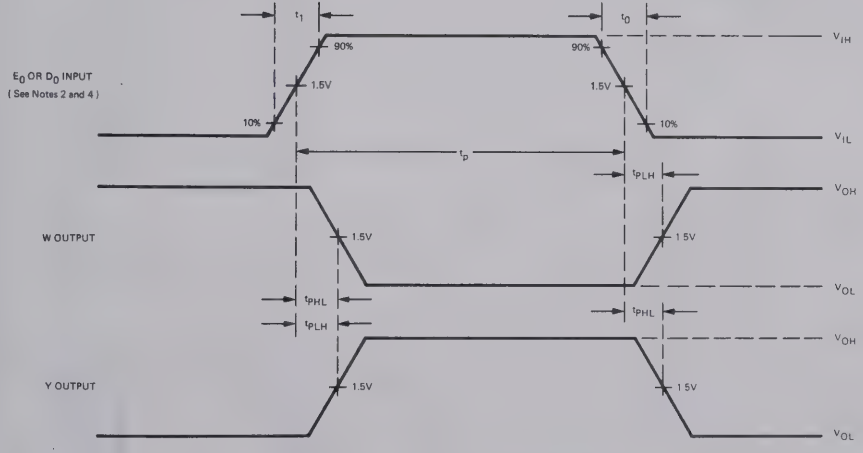
t_0
t_1
90%
1.5V
10%
V_{IH}
V_{IL}
STROBE INPUT (See Notes 1 and 4)
t_p
t_{PLH}
t_{PHL}
V_{OH}
V_{OL}
Y OUTPUT
W OUTPUT

STROBE-TO-OUTPUT VOLTAGE WAVEFORMS



t_0
t_1
90%
1.5V
10%
V_{IH}
V_{IL}
SELECT INPUT (See Notes 3 and 4)
t_p
t_{PLH}
t_{PHL}
V_{OH}
V_{OL}
W OUTPUT
Y OUTPUT

SELECT INPUT-TO-OUTPUT VOLTAGE WAVEFORMS



t_1
t_0
90%
1.5V
10%
V_{IH}
V_{IL}
E_0 OR D_0 INPUT (See Notes 2 and 4)
t_p
t_{PLH}
t_{PHL}
V_{OH}
V_{OL}
W OUTPUT
Y OUTPUT

DATA INPUT-TO-OUTPUT VOLTAGE WAVEFORMS

NOTES:

1. When measuring strobe to output times select input is at a LOW level, E_0 or D_0 is at a HIGH level, $V_1 = 4.5$ V.
2. When measuring dtat input-to-output times strobe and select inputs are at a LOW level and $V_1 = 4.5$ V.
3. When measuring select input-to-output times strobe input is at a LOW level, data input is at a HIGH level and $V_1 = 0$.
4. The input pulse has the following V_{IL} characteristics: $V_{IH} = 3$ V, $V_{IL} = 0$ V; $t_1 = t_0 = 10$ ns, PRR = 1 MHz, duty cycle = 50%, and generator $Z_{out} \approx 50\Omega$.

Fig. A SWITCHING TIMES

[†] Tests, as shown, are for the 93150/54150, 74150. Identical tests as spplicable are performed for the 93151/54151, 74151 and 93152/54152, 74152.

TTL/MSI 93153/54153, 74153

DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER

DESCRIPTION — The 93153/94153, 74153 is a monolithic, high speed, Dual 4-Input Digital Multiplexer. It consists of two multiplexing circuits with separate strobe inputs for each of the two 4-line sections, and with common input select logic. Active pull up outputs ensure high drive and high speed performance with a full fan out of 10 unit loads in the LOW state. Typical power dissipation is 180 mW.

PIN NAMES		LOADING
1G, 2G, $1C_{0-3}$, $2C_{0-3}$, A, B	Inputs	1 U.L.
1Y, 2Y	Outputs	10 U.L.

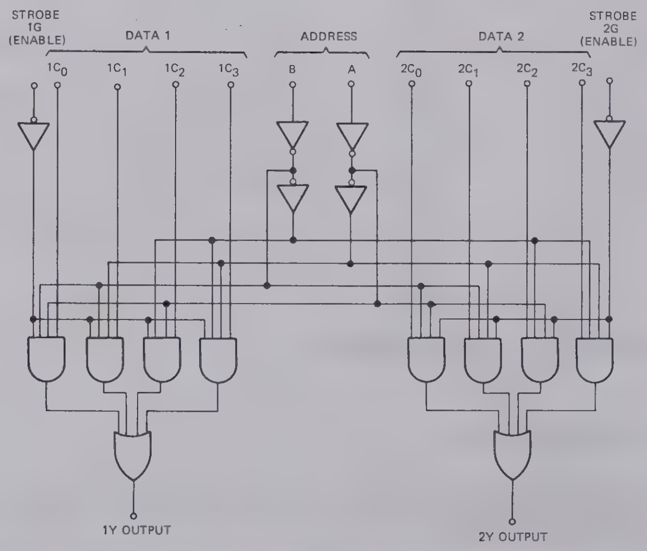
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE

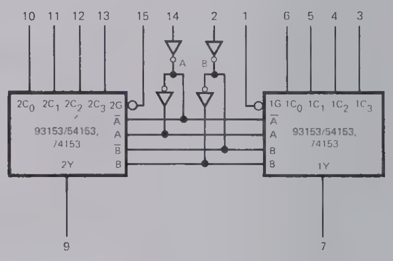
ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C_0	C_1	C_2	C_3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs A and B are common to both sections
H = HIGH level, L = LOW level, X = irrelevant

LOGIC DIAGRAM

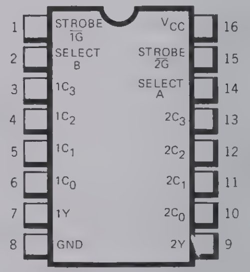

STROBE 1G (ENABLE)
DATA 1
1C0
1C1
1C2
1C3
ADDRESS
B
A
DATA 2
2C0
2C1
2C2
2C3
STROBE 2G (ENABLE)
1Y OUTPUT
2Y OUTPUT

LOGIC SYMBOL

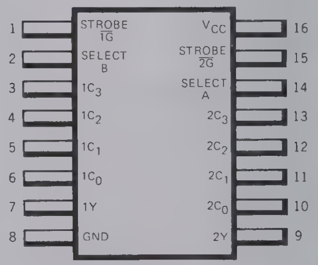

10
11
12
13
15
14
2
1
6
5
4
3
2C0
2C1
2C2
2C3
2G
A
B
93153/54153, /4153
2Y
1G
1C0
1C1
1C2
1C3
93153/54153, /4153
1Y
9
7

V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAM
DIP (TOP VIEW)


1
2
3
4
5
6
7
8
STROBE 1G
SELECT B
1C3
1C2
1C1
1C0
1Y
GND
16
15
14
13
12
11
10
9
VCC
STROBE 2G
SELECT A
2C3
2C2
2C1
2C0
2Y

FLATPAK (TOP VIEW)


1
2
3
4
5
6
7
8
STROBE 1G
SELECT B
1C3
1C2
1C1
1C0
1Y
GND
16
15
14
13
12
11
10
9
VCC
STROBE 2G
SELECT A
2C3
2C2
2C1
2C0
2Y

Positive Logic: See Truth Table.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93153XM/54153XM			93153XC/74153XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 2)	MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage	1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage	1 & 2
V_{OH}	Output HIGH Voltage	2.4	3.1		Volts	V_{CC} = MIN., I_{OH} = -800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	1
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	2
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 (each input)	3
I_{OS}	Output Short Circuit Current (Note 3)	-20		-55	mA	93153/54153 V_{CC} = MAX.	4
		-18		-57	mA	93153/74153	
I_{CCL}	Supply Current LOW		36	52	mA	93153/54153 V_{CC} = MAX.	5
			36	60	mA	93153/74153	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH} t_{PHL}	Data Input to Y Output		12 15	18 23	ns	V_{CC} = 5.0 V C_L = 30 pF R_L = 400 Ω	A
t_{PLH} t_{PHL}	Address Input to Y Output		22 22	34 34	ns		
t_{PLH} t_{PHL}	Strobe Input to Y Output		19 15	30 23	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

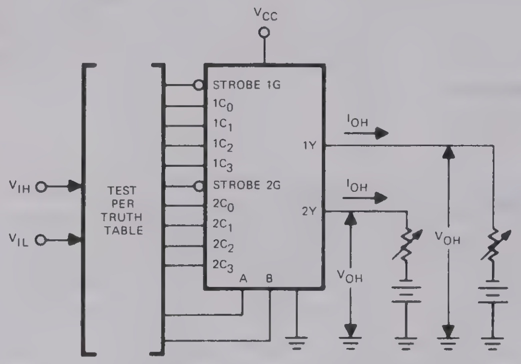

V_{CC}
STROBE 1G
$1C_0$
$1C_1$
$1C_2$
$1C_3$
STROBE 2G
$2C_0$
$2C_1$
$2C_2$
$2C_3$
A
B
1Y
2Y
I_{OH}
I_{OH}
V_{OH}
V_{OH}
V_{IH}
V_{IL}
TEST PER TRUTH TABLE

Fig. 1 V_{IH}, V_{IL}, V_{OH}

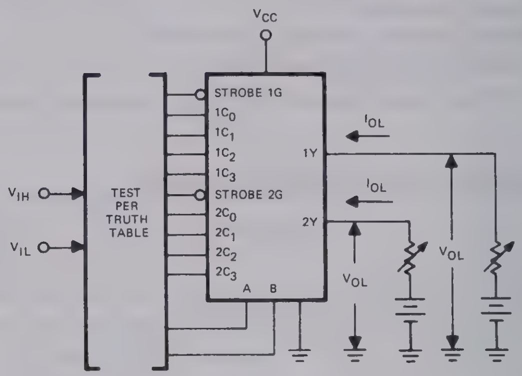
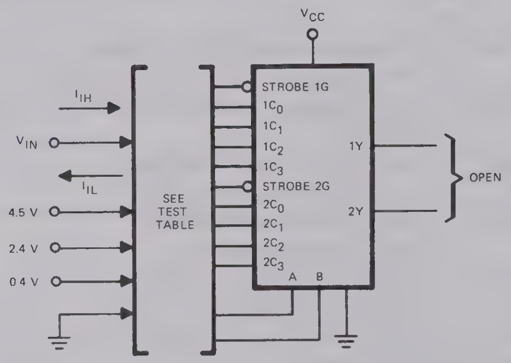

V_{CC}
STROBE 1G
$1C_0$
$1C_1$
$1C_2$
$1C_3$
STROBE 2G
$2C_0$
$2C_1$
$2C_2$
$2C_3$
A
B
1Y
2Y
I_{OL}
I_{OL}
V_{OL}
V_{OL}
V_{IH}
V_{IL}
TEST PER TRUTH TABLE

Fig. 2 V_{IH}, V_{IL}, V_{OL}


V_{CC}
I_{IH}
V_{IN}
I_{IL}
4.5 V
2.4 V
0.4 V
SEE TEST TABLE
STROBE 1G
$1C_0$
$1C_1$
$1C_2$
$1C_3$
STROBE 2G
$2C_0$
$2C_1$
$2C_2$
$2C_3$
A
B
1Y
2Y
OPEN

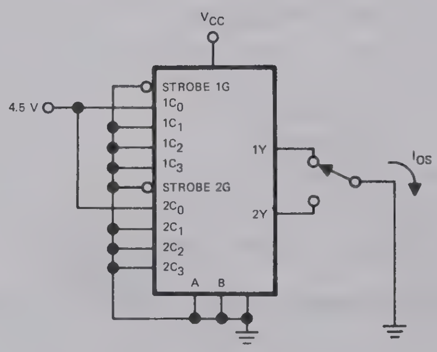
TEST TABLE

INPUT CONDITIONS				APPLY V_{IN}	
B	A	1G	2G	TEST I_{IL}	TEST I_{IH}
L	L	H	H		$1C_3$, $2C_3$
L	H	H	H		$1C_2$, $2C_2$
H	L	H	H		$1C_1$, $2C_1$
H	H	H	H		A,B, 1G, 2G, $1C_0$, $2C_0$
L	L	L	L	A,B, 1G, 2G, $1C_0$, $2C_0$	
L	H	L	L	$1C_1$, $2C_1$	
H	L	L	L	$1C_2$, $2C_2$	
H	H	L	L	$1C_3$, $2C_3$	

H = 2.4 V, L = 0.4 V

Note: Each input is tested separately. When I_{IH} is tested, all C inputs not under test are grounded. When I_{IL} is tested, all C inputs not under test are at 4.5 V.

Fig. 3 I_{IH}, I_{IL}


V_{CC}
4.5 V
STROBE 1G
$1C_0$
$1C_1$
$1C_2$
$1C_3$
STROBE 2G
$2C_0$
$2C_1$
$2C_2$
$2C_3$
A
B
1Y
2Y
I_{OS}

Note: Each output is tested separately.

Fig. 4 I_{OS}

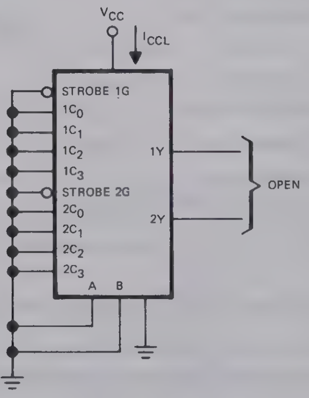
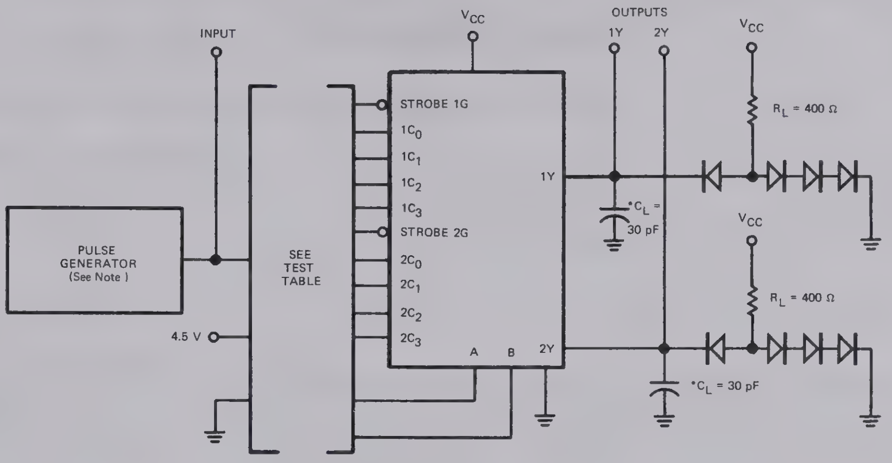

V_{CC}
I_{CCL}
STROBE 1G
$1C_0$
$1C_1$
$1C_2$
$1C_3$
STROBE 2G
$2C_0$
$2C_1$
$2C_2$
$2C_3$
A
B
1Y
2Y
OPEN

Fig. 5 I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

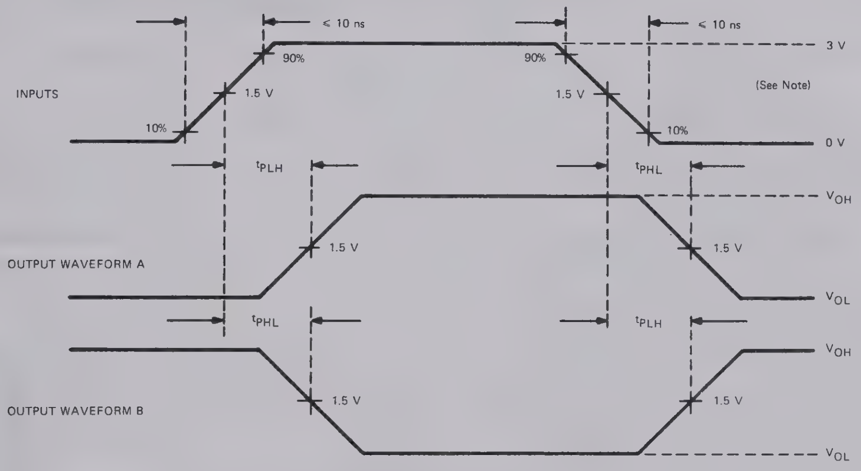
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS


INPUT
VCC
OUTPUTS
1Y
2Y
VCC
RL = 400 Ω
STROBE 1G
1C0
1C1
1C2
1C3
1Y
STROBE 2G
2C0
2C1
2C2
2C3
A
B
2Y
*CL = 30 pF
VCC
RL = 400 Ω
*CL = 30 pF
PULSE GENERATOR (See Note)
SEE TEST TABLE
4.5 V

*Includes probe and jig capacitance.

TEST CIRCUIT


≤ 10 ns
≤ 10 ns
3 V
90%
90%
INPUTS
1.5 V
1.5 V
(See Note)
10%
10%
0 V
tPLH
tPHL
VOH
OUTPUT WAVEFORM A
1.5 V
1.5 V
VOL
tPHL
tPLH
VOH
OUTPUT WAVEFORM B
1.5 V
1.5 V
VOL

NOTE: The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

VOLTAGE WAVEFORMS

TEST TABLE

INPUTS							OUTPUT Y WAVEFORM
B	A	C_0	C_1	C_2	C_3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5V	X	INPUT	X	X	GND	A
4.5V	GND	X	X	INPUT	X	GND	A
4.5V	4.5V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5V	X	X	GND	A
INPUT	GND	GND	X	4.5V	X	GND	A
GND	GND	4.5V	X	X	X	INPUT	B

X = irrelevant

Fig. A SWITCHING TIMES

TTL/MSI 93164/54164, 74164

8-BIT SERIAL TO PARALLEL CONVERTER

TO BE ANNOUNCED

DESCRIPTION — The 93164/54164, 74164 are 8-Bit Shift Registers with gated serial inputs and an asynchronous clear facility. The gated serial inputs (A and B) permit control over incoming data, as a LOW at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the LOW level at the next clock pulse. A HIGH level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH, but only information meeting the setup requirements will be entered. Clocking occurs on the LOW to HIGH level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects and are buffered to present one TTL load.

PIN NAMES		LOADING
CP	Clock Pulse Input	1 U.L.
$\overline{C}_L$	Clear Input	1 U.L.
A, B	Serial Inputs	1 U.L.
Q_A to Q_H	Parallel Outputs	5 U.L.

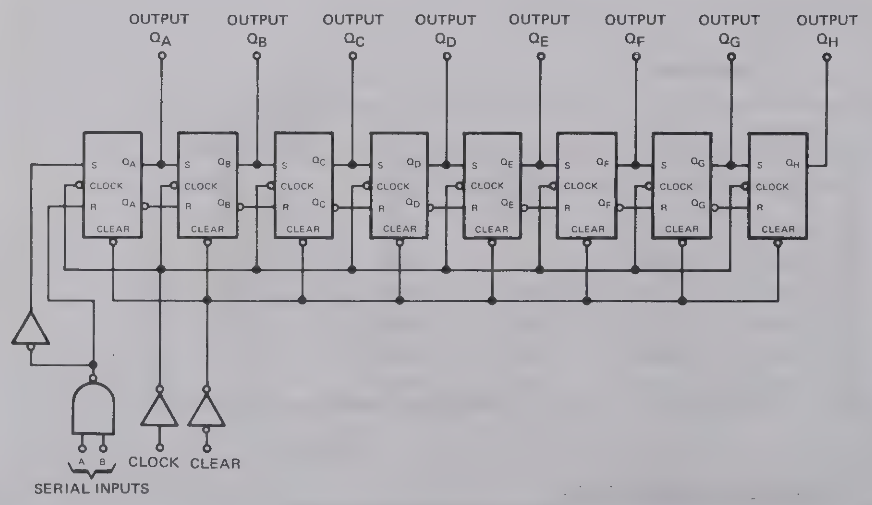
1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

TRUTH TABLE

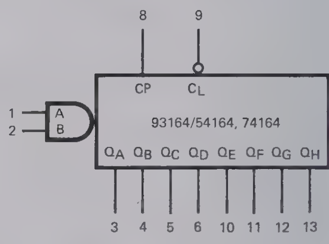
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

LOGIC DIAGRAM

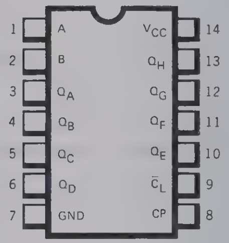

OUTPUT Q_A
OUTPUT Q_B
OUTPUT Q_C
OUTPUT Q_D
OUTPUT Q_E
OUTPUT Q_F
OUTPUT Q_G
OUTPUT Q_H
S
CLOCK
R
CLEAR
A
B
SERIAL INPUTS
CLOCK
CLEAR

LOGIC SYMBOL

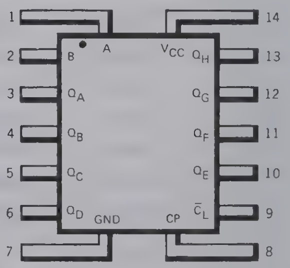

8
9
CP
C_L
1
2
A
B
93164/54164, 74164
Q_A Q_B Q_C Q_D Q_E Q_F Q_G Q_H
3 4 5 6 10 11 12 13

V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)


1 A
2 B
3 Q_A
4 Q_B
5 Q_C
6 Q_D
7 GND
14 V_{CC}
13 Q_H
12 Q_G
11 Q_F
10 Q_E
9 $\overline{C}_L$
8 CP

FLATPAK (TOP VIEW)


1 A
2 B
3 Q_A
4 Q_B
5 Q_C
6 Q_D
7 GND
14 V_{CC}
13 Q_H
12 Q_G
11 Q_F
10 Q_E
9 $\overline{C}_L$
8 CP

LOW input to clear resets all outputs to the LOW level.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93164XM/54164XM			93164XC/74164XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Logic Level			10			10	U.L.
	LOW Logic Level			5.0			5.0	
Input Clock Frequency, f_{CLOCK}		0		25	0		25	MHz
Width of Clock or Clear Input Pulse t_{PW}		20			20			ns
Data Setup Time, t_{setup} (See Fig. A)		15			15			ns
Data Hold Time, t_{HOLD} (See Fig. A)		0			0			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}	
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MAX., I_{IN} = −12 mA	
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 8.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	−10		−27.5	mA	93164/54164	V_{CC} = MAX.
		−9.0		−27.5	mA	93164/74164	
I_{CC}	Supply Current		30		mA	V_{IN}(clock) = 0.4V	V_{CC} = MAX. (Note 4)
			37	54	mA	V_{IN}(clock) = 2.4V	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
f_{max}	Maximum Input Count Frequency	25	36		MHz	C_L = 15 pF	V_{CC} = 5.0 V R_L = 800Ω (See Fig. A)
t_{PHL}	Turn On Delay Clear to Outputs		24	36	ns	C_L = 15 pF	
			28	42		C_L = 50 pF	
t_{PLH}	Turn Off Delay Clock to Outputs	8.0	17	27	ns	C_L = 15 pF	
		10	20	30		C_L = 50 pF	
t_{PHL}	Turn On Delay Clock to Outputs	10	21	32	ns	C_L = 15 pF	
		10	25	37		C_L = 50 pF	

NOTES:

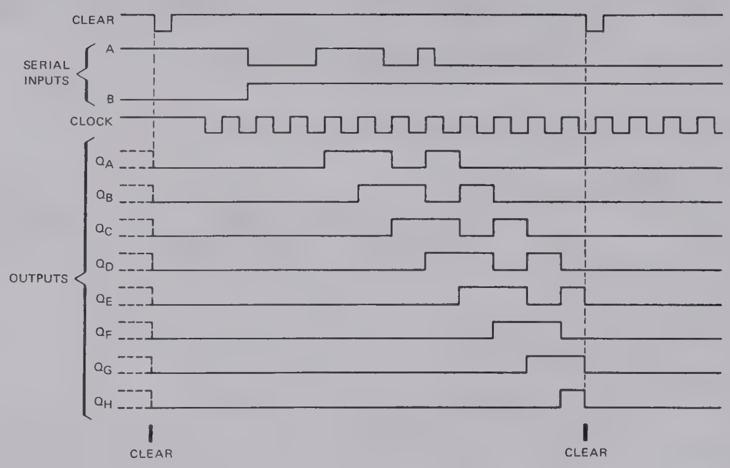
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than two outputs should be shorted at a time.

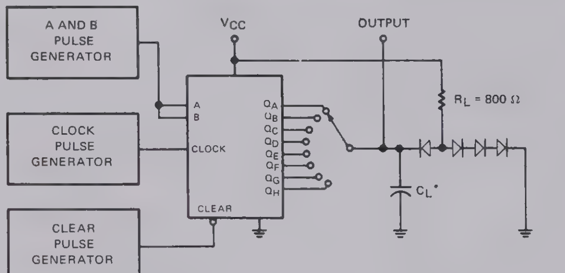
(4) Measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR AND INHIBIT SEQUENCES


CLEAR
SERIAL INPUTS
A
B
CLOCK
OUTPUTS
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
Q_H
CLEAR
CLEAR

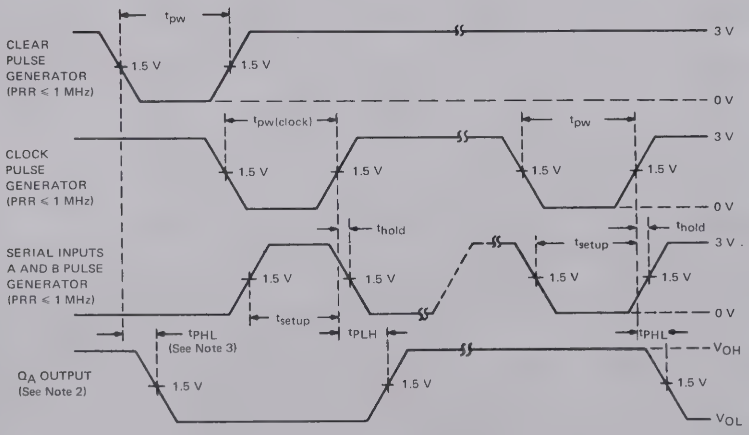
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS


A AND B PULSE GENERATOR
CLOCK PULSE GENERATOR
CLEAR PULSE GENERATOR
V_{CC}
OUTPUT
A
B
CLOCK
CLEAR
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
Q_H
$R_L = 800\ \Omega$
C_L*

*C_L includes probe and jig capacitance.

TEST CIRCUIT


CLEAR PULSE GENERATOR (PRR ⩽ 1 MHz)
CLOCK PULSE GENERATOR (PRR ⩽ 1 MHz)
SERIAL INPUTS A AND B PULSE GENERATOR (PRR ⩽ 1 MHz)
Q_A OUTPUT (See Note 2)
t_{pw}
$t_{pw(clock)}$
t_{hold}
t_{setup}
t_{PHL} (See Note 3)
t_{PLH}
t_{PHL}
1.5 V
3 V
0 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS

NOTES:

1. The pulse generators have the following characteristics: $t_r \leqslant 10\text{ns}$, $t_f \leqslant 10\text{ns}$, duty cycle ⩽ 50%, $Z_{OUT} = 50\Omega$.
2. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
3. Outputs are set to the HIGH level prior to the measurement of t_{PHL} from the clear input.

Fig. A SWITCHING TIMES

TTL/MSI 93165/54165, 74165
8-BIT PARALLEL TO SERIAL CONVERTER

DESCRIPTION – The 93165/54165, 74165 is an 8-Bit Serial Shift Register which features parallel-in access to each stage, gated clock input, complementary outputs from the last stage and input clamp diodes. Parallel-in access to each stage is made possible by eight individual direct data inputs which are enabled by a LOW level at the shift/load input.

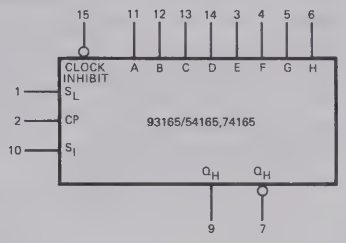
Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs HIGH inhibits clocking, and holding either clock input LOW with the load input HIGH enables the other clock input. The clock-inhibit input should be changed to the HIGH level only while the clock input is HIGH. Parallel loading is inhibited as long as the load input is HIGH. When taken LOW, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

Typical power dissipation is 210 mW and maximum input clock frequency is typically 26 MHz.

PIN NAMES		LOADING
A to H	Parallel Inputs	1 U.L.
S_I	Serial Input	1 U.L.
CP	Clock Input	1 U.L.
S_L	Shift Load	2 U.L.
$\overline{\text{CLOCK INHIBIT}}$	Clock Inhibit	1 U.L.
Q_H, $\overline{Q}_H$	Outputs	10 U.L.

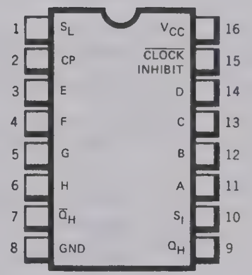
NOTE: 1 U.L. = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL

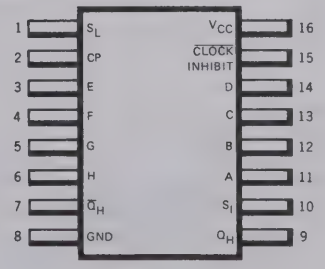

15
11
12
13
14
3
4
5
6
CLOCK INHIBIT
A
B
C
D
E
F
G
H
1
S_L
2
CP
10
S_I
93165/54165,74165
Q_H
Q̄_H
9
7

V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

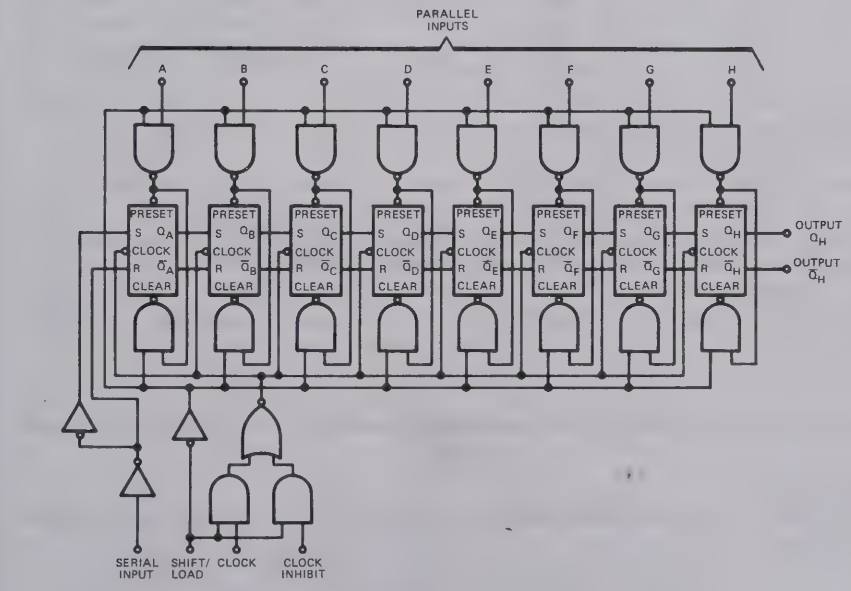

1 S_L
2 CP
3 E
4 F
5 G
6 H
7 Q̄_H
8 GND
16 V_CC
15 CLOCK INHIBIT
14 D
13 C
12 B
11 A
10 S_I
9 Q_H

FLATPAK (TOP VIEW)


1 S_L
2 CP
3 E
4 F
5 G
6 H
7 Q̄_H
8 GND
16 V_CC
15 CLOCK INHIBIT
14 D
13 C
12 B
11 A
10 S_I
9 Q_H

Positive Logic: See Description.

LOGIC DIAGRAM


PARALLEL INPUTS
A
B
C
D
E
F
G
H
PRESET
S
CLOCK
R
CLEAR
Q_A
Q̄_A
Q_B
Q̄_B
Q_C
Q̄_C
Q_D
Q̄_D
Q_E
Q̄_E
Q_F
Q̄_F
Q_G
Q̄_G
Q_H
Q̄_H
OUTPUT Q_H
OUTPUT Q̄_H
SERIAL INPUT
SHIFT/ LOAD
CLOCK
CLOCK INHIBIT

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93165XM/54165XM			93165XC/74165XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		15			15			ns
Clock-enable setup time, t_{setup} (See Fig. 1)		30			30			ns
Parallel input setup time, t_{setup} (See Fig. 1)		10			10			ns
Serial input setup time, t_{setup} (see Fig. 2)		20			20			ns
Shift setup time, t_{setup} (See Fig. 2)		45			45			ns
Hold time at any input, t_{hold}		0			0			ns

X=package type; F for Flatpak, D for Cèramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Threshold Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Threshold Voltage	
V_{CD}	Input Clamp Diode Voltage				-1.5	Volts	V_{CC} = MAX., I_{IN} = –12 mA	
V_{OH}	Output HIGH Voltage		2.4			Volts	V_{CC} = MIN., I_{OH} = –800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
V_{OL}	Output LOW Voltage				0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
I_I	Input Current at MAX. Input Voltage				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current	Other Inputs			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
		Load Inputs			80			
I_{IL}	Input LOW Current	Other Inputs			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
		Load Inputs			-3.2			
I_{OS}	Output Short Circuit Current (Note 3)		-20		-55	mA	93165/54165	V_{CC} = MAX.
			-18		-55	mA	93165/74165	
I_{CC}	Supply Current (Note 4)			42	63	mA	V_{CC} = MAX.	

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

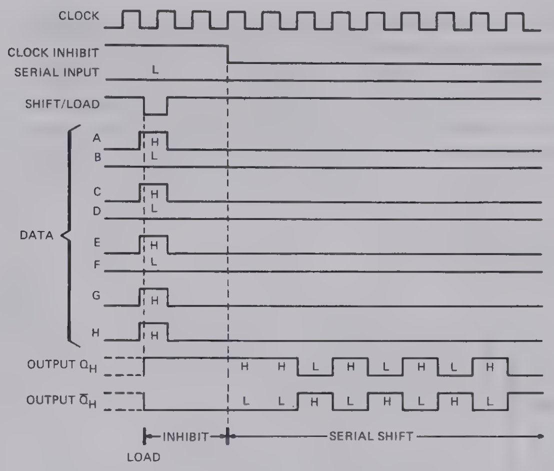
(3) Not more than one output should be shorted at a time.

(4) With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

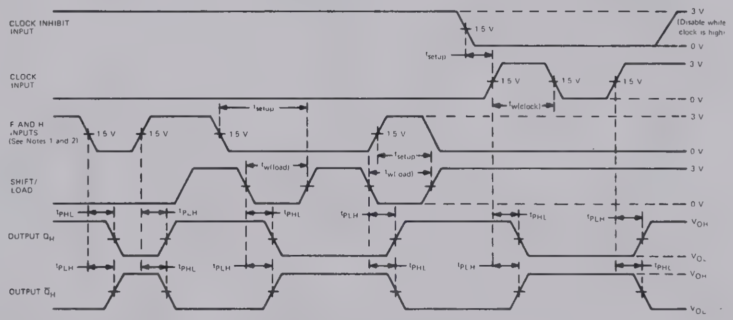
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
f_{max}	Max. Input Count Frequency	20	26		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 400\Omega$ (See Figs. 1 Thru 3)
t_{PLH} t_{PHL}	Load Input to Any Output		21 27	31 40	ns	
t_{PLH} t_{PHL}	Clock Input to Any Output		16 21	24 31	ns	
t_{PLH} t_{PHL}	H Input to Q_H Output		11 24	17 36	ns	
t_{PLH} t_{PHL}	H Input to $\overline{Q}_H$ Output		18 18	27 27	ns	

TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCES


CLOCK
CLOCK INHIBIT
SERIAL INPUT
L
SHIFT/LOAD
DATA
A
B
C
D
E
F
G
H
H
L
OUTPUT Q_H
OUTPUT Q̄_H
H H L H L H L H
L L H L H L H L
INHIBIT
SERIAL SHIFT
LOAD

PARAMETER MEASUREMENT INFORMATION

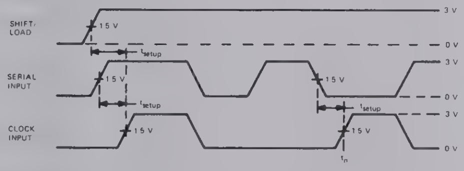
SWITCHING CHARACTERISTICS


CLOCK INHIBIT INPUT
CLOCK INPUT
F AND H INPUTS (See Notes 1 and 2)
SHIFT/LOAD
OUTPUT Q_H
OUTPUT Q̄_H
1.5 V
3 V
0 V
(Disable while clock is high)
t_setup
t_w(clock)
t_w(load)
t_PHL
t_PLH
V_OH
V_OL

NOTES:

1. The remaining six data inputs and the serial input are LOW.
2. Prior to test, HIGH level data is loaded into H input.
3. The input pulse generators have the following characteristics:
   $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns, PRR $\leqslant 1$ MHz, duty cycle $\leqslant 50\%$, $Z_{out} \approx 50\ \Omega$. When testing f_{max}, vary clock PRR.

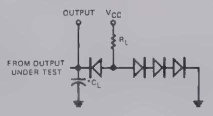
Fig. 1 VOLTAGE WAVEFORMS


SHIFT/LOAD
SERIAL INPUT
CLOCK INPUT
1.5 V
3 V
0 V
t_setup
t_n

NOTES:

1. The eight data inputs and the clock-inhibit input are LOW. Results are monitored at output Q_H at t_{n+7}.
2. The inputs pulse generators have the following characteristics:
   $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns, PRR $\leqslant 1$ MHz, duty cycle $\leqslant 50\%$, $Z_{out} \approx 50\ \Omega$.

Fig. 2 VOLTAGE WAVEFORMS


OUTPUT
V_CC
R_L
FROM OUTPUT UNDER TEST
*C_L

*C_L includes probe and jig capacitance.

Fig. 3 LOAD CIRCUIT FOR SWITCHING TESTS

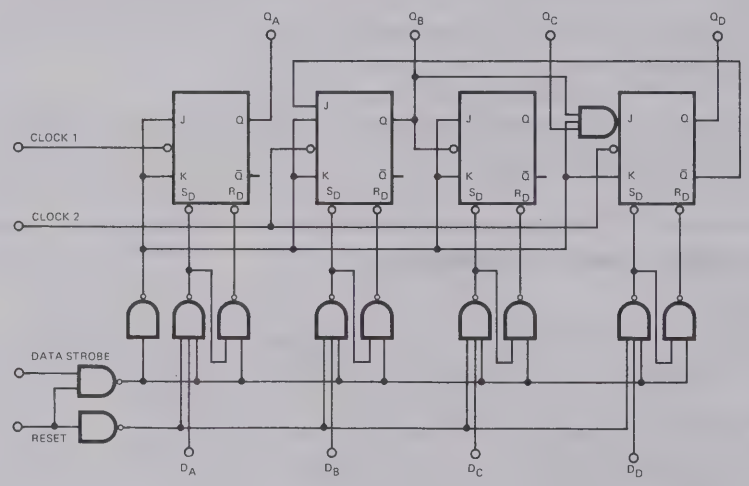
TTL/MSI 93176/54176, 74176
93177/54177,74177
BCD DECADE/4-BIT BINARY COUNTER

TO BE ANNOUNCED

DESCRIPTION – The 93176/54176, 74176 is a Decade Counter that can be connected in BCD counting mode, in a divide-by-two and divide-by-five configuration, or in the bi-quinary mode. The 93177/54177, 74177 can be connected as a divide-by-two, eight, or sixteen counter. Both counters feature strobed parallel-entry capability. A LOW at the Data Strobe inputs transfers the data at the parallel inputs to the outputs. Each counter is provided with a reset input, which when LOW resets the outputs to LOW state. The counting operation is performed on the negative going edge of the clock pulse.

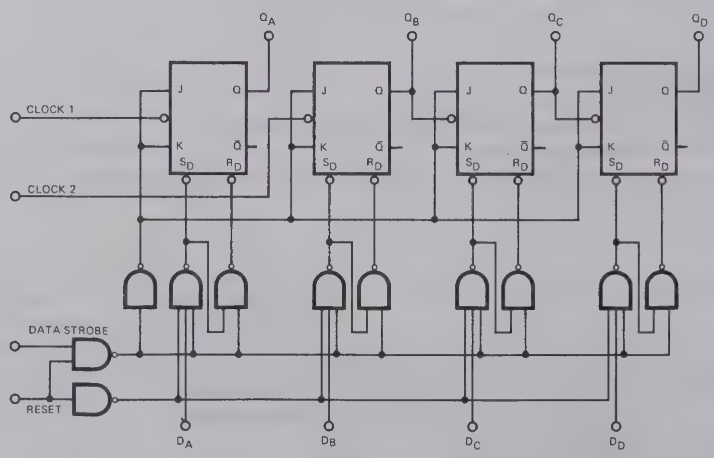
LOGIC DIAGRAM

93176/54176, 74176



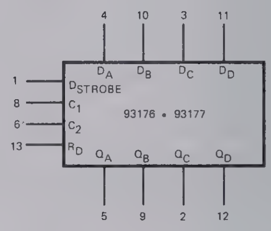
Q_A
Q_B
Q_C
Q_D
CLOCK 1
CLOCK 2
J
K
Q
$\bar{Q}$
S_D
R_D
DATA STROBE
RESET
D_A
D_B
D_C
D_D

93177/54177, 74177



Q_A
Q_B
Q_C
Q_D
CLOCK 1
CLOCK 2
J
K
Q
$\bar{Q}$
S_D
R_D
DATA STROBE
RESET
D_A
D_B
D_C
D_D

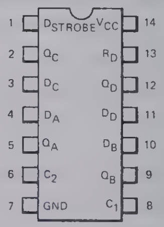
LOGIC SYMBOL



4
10
3
11
D_A
D_B
D_C
D_D
1
D_{STROBE}
8
C_1
6
C_2
13
R_D
93176 • 93177
Q_A
Q_B
Q_C
Q_D
5
9
2
12

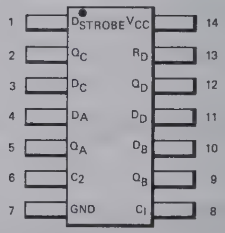
Pin numbers are shown for DIP only.

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1
D_{STROBE}
V_{CC}
14
2
Q_C
R_D
13
3
D_C
Q_D
12
4
D_A
D_D
11
5
Q_A
D_B
10
6
C_2
Q_B
9
7
GND
C_1
8

FLATPAK (TOP VIEW)



1
D_{STROBE}
V_{CC}
14
2
Q_C
R_D
13
3
D_C
Q_D
12
4
D_A
D_D
11
5
Q_A
D_B
10
6
C_2
Q_B
9
7
GND
C_1
8

TTL/MSI 93178/54178, 74178
93179/54179, 74179
4-BIT SHIFT REGISTERS

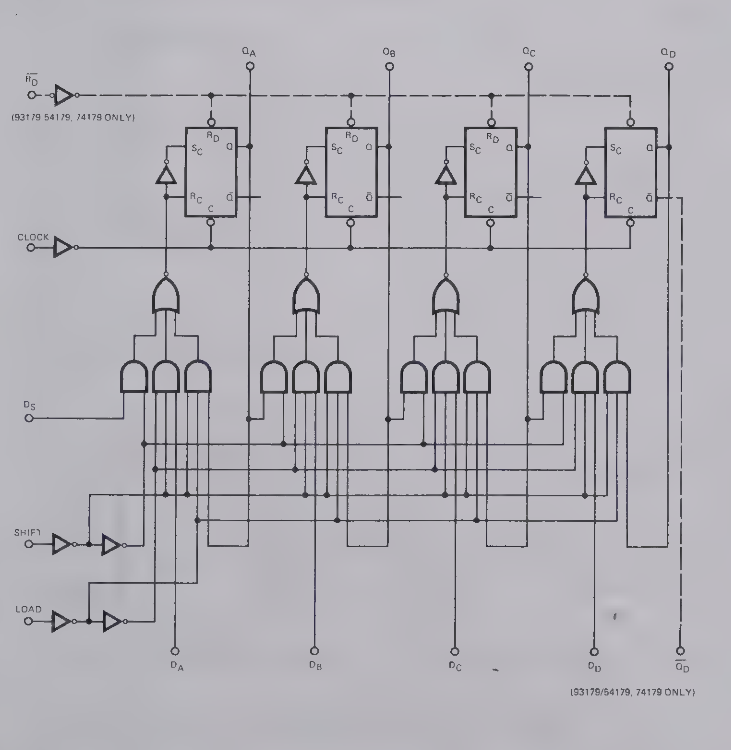
TO BE ANNOUNCED

DESCRIPTION — The 93178 and 93179 are 4-Bit Shift Registers with both serial and parallel data entry capability. The 93179 features a direct reset ($\overline{R}_D$), and a $\overline{D}_{out}$ line in addition to the available outputs of the 93178. The truth table below indicates the three possible control states: shift right, parallel entry and hold. The clock line is buffered to minimize input clock loading. All changes occur on the negative-going clock transition. Since data transfer is synchronous with the clock, data may be transferred in any serial/parallel input/output relationship.

TRUTH TABLE

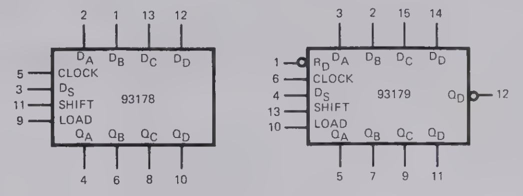
CONTROL STATE	LOAD	SHIFT
Hold	L	L
Parallel Entry	H	L
Shift Right	L	H
Shift Right	H	H

LOGIC DIAGRAM



$\overline{R}_D$
(93179 54179, 74179 ONLY)
Q_A
Q_B
Q_C
Q_D
S_C
R_D
Q
R_C
C
$\overline{Q}$
CLOCK
D_S
SHIFT
LOAD
D_A
D_B
D_C
D_D
$\overline{Q}_D$
(93179/54179, 74179 ONLY)

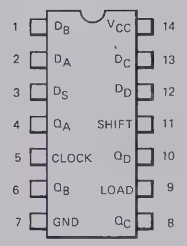
LOGIC SYMBOL



2
1
13
12
5
3
11
9
CLOCK
D_S
SHIFT
LOAD
D_A
D_B
D_C
D_D
93178
Q_A
Q_B
Q_C
Q_D
4
6
8
10
3
2
15
14
1
6
4
13
10
$\overline{R}_D$
CLOCK
D_S
SHIFT
LOAD
93179
Q_D
12
Q_A
Q_B
Q_C
Q_D
5
7
9
11

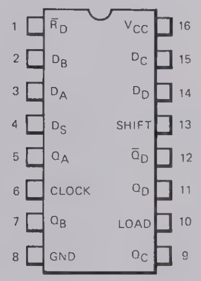
Pin numbers are shown for DIP only.

CONNECTION DIAGRAM
DIP (TOP VIEW)



1 D_B
2 D_A
3 D_S
4 Q_A
5 CLOCK
6 Q_B
7 GND
14 V_{CC}
13 D_C
12 D_D
11 SHIFT
10 Q_D
9 LOAD
8 Q_C

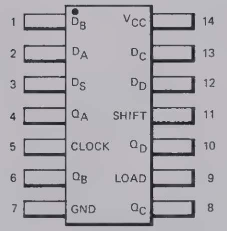
93178/54178, 74178



1 $\overline{R}_D$
2 D_B
3 D_A
4 D_S
5 Q_A
6 CLOCK
7 Q_B
8 GND
16 V_{CC}
15 D_C
14 D_D
13 SHIFT
12 $\overline{Q}_D$
11 Q_D
10 LOAD
9 Q_C

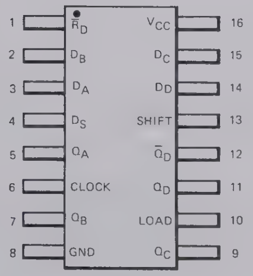
93179/54179, 74179

FLATPAK (TOP VIEW)



1 D_B
2 D_A
3 D_S
4 Q_A
5 CLOCK
6 Q_B
7 GND
14 V_{CC}
13 D_C
12 D_D
11 SHIFT
10 Q_D
9 LOAD
8 Q_C

93178/54178, 74178



1 $\overline{R}_D$
2 D_B
3 D_A
4 D_S
5 Q_A
6 CLOCK
7 Q_B
8 GND
16 V_{CC}
15 D_C
14 D_D
13 SHIFT
12 $\overline{Q}_D$
11 Q_D
10 LOAD
9 Q_C

93179/54179, 74179

TTL/MSI 93180/54180, 74180

8-BIT PARITY GENERATOR/CHECKER

DESCRIPTION — The 93180/54180 or 74180 are monolithic, 8-Bit Parity Check/Generators which feature control inputs and even/odd outputs to enhance operation in either odd or even parity applications. Cascading these circuits allows unlimited word length expansion. Typical application would be to generate and check parity on data being transmitted from one register to another. Typical power dissipation is 170 mW.

As with all Fairchild TTL products, all inputs are diode-clamped to minimize transmission-line effects and simplify system design.

PIN NAMES		**LOADING**
I_0 to I_7	Parity Inputs	1 U.L.
P_O	Odd Parity Input	2 U.L.
P_E	Even Parity Input	2 U.L.
ΣQ_O	Sum Odd Outputs	10 U.L.
ΣQ_E	Sum Even Outputs	10 U.L.

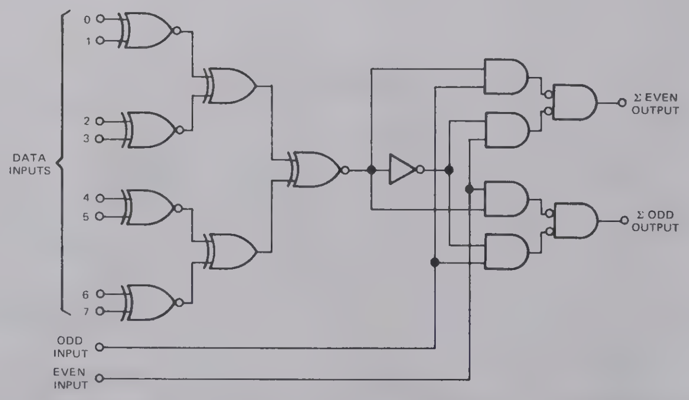
Note: 1 U.L. = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE

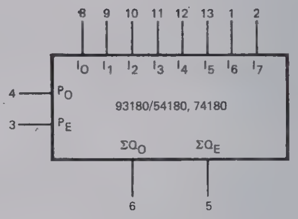
INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

X = irrelevant

LOGIC DIAGRAM

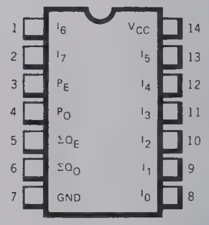

0
1
2
3
4
5
6
7
DATA INPUTS
Σ EVEN OUTPUT
Σ ODD OUTPUT
ODD INPUT
EVEN INPUT

LOGIC SYMBOL

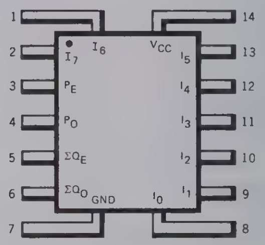

8
9
10
11
12
13
1
2
I0
I1
I2
I3
I4
I5
I6
I7
4
PO
3
PE
93180/54180, 74180
ΣQO
ΣQE
6
5

V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)


1
2
3
4
5
6
7
I6
I7
PE
PO
ΣQE
ΣQO
GND
VCC
I5
I4
I3
I2
I1
I0
14
13
12
11
10
9
8

FLATPAK (TOP VIEW)


1
2
3
4
5
6
7
I7
I6
PE
PO
ΣQE
ΣQO
GND
I0
VCC
I5
I4
I3
I2
I1
14
13
12
11
10
9
8

Positive logic: See truth table.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93180XM/54180XM			93180XC/74180XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	LOW Level			10			10	U.L.
	HIGH Level			20			20	

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		1
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −800 µA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1
I_{IH}	Input HIGH Current at Each Data Input			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V		2
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IH}	Input HIGH Current at Even or Odd Input			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V		2
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at Each Data Input			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		2
I_{IL}	Input LOW Current at Even or Odd Input			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		2
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	93180/54180	V_{CC} = MAX.	3
		−18		−55	mA	93180/74180		
I_{CC}	Supply Current		34	49	mA	93180/74180	V_{CC} = MAX.	3 & 4
			34	56	mA	93180/54180		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH} t_{PHL}	Data Input to Σ Even Output		40 45	60 68	ns	V_{CC} = 5.0 V C_L = 15 pF	A
t_{PLH} t_{PHL}	Data Input to Σ Odd Output		32 25	48 38	ns	R_L = 400Ω Odd Input Ground	
t_{PLH} t_{PHL}	Data Input to Σ Even Output		32 25	48 38	ns	V_{CC} = 5.0 V C_L = 15 pF	A
t_{PLH} t_{PHL}	Data Input to Σ Odd Output		40 45	60 68	ns	R_L = 400Ω Even Input Ground	
t_{PLH}	Even or Odd Input to Σ Even or Σ Odd Output		13	20	ns	V_{CC} = 5.0 V C_L = 15 pF	A
t_{PHL}	Even or Odd Input to Σ Even or Σ Odd Output		7.0	10	ns	R_L = 400Ω	

NOTES

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the particular circuit type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time.

(4) These voltage values are with respect to network ground terminal.

PARAMETER MEASUREMENT INFORMATION

dc TEST CIRCUITS*

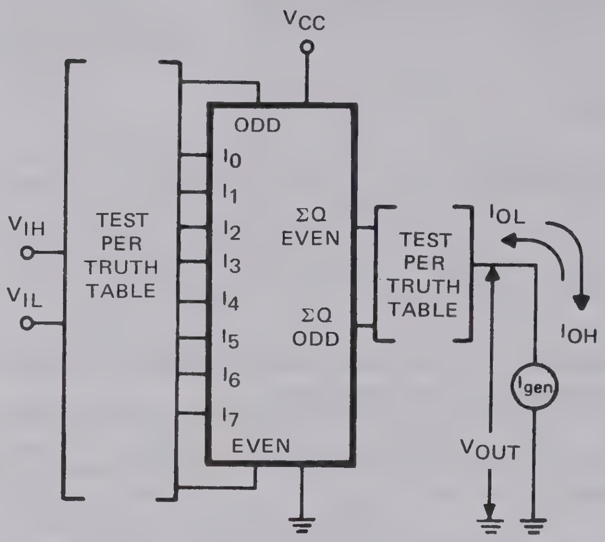
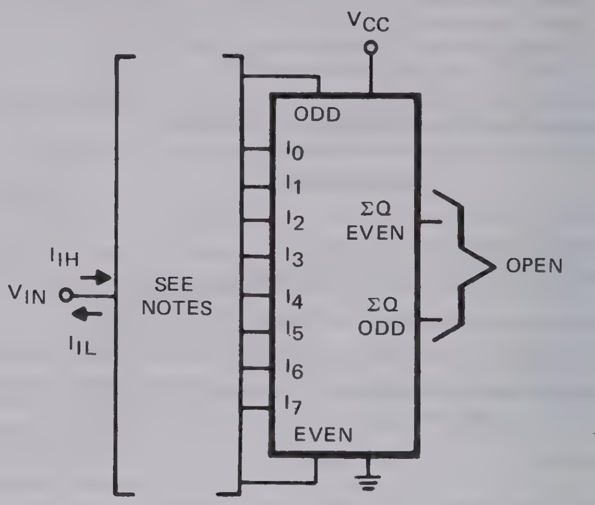
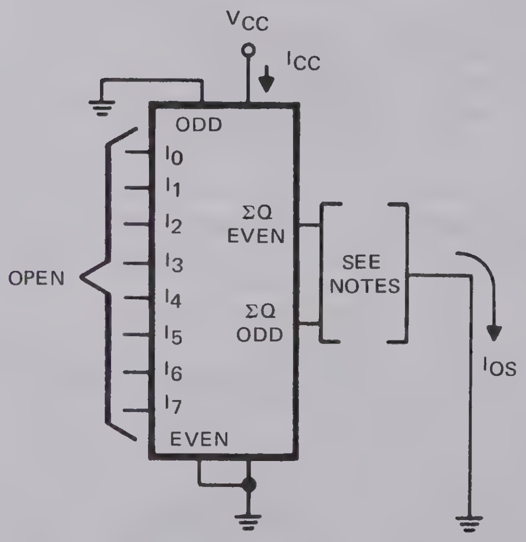

VCC
ODD
I0
I1
I2
I3
I4
I5
I6
I7
EVEN
ΣQ EVEN
ΣQ ODD
VIH
VIL
TEST PER TRUTH TABLE
TEST PER TRUTH TABLE
IOL
IOH
Igen
VOUT

Fig. 1


VCC
ODD
I0
I1
I2
I3
I4
I5
I6
I7
EVEN
ΣQ EVEN
ΣQ ODD
OPEN
IIH
VIN
IIL
SEE NOTES

NOTES:
1. Each output is tested separately.
2. Odd and even inputs are each tested for I_{IH} and I_{IL} with both an even-code and an odd-code applied at the data inputs.

Fig. 2


VCC
ICC
ODD
I0
I1
I2
I3
I4
I5
I6
I7
EVEN
ΣQ EVEN
ΣQ ODD
OPEN
SEE NOTES
IOS

NOTES:
1. Each output is tested separately.
2. When testing I_{CC} both outputs are open.

Fig. 3

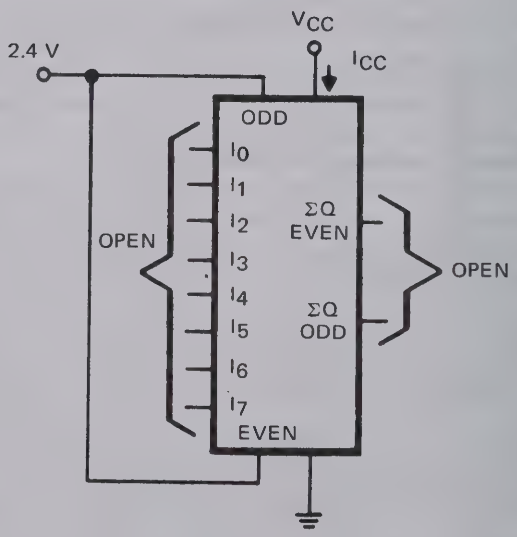
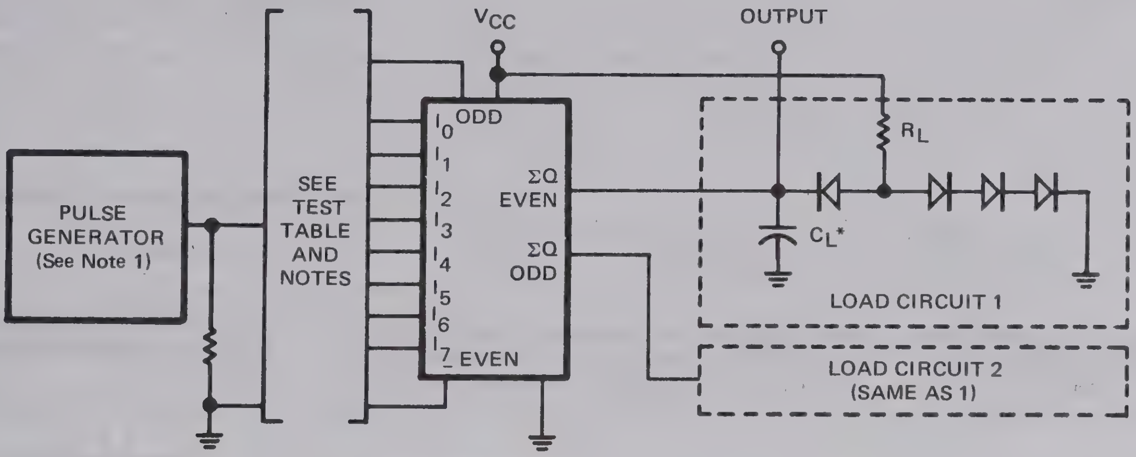

2.4 V
VCC
ICC
ODD
I0
I1
I2
I3
I4
I5
I6
I7
EVEN
ΣQ EVEN
ΣQ ODD
OPEN
OPEN

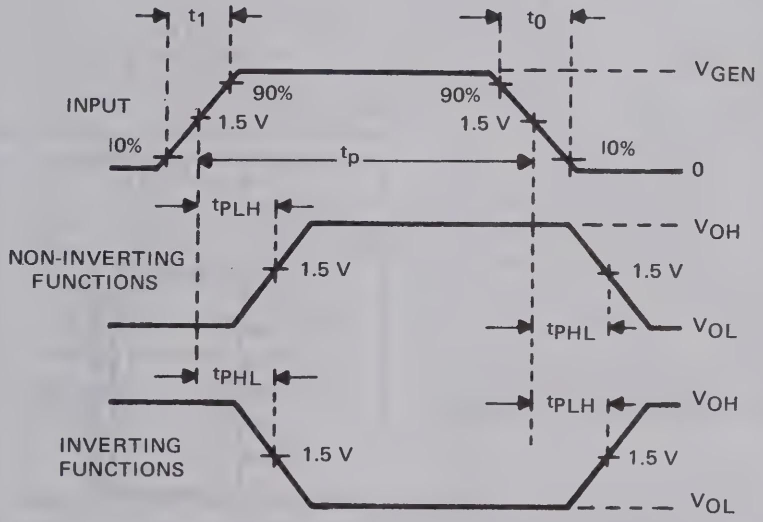
Fig. 4

PARAMETER MEASUREMENT INFORMATION (con't)

SWITCHING CHARACTERISTICS


VCC
OUTPUT
PULSE GENERATOR (See Note 1)
SEE TEST TABLE AND NOTES
I0 ODD
I1
I2
I3
I4
I5
I6
I7 EVEN
ΣQ EVEN
ΣQ ODD
RL
CL*
LOAD CIRCUIT 1
LOAD CIRCUIT 2 (SAME AS 1)

*C_L includes probe and jig capacitance.


t1
t0
VGEN
INPUT
90%
90%
1.5 V
1.5 V
10%
10%
tp
0
tPLH
VOH
NON-INVERTING FUNCTIONS
1.5 V
1.5 V
VOL
tPHL
tPHL
tPLH
VOH
INVERTING FUNCTIONS
1.5 V
1.5 V
VOL

VOLTAGE WAVEFORMS

NOTES:
1. The pulse generator has the following characteristics: $V_{gen} = 3V$, $t_1 = t_0 = 10$ ns, $t_p = 500$ ns, PRR = 1 MHz, and $Z_{OUT} \approx 50\ \Omega$.
2. Inputs not specified are open.

TEST TABLE†

INPUT CONDITIONS		OUTPUT TESTED
APPLY PULSE	GND	
0	ODD	Σ EVEN
1	ODD	Σ EVEN
2	ODD	Σ EVEN
3	ODD	Σ EVEN
4	ODD	Σ EVEN
5	ODD	Σ EVEN
6	ODD	Σ EVEN
7	ODD	Σ EVEN
0	ODD	Σ ODD
1	ODD	Σ ODD
2	ODD	Σ ODD
3	ODD	Σ ODD
4	ODD	Σ ODD
5	ODD	Σ ODD
6	ODD	Σ ODD
7	ODD	Σ ODD
EVEN	0	Σ EVEN
ODD	NONE	Σ EVEN
EVEN	NONE	Σ ODD
ODD	0	Σ ODD

†Repeat all but the last 4 tests with the even input grounded.

Fig. A — SWITCHING TIMES

TTL/MSI 93H183/54H183, 74H183

HIGH SPEED DUAL CARRY/SAVE FULL ADDER

DESCRIPTION — The 93H183/54H183, 74H183 features two independent, high speed, Full Adders. Typical average sum and carry propagation delay times are 11 ns. Each adder has an individual carry output from each bit for use in multiple-input, carry/save techniques to produce the true sum and true carry outputs.

PIN NAMES		**LOADING** (Note a)
1A, 1B, $1C_n$, 2A, 2B, $2C_n$	Inputs	3.75 U.L.
$1C_{n+1}$, 1Σ, $2C_{n+1}$, 2Σ	Outputs (Note b)	12.5 U.L.

NOTES:

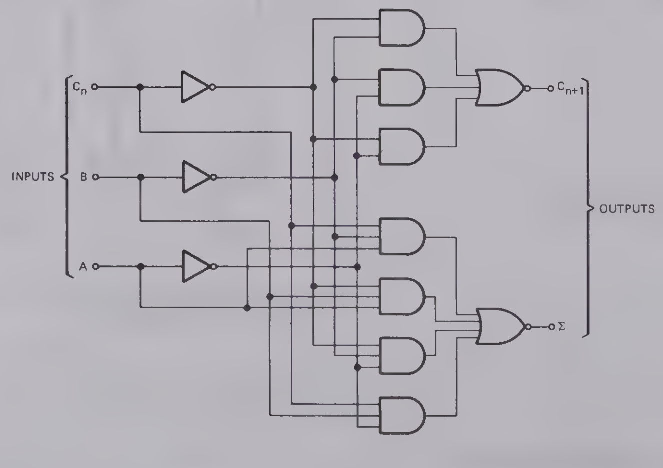
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. 12.5 U.L. is the LOW drive factor and 25 U.L. is the HIGH drive factor.

TRUTH TABLE

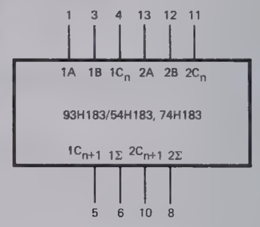
INPUTS			OUTPUTS	
C_n	B	A	Σ	C_{n+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

LOGIC DIAGRAM
(EACH ADDER)



INPUTS
Cn
B
A
Cn+1
Σ
OUTPUTS

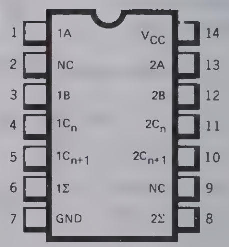
LOGIC SYMBOL



1 3 4 13 12 11
1A 1B 1Cn 2A 2B 2Cn
93H183/54H183, 74H183
1Cn+1 1Σ 2Cn+1 2Σ
5 6 10 8

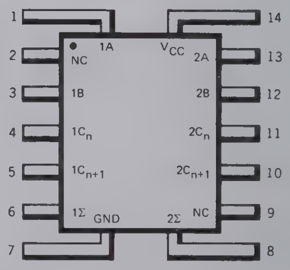
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 1A
2 NC
3 1B
4 1Cn
5 1Cn+1
6 1Σ
7 GND
14 VCC
13 2A
12 2B
11 2Cn
10 2Cn+1
9 NC
8 2Σ

FLATPAK (TOP VIEW)



1 1A
2 NC
3 1B
4 1Cn
5 1Cn+1
6 1Σ
7 GND
14 VCC
13 2A
12 2B
11 2Cn
10 2Cn+1
9 NC
8 2Σ

NC — No internal connection
Positive logic: See truth table

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	93H183XM/54H183XM			93H183XC/74H183XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −1 mA, V_{IH} = 2.0 V		1
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IL} = 0.8 V		2
I_{IH}	Input HIGH Current			150	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Any Input	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−6.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Any Input		3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.		4
I_{CCH}	Supply Current HIGH		40		mA	V_{CC} = MAX., V_{IN} = 4.5 V, All Outputs HIGH		5
I_{CCL}	Supply Current LOW		48	69	mA	93H183/54H183	V_{CC} = MAX., V_{IN} = 0 V All Outputs LOW	5
			48	75	mA	93H183/74H183		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280Ω	A
t_{PHL}	Turn On Delay Input to Output		12	18	ns		

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

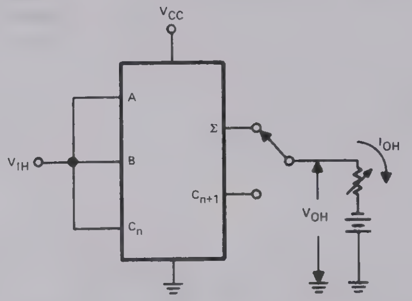
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

(4) Voltage values, except interemitter voltage, are with respect to network ground terminal.

PARAMETER MEASUREMENT INFORMATION

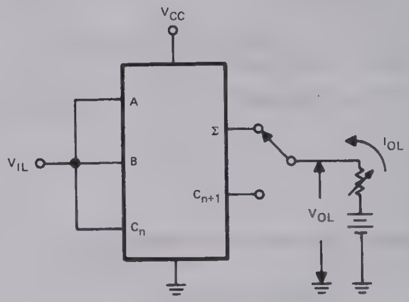
DC TEST CIRCUITS*



V_{CC}
A
B
C_n
Σ
C_{n+1}
V_{IH}
I_{OH}
V_{OH}

Each output is tested separately.

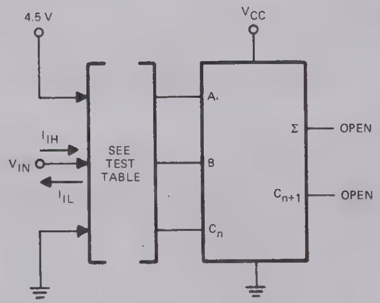
Fig. 1 — V_{IH}, V_{OH}



V_{CC}
A
B
C_n
Σ
C_{n+1}
V_{IL}
I_{OL}
V_{OL}

Each output is tested separately.

Fig. 2 — V_{IL}, V_{OL}



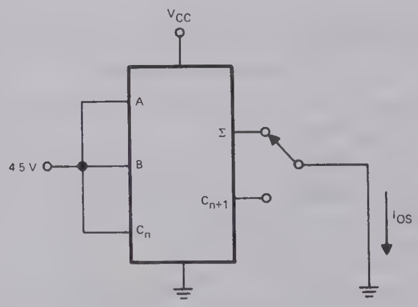
4.5 V
V_{CC}
I_{IH}
V_{IN}
I_{IL}
SEE TEST TABLE
A
B
C_n
Σ
OPEN
C_{n+1}
OPEN

Each input is tested for both combinations of states of the other inputs.

Fig. 3. — I_{IH}, I_{IL}

TEST TABLE

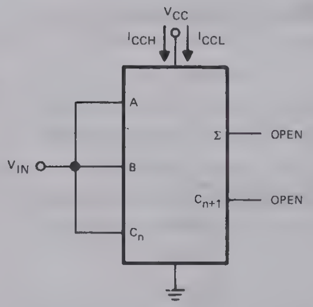
APPLY V_{IN}, MEASURE I_{IH}/I_{IL}	CONDITIONS ON OTHER INPUTS	
	4.5 V	GND
A	B, C_n	NONE
	B	C_n
	C_n	B
	NONE	B, C_n
B	A, C_n	NONE
	A	C_n
	C_n	A
	NONE	A, C_n
C_n	A, B	NONE
	A	B
	B	A
	NONE	A, B



V_{CC}
A
B
C_n
Σ
C_{n+1}
4.5 V
I_{OS}

Each output is tested separately.

Fig. 4 — I_{OS}



V_{CC}
I_{CCH}
I_{CCL}
A
B
C_n
Σ
OPEN
C_{n+1}
OPEN
V_{IN}

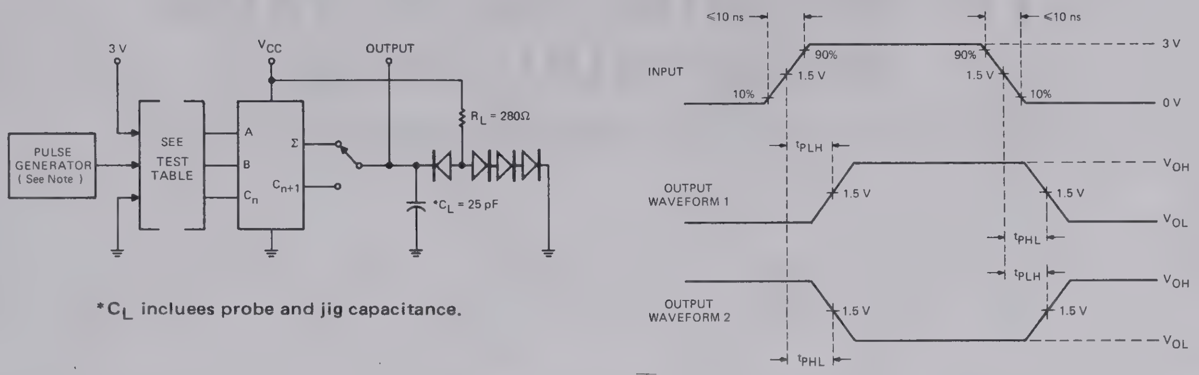
Both adders are tested simultaneously.

Fig. 5 — I_{CCH}, I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS


3 V
VCC
OUTPUT
PULSE GENERATOR (See Note)
SEE TEST TABLE
A
B
Cn
Σ
Cn+1
RL = 280Ω
*CL = 25 pF
≤10 ns
≤10 ns
90%
90%
1.5 V
1.5 V
10%
10%
3 V
0 V
INPUT
tPLH
tPHL
OUTPUT WAVEFORM 1
1.5 V
1.5 V
VOH
VOL
tPHL
tPLH
OUTPUT WAVEFORM 2
1.5 V
1.5 V
VOH
VOL
tPHL

*C_L inclues probe and jig capacitance.

NOTE:
The generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

TEST CIRCUIT

VOLTAGE WAVEFORMS

Fig. A – SWITCHING TIMES

TEST TABLE FOR FIG. A (EACH ADDER)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR	APPLY 3V	APPLY GND	OUTPUT UNDER TEST	OUTPUT WAVEFORM
1	t_{PLH}	A	B, C_n		Σ	1
2	t_{PHL}					
3	t_{PLH}	A	B	C_n	Σ	2
4	t_{PHL}					
5	t_{PLH}	A	C_n	B	Σ	2
6	t_{PHL}					
7	t_{PLH}	A		B, C_n	Σ	1
8	t_{PHL}					
9	t_{PLH}	A	B	C_n	C_{n+1}	1
10	t_{PHL}					
11	t_{PLH}	A	C_n	B	C_{n+1}	1
12	t_{PHL}					
13	t_{PLH}	B	A, C_n		Σ	1
14	t_{PHL}					
15	t_{PLH}	B	A	C_n	Σ	2
16	t_{PHL}					
17	t_{PLH}	B	C_n	A	Σ	2
18	t_{PHL}					
19	t_{PLH}	B		A, C_n	Σ	1
20	t_{PHL}					
21	t_{PLH}	B	A	C_n	C_{n+1}	1
22	t_{PHL}					
23	t_{PLH}	B	C_n	A	C_{n+1}	1
24	t_{PHL}					
25	t_{PLH}	C_n	A, B		Σ	1
26	t_{PHL}					
27	t_{PLH}	C_n	A	B	Σ	2
28	t_{PHL}					
29	t_{PLH}	C_n	B	A	Σ	2
30	t_{PHL}					
31	t_{PLH}	C_n		A, B	Σ	1
32	t_{PHL}					
33	t_{PLH}	C_n	A	B	C_{n+1}	1
34	t_{PHL}					
35	t_{PLH}	C_n	B	A	C_{n+1}	1
36	t_{PHL}					

TTL/MSI 93190/54190, 74190
93191/54191, 74191
UP/DOWN DECADE AND BINARY COUNTER

DESCRIPTION – The 93190/54190, 74190 and 93191/54191, 74191 are Synchronous Up/Down Counters with enable control presetting facility, single line up/down control, cascading for multi-decade operation and buffered inputs. The 93190/54190, 74190 is a BCD counter, while the 93191/54191, 74191 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when input conditions are met. This mode of operation will eliminate the output counting spikes which are normally associated with asynchronous (ripple clock) counters.

A HIGH at the enable input inhibits counting. A LOW at the enable input and a LOW-to-HIGH clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is HIGH. The down/up input determines the direction of the count. When LOW, the count goes up; when HIGH, the count goes down.

These counters are fully programmable. The outputs may be preset to any state by placing a LOW on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the state of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

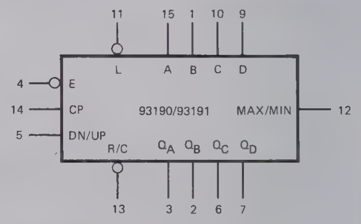
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a HIGH level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a LOW level output pulse equal in width to the LOW level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish lookahead for high speed operation.

Power dissipation is typically 325 mW for either the decade or binary version. Maximum input clock frequency is typically 25 MHz and is guaranteed to be at least 20 MHz.

PIN NAMES		LOADING
$\overline{L}$	Load Input	1 U.L.
A, B, C, D	Parallel Input	1 U.L.
$\overline{E}$	Enable Input	3 U.L.
CP	Clock Input	1 U.L.
DN/UP	Down/Up Input	1 U.L.
$\overline{R/C}$	Ripple Clock Output	10 U.L.
Q_A, Q_B, Q_C, Q_D	Parallel Output	10 U.L.
Max/Min	Max./Min. Output	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

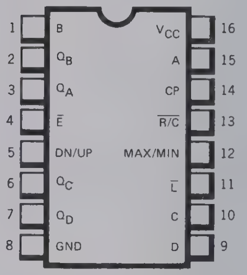
LOGIC SYMBOL



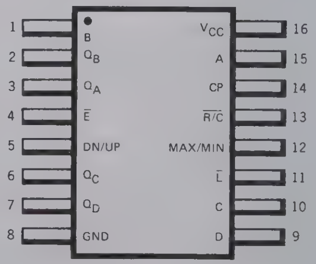
V_{CC} = Pin 16
GND = Pin 8

93190/54190, 74190
93191/54191, 74191

CONNECTION DIAGRAM
DIP (TOP VIEW)

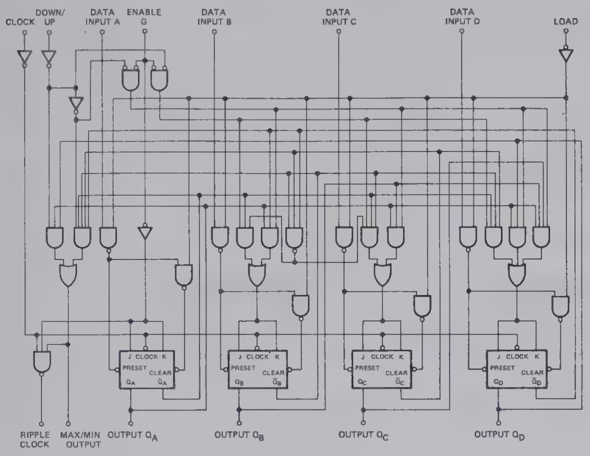


FLATPAK (TOP VIEW)

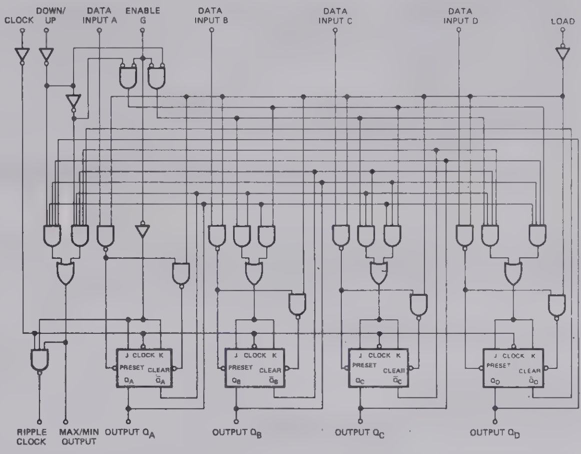


Asynchronous inputs:
LOW input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$

LOGIC DIAGRAMS

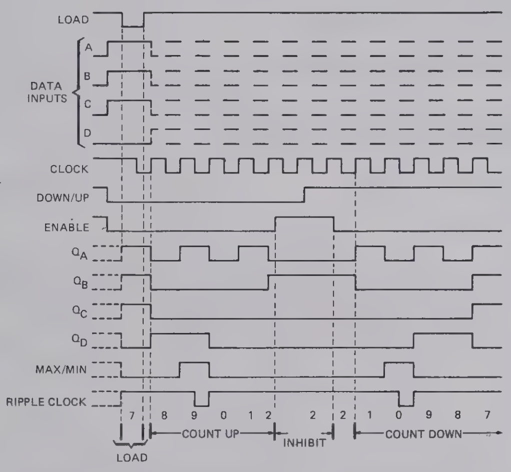

CLOCK
DOWN/UP
DATA INPUT A
ENABLE G
DATA INPUT B
DATA INPUT C
DATA INPUT D
LOAD
J CLOCK K
PRESET
CLEAR
Q_A $\bar{Q}_A$
Q_B $\bar{Q}_B$
Q_C $\bar{Q}_C$
Q_D $\bar{Q}_D$
RIPPLE CLOCK
MAX/MIN OUTPUT
OUTPUT Q_A
OUTPUT Q_B
OUTPUT Q_C
OUTPUT Q_D

DECADE COUNTER
93190/54190, 74190


CLOCK
DOWN/UP
DATA INPUT A
ENABLE G
DATA INPUT B
DATA INPUT C
DATA INPUT D
LOAD
J CLOCK K
PRESET
CLEAR
Q_A $\bar{Q}_A$
Q_B $\bar{Q}_B$
Q_C $\bar{Q}_C$
Q_D $\bar{Q}_D$
RIPPLE CLOCK
MAX/MIN OUTPUT
OUTPUT Q_A
OUTPUT Q_B
OUTPUT Q_C
OUTPUT Q_D

BINARY COUNTER
93191/54191, 74191

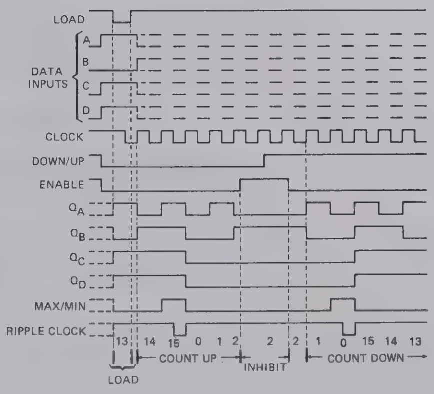
TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCE


LOAD
DATA INPUTS
A
B
C
D
CLOCK
DOWN/UP
ENABLE
Q_A
Q_B
Q_C
Q_D
MAX/MIN
RIPPLE CLOCK
7
8
9
0
1
2
2
2
1
0
9
8
7
COUNT UP
INHIBIT
COUNT DOWN
LOAD

The following sequence is illustrated:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

DECADE COUNTER
93190/54190, 74190


LOAD
DATA INPUTS
A
B
C
D
CLOCK
DOWN/UP
ENABLE
Q_A
Q_B
Q_C
Q_D
MAX/MIN
RIPPLE CLOCK
13
14
15
0
1
2
2
2
1
0
15
14
13
COUNT UP
INHIBIT
COUNT DOWN
LOAD

The following sequence is illustrated:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

BINARY COUNTER
93191/54191, 74191

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93190XM/54190XM 93191XM/54191XM			93190XC/74190XC 93191XC/74191XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	
Input Clock Frequency, f_{clock}		0		20	0		20	MHz
Width of Clock Input Pulse, $t_{w(clock)}$		25			25			ns
Width of Load Input Pulse, $t_{w(load)}$		35			35			ns
Data Setup Time, t_{setup} (See Fig. 1 and 2)		20			20			ns
Data Hold Time, t_{hold}		0			0			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Threshold Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Threshold Voltage	
V_{CD}	Input Clamp Diode Voltage				−1.5	Volts	V_{CC} = MIN., $I_{IN} = -12mA$	
V_{OH}	Output HIGH Voltage		2.4			Volts	V_{CC} = MIN., $I_{OH} = -800\ \mu A$, $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V	
V_{OL}	Output LOW Voltage				0.4	Volts	V_{CC} = MIN., $I_{OL} = 16$ mA, $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V	
I_I	Input Current at Max Input Voltage				1.0	mA	V_{CC} = MAX., $V_{IN} = 5.5$ V	
I_{IH}	Input HIGH Current	Other Inputs			40	μA	V_{CC} = MAX., $V_{IN} = 2.4$ V	
		Enable Input			120			
I_{IL}	Input LOW Current	Other Inputs			−1.6	mA	V_{CC} = MAX., $V_{IN} = 0.4$ V	
		Enable Input			−4.8			
I_{OS}	Output Short Circuit Current (Note 3)		−20		−65	mA	93190/54190; 93191/54191	V_{CC} = MAX.
			−18		−65		93190/74190; 93191/74191	
I_{CC}	Supply Current (Note 4)			65	105	mA	V_{CC} = MAX.	

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

(2) Typical limits are at $V_{CC} = 5.0$ V, 25°C.

(3) Not more than one output should be shorted at a time.

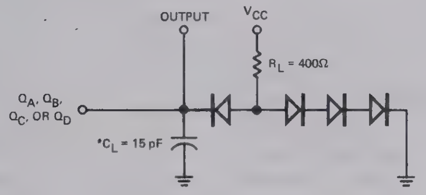
(4) I_{CC} is measured with all inputs grounded and all outputs open.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	A TEST CONDITIONS
f_{max}	Max. Input Clock Frequency	20	25		MHz	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 400\Omega$ (See Fig. 1 and Fig. 3 thru 7)
t_{PLH} t_{PHL}	Load Input to Q_A, Q_B, Q_C, Q_D Output		22 33	33 50	ns	
t_{PLH} t_{PHL}	Data Input A, B, C, D, to Q_A, Q_B, Q_C, Q_D Output		14 35	22 50	ns	
t_{PLH} t_{PHL}	Clock Input to Ripple Clock Output		13 16	20 24	ns	
t_{PLH} t_{PHL}	Clock Input to Q_A, Q_B, Q_C, Q_D Output		16 24	24 36	ns	
t_{PLH} t_{PHL}	Clock Input to Max./Min. Output		28 37	42 52	ns	
t_{PLH} t_{PHL}	Down/Up Input to Ripple Clock Output		30 30	45 45	ns	
t_{PLH} t_{PHL}	Down/Up Input to Max./Min. Output		21 22	33 33	ns	

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS


OUTPUT
V_{CC}
$R_L = 400\Omega$
Q_A, Q_B, Q_C, OR Q_D
$^*C_L = 15$ pF

*C_L includes probe & jig capacitance.

Fig. 1 — LOAD CIRCUIT FOR SWITCHING TIME MEASUREMENT

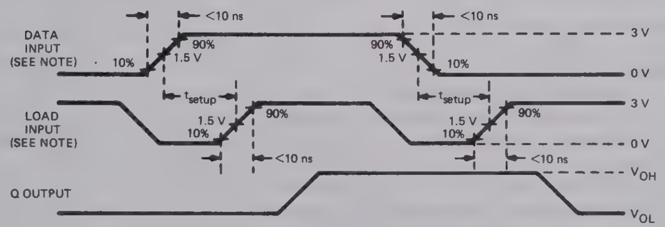
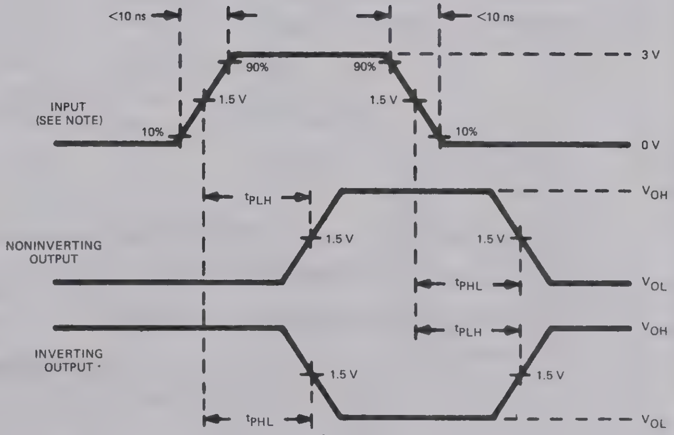

<10 ns
<10 ns
DATA INPUT (SEE NOTE)
10%
90%
1.5 V
90%
1.5 V
10%
3 V
0 V
LOAD INPUT (SEE NOTE)
t_{setup}
1.5 V
10%
90%
t_{setup}
1.5 V
10%
90%
3 V
0 V
<10 ns
<10 ns
Q OUTPUT
V_{OH}
V_{OL}

Fig. 2 — SETUP TIME VOLTAGE WAVEFORMS


<10 ns
<10 ns
3 V
90%
90%
INPUT (SEE NOTE)
1.5 V
1.5 V
10%
10%
0 V
t_{PLH}
V_{OH}
NONINVERTING OUTPUT
1.5 V
1.5 V
t_{PHL}
V_{OL}
t_{PLH}
V_{OH}
INVERTING OUTPUT
1.5 V
1.5 V
t_{PHL}
V_{OL}

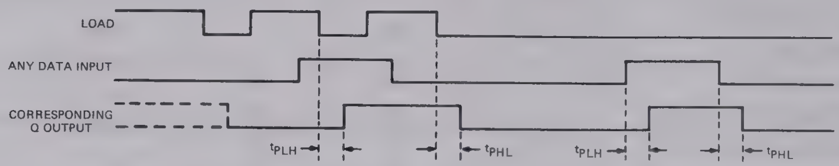
See waveform sequences in Figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in Figures 4 through 7.

Fig. 3 — GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTE:
The input pulses are supplied by generators having the following characteristics: $Z_{out} = 50\Omega$, duty cycle ≤ 50%, PRR ≤ 1 MHz.

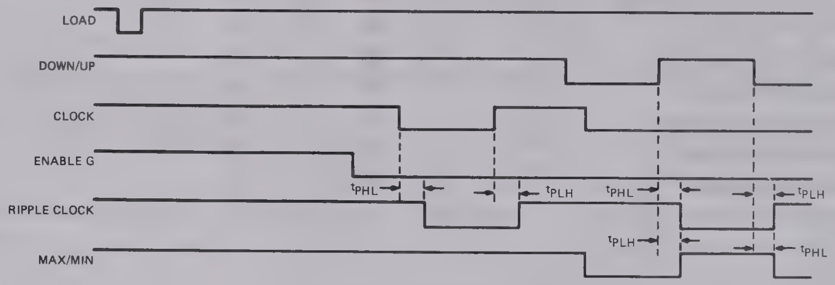
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (cont'd)


LOAD
ANY DATA INPUT
CORRESPONDING Q OUTPUT
t_{PLH}
t_{PHL}
t_{PLH}
t_{PHL}

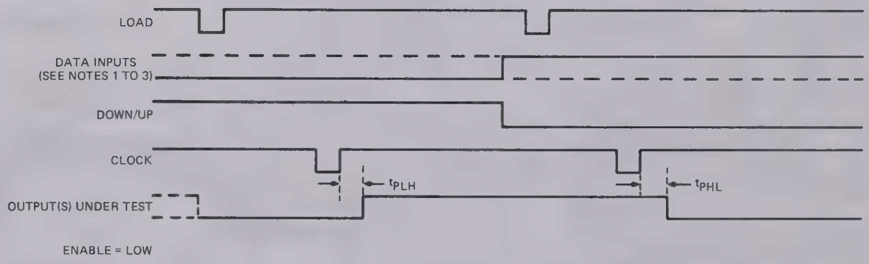
NOTE: Conditions on other inputs are irrelevant.

Fig. 4 – LOAD TO OUTPUT AND DATA TO OUTPUT


LOAD
DOWN/UP
CLOCK
ENABLE G
RIPPLE CLOCK
MAX/MIN
t_{PHL}
t_{PLH}
t_{PHL}
t_{PLH}
t_{PLH}
t_{PHL}

NOTE: All data inputs are LOW.

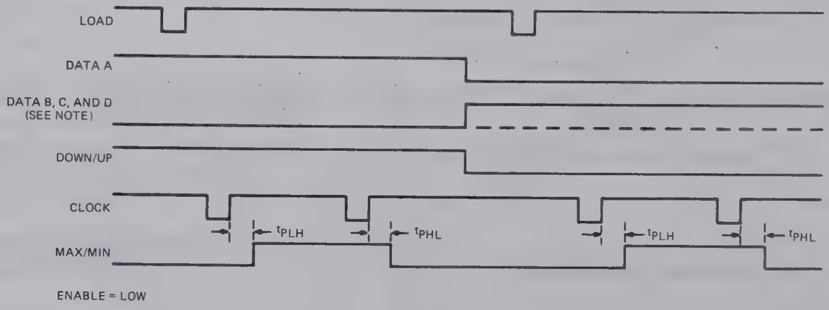
Fig. 5 – ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN


LOAD
DATA INPUTS (SEE NOTES 1 TO 3)
DOWN/UP
CLOCK
OUTPUT(S) UNDER TEST
t_{PLH}
t_{PHL}
ENABLE = LOW

NOTES:

1. To test Q_A, Q_B, and Q_C outputs of 93190/54190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
2. To test Q_D output of 93190/54190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the LOW logic level.
3. To test Q_A, Q_B, Q_C, and Q_D outputs of 93191/54191: All four data inputs are shown by the solid line.

Fig. 6 – CLOCK TO OUTPUT


LOAD
DATA A
DATA B, C, AND D (SEE NOTE)
DOWN/UP
CLOCK
MAX/MIN
t_{PLH}
t_{PHL}
t_{PLH}
t_{PHL}
ENABLE = LOW

NOTE: Data inputs B and C are shown by the dashed line for 93190/54190 and the solid line for 93191/54191. Data input D is shown by the solid line for both devices.

Fig. 7 – CLOCK TO MAX/MIN

TTL/MSI 93196/54196, 74196
93197/54197, 74197
HIGH SPEED DECADE AND BINARY COUNTER

TO BE ANNOUNCED

DESCRIPTION — The 93196/54196, 74196 and 93197/54197, 74197 High Speed Counters will provide either a divide-by-two and a divide-by-five counter (93196/54196, 74196) or a divide-by-two and a divide-by-eight counter (93197/54197, 74197). The counters are fully presettable to any output state by placing a LOW on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is LOW, but will remain unchanged when the count/load is HIGH and the clock inputs are inactive.

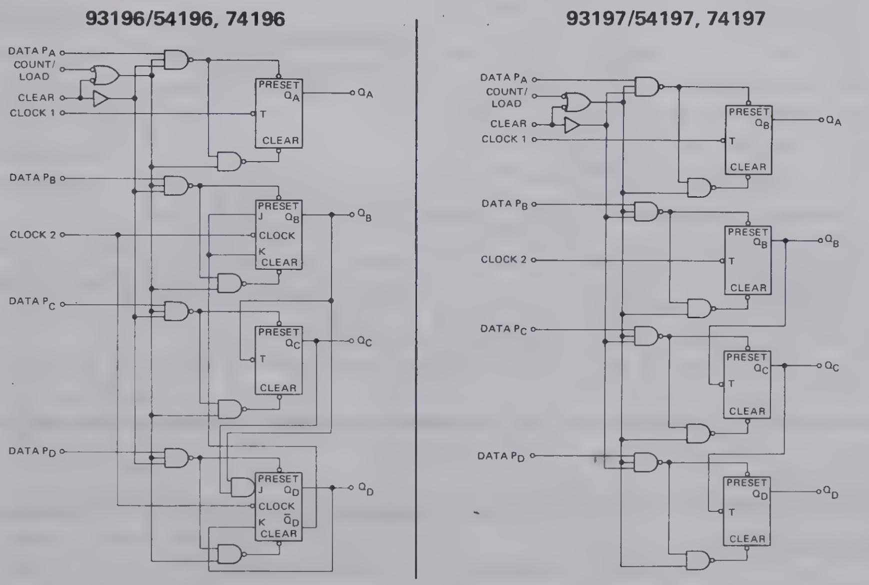
These high speed counters will accept count frequencies of 0 to 50 MHz at the clock 1 input and 0 to 25 MHz at the clock 2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken LOW, sets all outputs LOW regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Typical power dissipation is 240 mW.

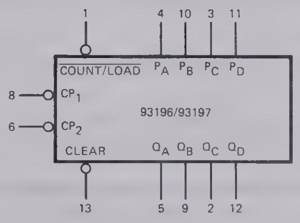
PIN NAMES		LOADING (Note a)
P_A, P_B, P_C, P_D	Parallel Inputs	1 U.L.
$\overline{CP}_1$, $\overline{CP}_2$	Clock Inputs (Note b)	2 U.L.
$\overline{CLEAR}$	Clear Input	2 U.L.
$\overline{COUNT/LOAD}$	Count Load Input	1 U.L.
Q_A, Q_B, Q_C, Q_D	Parallel Outputs	10 U.L.

NOTES:
(a) 1 U.L. = 40 μA HIGH/1.6 mA LOW
(b) $\overline{CP}_2$ — 3 U.L. on 93196

LOGIC DIAGRAM

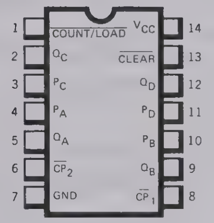

93196/54196, 74196
93197/54197, 74197
DATA PA
COUNT/LOAD
CLEAR
CLOCK 1
DATA PB
CLOCK 2
DATA PC
DATA PD
PRESET
CLEAR
T
J
K
CLOCK
QA
QB
QC
QD

LOGIC SYMBOL

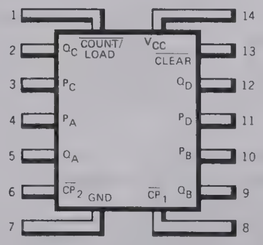

1
4
10
3
11
COUNT/LOAD
PA
PB
PC
PD
8
CP1
93196/93197
6
CP2
CLEAR
QA
QB
QC
QD
13
5
9
2
12

V_{CC} = Pin 14
Gnd = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)


1
2
3
4
5
6
7
14
13
12
11
10
9
8
COUNT/LOAD
VCC
QC
CLEAR
PC
QD
PA
PD
QA
PB
CP2
QB
GND
CP1

FLATPAK (TOP VIEW)


1
2
3
4
5
6
7
14
13
12
11
10
9
8
QC
COUNT/LOAD
VCC
CLEAR
PC
QD
PA
PD
QA
PB
CP2
GND
CP1
QB

Asynchronous input: LOW input to clear sets Q_A, Q_B, Q_C and Q_D LOW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93196XM/54196XM 93197XM/54197XM MIN.	TYP.	MAX.	93196XC/74196XC 93197XC/74197XC MIN.	TYP.	MAX.	UNITS
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N HIGH Logic/LOW Logic				20/10			20/10	U.L.
Count Frequency (See Fig. 1) $\overline{CP}_1/\overline{CP}_2$		0/0		50/25	0/0		50/25	MHz
Pulse Width, t_w (See Fig. 1)	$\overline{CP}_1/\overline{CP}_2$	10/20			10/20			ns
	$\overline{\text{Clear}}$/Load	15/20			15/20			
Input Hold Time, t_{hold} (See Fig. 1)	HIGH & LOW Level Data	tw (Load)			tw (Load)			ns
Input Setup Time, t_{setup} (See Fig. 1)	HIGH Data/LOW Data	10/15			10/15			ns
Count Enable Time, t_{enable}* (See Fig. 1)		20			20			ns
Clock Input Pulse Fall Time t_f (See Fig. 1)				75			75	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

*Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must be both HIGH to ensure counting.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	TYP. (Note 2)	MAX.	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage				−1.5	Volts	V_{CC} = MAX., I_{IN} = −12 mA	
V_{OH}	Output HIGH Voltage		2.4			Volts	V_{CC} = MIN., I_{OH} = −800 µA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
V_{OL}	Output LOW Voltage				0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, (Note 4) V_{IH} = 2.0 V, V_{IL} = 0.8 V	
I_I	Input Current at Max. Input Voltage				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current	Data, Count/$\overline{\text{Load}}$			40	µA		V_{CC} = MAX. V_{IN} = 2.4 V
		$\overline{\text{Clear}}$, $\overline{CP}_1$			80	µA		
		$\overline{CP}_2$			120	µA	93196/54196, 74196	
					80	µA	93197/54197, 74197	
I_{IL}	Input LOW Current	Data, Count/$\overline{\text{Load}}$			−1.6	mA		V_{CC} = MAX. V_{IN} = 0.4 V
		$\overline{\text{Clear}}$			−3.2	mA		
		$\overline{CP}_1$			−4.8	mA		
		$\overline{CP}_2$			−6.4	mA	93196/54196, 74196	
					−3.2	mA	93197/54197, 74197	
I_{OS}	Output Short Circuit Current (Note 3)		−20		−57	mA	93196/54196, 93197/54197	V_{CC} = MAX.
			−18		−57	mA	93196/74196, 93197/74197	
I_{CC}	Supply Current (Note 5)			48	59	mA	V_{CC} = MAX.	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock 2 input. This permits driving the clock 2 input while fanning out to 10 Series 54/74 loads.
(5) I_{CC} is measured with all inputs grounded and all outputs open.

TYPICAL COUNT CONFIGURATIONS

93196/54196, 74196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock 2 input must be externally connected to the Q_A output. The clock 1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown at the right.
2. If a symmetrical divide-by-ten count is desired for any application requiring division of a binary count by a power of ten, the Q_D output must be externally connected to the clock 1 input. The input count is then applied at the clock 2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table shown at the right.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock 2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

93196/54196, 74196
TRUTH TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES:
A. Output Q_A connected to clock 2 input.
B. Output Q_D connected to clock 1 input.

93197/54197, 74197

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high speed 4-bit ripple counter, output Q_A must be externally connected to the clock 2 input. The input count pulses are applied to the clock 1 input. Simultaneous divisions by 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C, Q_D output as shown in the truth table at the right.
2. When used as a 3-bit ripple counter, the input count pulses are applied to the clock 2 input. Simultaneous frequency divisions by 2, 4 and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple counter.

93197/54197, 74197
TRUTH TABLE

(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE:
A. Output Q_A connected to clock 2 input.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

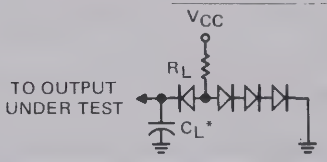
Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

SWITCHING CHARACTERISTICS (T_A = 25°C) (see Fig. 1)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
f_{MAX}	(MAX. Input Count Frequency)	50	70		MHz		V_{CC} = 5 V R_L = 400 Ω C_L = 15 pF
t_{PLH}	$\overline{\text{Clock 1}}$ Input to Q_A Output		7.0	12	ns		
t_{PHL}			10	15			
t_{PLH}	$\overline{\text{Clock 2}}$ Input to Q_B Output		12	18	ns		
t_{PHL}			14	21			
t_{PLH}	$\overline{\text{Clock 2}}$ Input to Q_C Output		24	36	ns		
t_{PHL}			28	42			
t_{PLH}	$\overline{\text{Clock 2}}$ Input to Q_D Output		14	21	ns	93196/54196, 74196	
			36	54	ns	93197/54197, 74197	
t_{PHL}			12	18	ns	93196/54196, 74196	
			42	63	ns	93197/54197, 74197	
t_{PLH}	A, B, C, D Inputs to Q_A, Q_B, Q_C, Q_D Outputs		16	24	ns		
t_{PHL}			25	38			
t_{PLH}	Load Input to Any Output		22	33	ns		
t_{PHL}			24	36			
t_{PHL}	$\overline{\text{Clear}}$ Input to Any Output		25	37	ns		

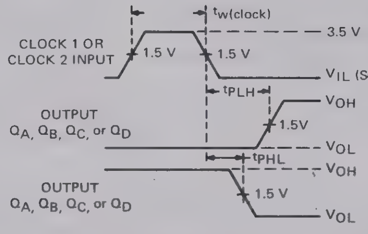
PARAMETER MEASUREMENT INFORMATION



V_{CC}
R_L
TO OUTPUT UNDER TEST
C_L*

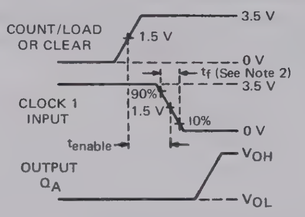
*C_L includes probe and jig capacitance.

LOAD CIRCUIT



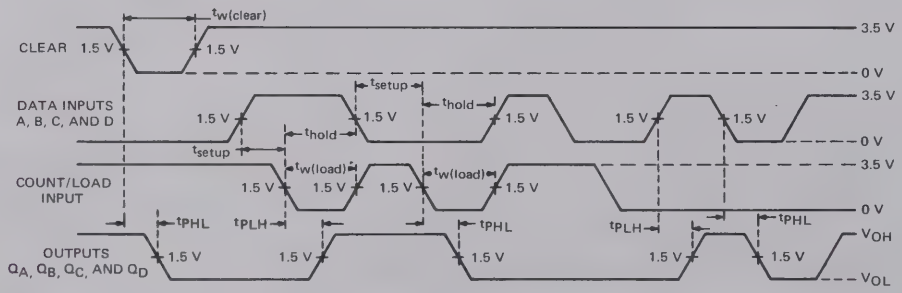
$t_{w(clock)}$
3.5 V
CLOCK 1 OR CLOCK 2 INPUT
1.5 V
1.5 V
V_{IL} (See Note 1)
t_{PLH}
V_{OH}
OUTPUT Q_A, Q_B, Q_C, or Q_D
1.5 V
V_{OL}
t_{PHL}
V_{OH}
OUTPUT Q_A, Q_B, Q_C, or Q_D
1.5 V
V_{OL}

CLOCK-MODE VOLTAGE WAVEFORMS



COUNT/LOAD OR CLEAR
1.5 V
3.5 V
0 V
t_f (See Note 2)
3.5 V
CLOCK 1 INPUT
90%
1.5 V
10%
0 V
t_{enable}
OUTPUT Q_A
V_{OH}
V_{OL}

CLOCK ENABLE TIME VOLTAGE WAVEFORMS



$t_{w(clear)}$
CLEAR 1.5 V
1.5 V
3.5 V
0 V
t_{setup}
t_{hold}
DATA INPUTS A, B, C, AND D
1.5 V
1.5 V
1.5 V
1.5 V
1.5 V
3.5 V
0 V
t_{hold}
t_{setup}
$t_{w(load)}$
$t_{w(load)}$
COUNT/LOAD INPUT
1.5 V
1.5 V
1.5 V
1.5 V
3.5 V
0 V
t_{PHL}
t_{PLH}
t_{PHL}
t_{PLH}
t_{PHL}
OUTPUTS Q_A, Q_B, Q_C, AND Q_D
1.5 V
1.5 V
1.5 V
1.5 V
1.5 V
V_{OH}
V_{OL}

CLEAR AND LOAD VOLTAGE WAVEFORMS

NOTES:

1. The input pulse generator has the following characteristics: for testing f_{max}, V_{IL} = 0.3 ± 0.1 V, duty cycle = 50%, $t_r < 5$ ns, and $t_f < 5$ ns; for all other measurements V_{IL} = 0, PRR ⩽ 1 MHz, duty cycle ⩽ 50%, $t_r < 5$ ns, and unless otherwise specified, $t_f < 5$ ns.
2. Fall time of clock 1 is measured with count/load and clear high. When measuring clock enable time, $t_f < 5$ ns.
3. Unless otherwise specified, Q_A is connected to Clock 2.

Fig. 1

TTL/MSI 93198/54198, 74198

8-BIT SHIFT REGISTER

TO BE ANNOUNCED

DESCRIPTION — The 93198/54198, 74198 are Bidirectional Registers that are designed to incorporate virtually all of the features a system designer may want in a shift register. The 93198/54198, 74198 feature 35 MHz shift frequency, parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating mode-control inputs and a direct overriding clear line. The register has four distinct modes of operation: (1) parallel (broadside) load, (2) shift right (in the direction Q_A toward Q_H), (3) shift left (in the direction Q_H toward Q_A), (4) inhibit clock (do nothing).

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S_0 and S_1, HIGH. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is HIGH and S_1 is LOW. Serial data for this mode is entered at the shift-right data input. When S_0 is LOW and S_1 is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW. The mode controls should be changed only while the clock input is HIGH.

Typical power dissipation is 360 mW and all inputs are diode-clamped.

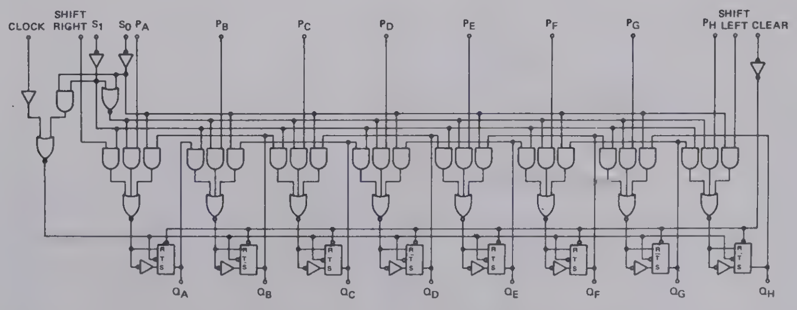
PIN NAMES		LOADING
P_A to P_H	Parallel Data Inputs	1 U.L.
S_0, S_1	Mode Control Inputs	1 U.L.
L	Shift Left Serial Input	1 U.L.
R	Shift Right Serial Input	1 U.L.
CP	Clock (Active HIGH Going Edge) Input	1 U.L.
$\overline{CL}$	Clear (Active LOW) Input	1 U.L.
Q_A to Q_H	Data Outputs	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

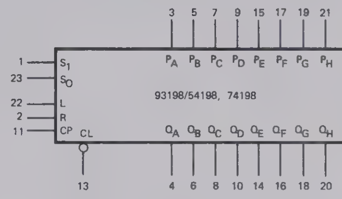
TRUTH TABLE OPERATION OF MODE CONTROL

INPUTS		MODE
S_1	S_0	
L	L	INHIBIT CLOCK
L	H	SHIFT RIGHT
H	L	SHIFT LEFT
H	H	PARALLEL LOAD

LOGIC DIAGRAM

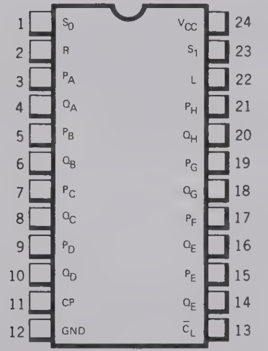

CLOCK
SHIFT RIGHT
S_1
S_0
P_A
P_B
P_C
P_D
P_E
P_F
P_G
P_H
SHIFT LEFT
CLEAR
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
Q_H

LOGIC SYMBOL

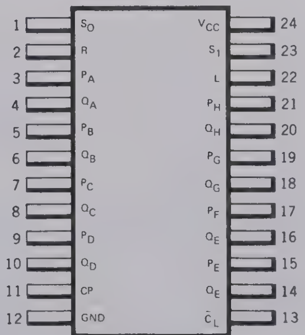

3 5 7 9 15 17 19 21
P_A P_B P_C P_D P_E P_F P_G P_H
1 S_1
23 S_0
22 L
2 R
11 CP CL
93198/54198, 74198
Q_A Q_B Q_C Q_D Q_E Q_F Q_G Q_H
13
4 6 8 10 14 16 18 20

V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 S_0
2 R
3 P_A
4 Q_A
5 P_B
6 Q_B
7 P_C
8 Q_C
9 P_D
10 Q_D
11 CP
12 GND
24 V_{CC}
23 S_1
22 L
21 P_H
20 Q_H
19 P_G
18 Q_G
17 P_F
16 Q_F
15 P_E
14 Q_E
13 $\overline{C}_L$

FLATPAK (TOP VIEW)


1 S_0
2 R
3 P_A
4 Q_A
5 P_B
6 Q_B
7 P_C
8 Q_C
9 P_D
10 Q_D
11 CP
12 GND
24 V_{CC}
23 S_1
22 L
21 P_H
20 Q_H
19 P_G
18 Q_G
17 P_F
16 Q_E
15 P_E
14 Q_E
13 $\overline{C}_L$

Positive logic: See truth table for mode control (S_0, S_1)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to $+V_{CC}$ value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93198XM/54198XM			93198XC/74198XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	
Input Count Frequency, f_{count}		0		25	0		25	MHz
Width of Clock or Clear Pulse, t_W (See Fig. 1)		20			20			ns
Mode-Control Setup Time, t_{setup}		30			30			ns
Data Setup Time, t_{setup} (See Fig. 1)		20			20			ns
Hold Time at Any Input, t_{hold} (See Fig. 1)		0			0			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

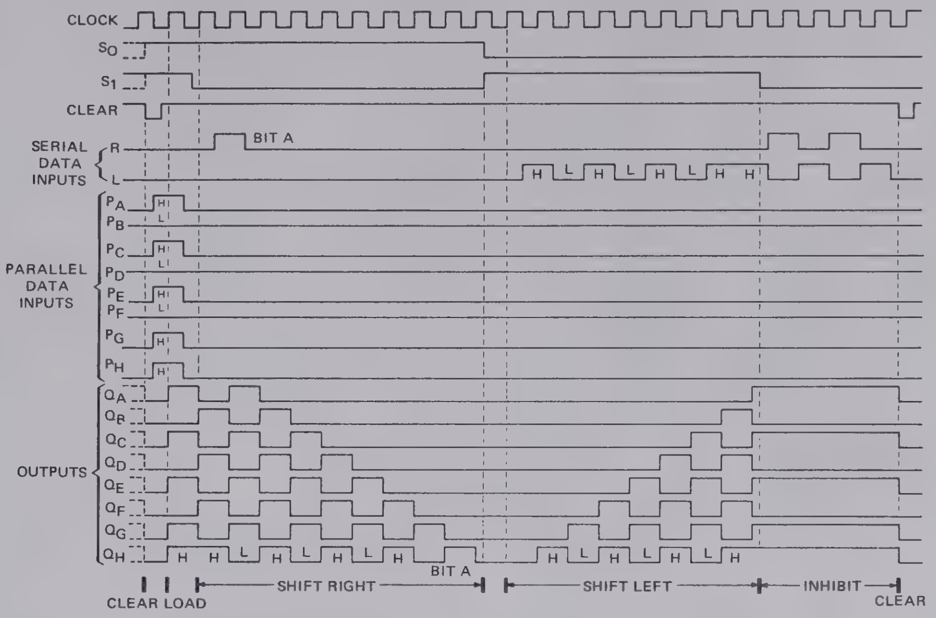
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MAX., I_{IN} = −12 mA	
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −800 µA, V_{IH} = 2.0 V, VIL = 0.8 V	
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
I_I	Input Current at MAX. Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	93198/54198	V_{CC} = MAX.
		−18		−57	mA	93198/74198	
I_{CC}	Supply Current		72	104	mA	93198/54198	V_{CC} = MAX., S_0, S_1 = 4.5 V CP = Momentary GND then 4.5 V $\overline{CL}$, P_A to P_H = GND All Outputs are Open
			72	116	mA	93198/74198	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{MAX}	Maximum Input Count Frequency	25	35		MHz	
t_{PHL}	Turn On Delay Clear to Output		23	35	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400 Ω (see Fig. 1)
t_{PLH}	Turn Off Delay Clock to Output	8	17	26	ns	
t_{PHL}	Turn On Delay Clock to Output	8	20	30	ns	

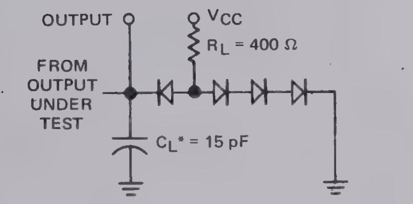
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES


CLOCK
S_0
S_1
CLEAR
SERIAL DATA INPUTS
R
L
BIT A
H L H L H L H H
PARALLEL DATA INPUTS
P_A
P_B
P_C
P_D
P_E
P_F
P_G
P_H
H
L
OUTPUTS
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
Q_H
H H L H L H L H
BIT A
H L H L H L H
CLEAR LOAD
SHIFT RIGHT
SHIFT LEFT
INHIBIT
CLEAR

SWITCHING PARAMETER MEASUREMENT INFORMATION

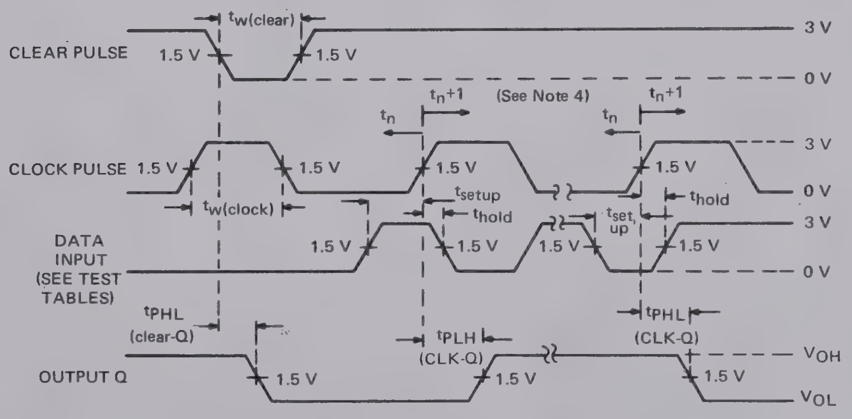
LOAD FOR OUTPUT UNDER TEST


OUTPUT
V_{CC}
R_L = 400 Ω
FROM OUTPUT UNDER TEST
C_L* = 15 pF

*C_L includes probe and jig capacitance.

TEST TABLE FOR SYNCHRONOUS INPUTS

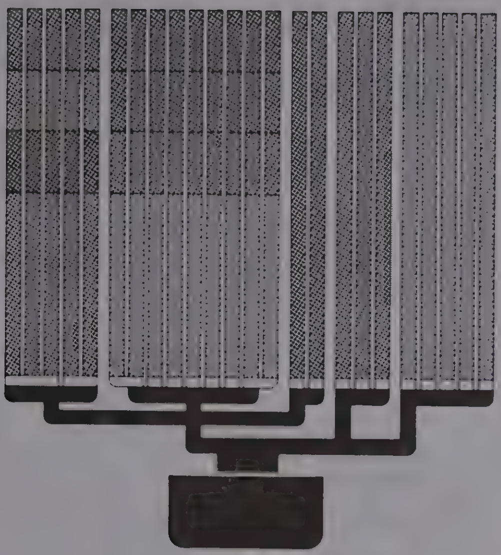
DATA INPUT FOR TEST	S_1	S_0	OUTPUT TESTED (SEE NOTE 3)
P_A	4.5 V	4.5 V	Q_A at t_n+1
P_B	4.5 V	4.5 V	Q_B at t_n+1
P_C	4.5 V	4.5 V	Q_C at t_n+1
P_D	4.5 V	4.5 V	Q_D at t_n+1
P_E	4.5 V	4.5 V	Q_E at t_n+1
P_F	4.5 V	4.5 V	Q_F at t_n+1
P_G	4.5 V	4.5 V	Q_G at t_n+1
P_H	4.5 V	4.5 V	Q_H at t_n+1
L Serial Input	4.5 V	0 V	Q_A at t_n+8
R Serial Input	0 V	4.5 V	Q_H at t_n+8


$t_{w(clear)}$
CLEAR PULSE
1.5 V
1.5 V
3 V
0 V
t_n+1
(See Note 4)
t_n+1
t_n
t_n
CLOCK PULSE
1.5 V
1.5 V
1.5 V
1.5 V
3 V
0 V
$t_{w(clock)}$
t_{setup}
t_{hold}
t_{hold}
$t_{set, up}$
DATA INPUT (SEE TEST TABLES)
1.5 V
1.5 V
1.5 V
1.5 V
3 V
0 V
t_{PHL} (clear-Q)
t_{PLH} (CLK-Q)
t_{PHL} (CLK-Q)
OUTPUT Q
1.5 V
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS

NOTES:
1. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{hold} = 0$ ns. When testing f_{MAX}, vary the clock PRR.
2. A clear pulse is applied prior to each test.
3. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+8 with a functional test.
4. t_n = bit time before clocking transition
   t_n+1 = bit time after one clocking transition
   t_n+8 = bit time after eight clocking transitions

Fig. 1



Memory — 93400 Data Sheets

TTL MEMORY 93400 • 93400B • 93401

256-BIT READ/WRITE MEMORY & DECODER/DRIVER

FORMERLY 4100 • 4100B • 4101

DESCRIPTION – The 93400 256-Bit Read/Write Memory and the 93401 Decoder/Driver are components for use in high speed memory systems. The 93400 is a fast 256 x 1 random access read/write memory which is addressed with a partially decoded x-y coincident selection scheme. There are two device grades, with the 93400B having a slower access time than the 93400. The companion decoder and buffer driver, 93401, converts binary addresses into the partially decoded form required by the 93400, and provides sufficient drive to connect to 32 93400's. Both devices are supplied in 16-lead Dual In-Line Packages.

93400/93400B

- TTL COMPATIBLE
- 16-LEAD PACKAGE
- OUTPUT WIRED–OR CAPABILITY
- 70 ns TYPICAL ACCESS TIME (93400)
- 125 ns TYPICAL ACCESS TIME (93400B)
- LOW INPUT LOADING

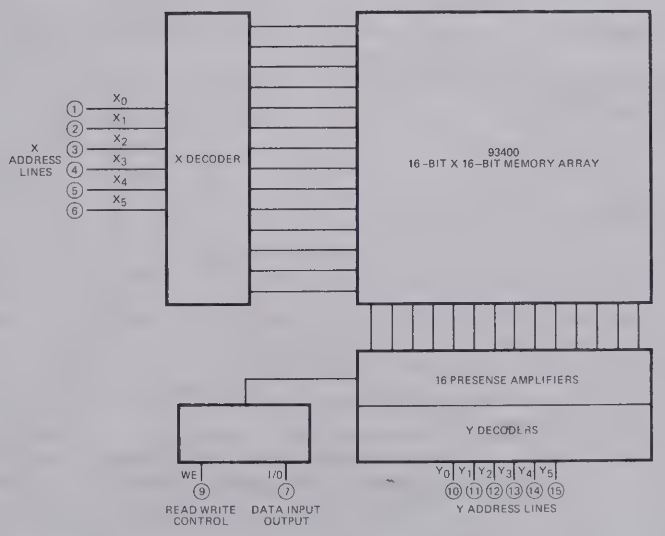
93401

- TTL COMPATIBLE
- 16-LEAD PACKAGE
- 20 ns TYPICAL THROUGH DELAY
- LOW INPUT LOADING
- 4 ENABLE INPUTS FOR CHIP SELECTION
- DRIVES UP TO 32 93400's

ABSOLUTE MAXIMUM RATINGS

V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
Input Voltage	–0.5 V to +5.25 V
Voltage Applied to Output when Output is HIGH	–0.5 V to $+V_{CC}$
Current into Output when Output is LOW	+25 mA
Storage Temperature	–65°C to +150°C

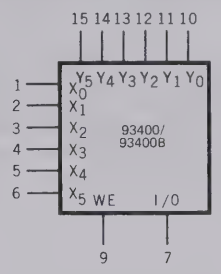
LOGIC DIAGRAM



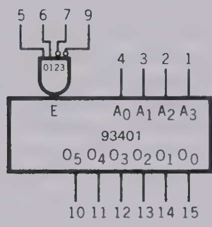
X ADDRESS LINES
①
②
③
④
⑤
⑥
x_0
x_1
x_2
x_3
x_4
x_5
X DECODER
93400
16-BIT X 16-BIT MEMORY ARRAY
16 PRESENSE AMPLIFIERS
Y DECODERS
WE
⑨
READ WRITE CONTROL
I/0
⑦
DATA INPUT OUTPUT
Y_0 Y_1 Y_2 Y_3 Y_4 Y_5
⑩ ⑪ ⑫ ⑬ ⑭ ⑮
Y ADDRESS LINES

○ = PIN NUMBERS

LOGIC SYMBOLS



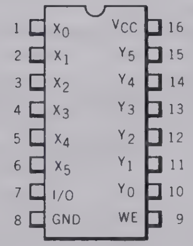
15 14 13 12 11 10
Y_5 Y_4 Y_3 Y_2 Y_1 Y_0
1 X_0
2 X_1
3 X_2
4 X_3
5 X_4
6 X_5
93400/
93400B
WE
I/0
9
7



5 6 7 9
0123
4 3 2 1
E
A_0 A_1 A_2 A_3
93401
O_5 O_4 O_3 O_2 O_1 O_0
10 11 12 13 14 15

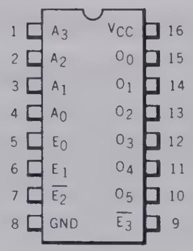
V_{CC} = Pin 16
Gnd = Pin 8

CONNECTION DIAGRAMS
(TOP VIEWS)
93400/93400B



1 X_0
2 X_1
3 X_2
4 X_3
5 X_4
6 X_5
7 I/0
8 GND
V_{CC} 16
Y_5 15
Y_4 14
Y_3 13
Y_2 12
Y_1 11
Y_0 10
WE 9

93401



1 A_3
2 A_2
3 A_1
4 A_0
5 E_0
6 E_1
7 $\overline{E_2}$
8 GND
V_{CC} 16
O_0 15
O_1 14
O_2 13
O_3 12
O_4 11
O_5 10
$\overline{E_3}$ 9

FUNCTIONAL DESCRIPTIONS

The 93400 and 93400B contain 256 bipolar storage cells arranged in a 16 by 16 format. Any one of the 256 cells may be accessed by supplying an address code on the X address inputs and the Y address inputs. Internal decoders decode the X and Y addresses into one of 16 rows and one of 16 columns in the matrix of storage cells. Data may be written into or read out from the cell lying at the intersection of the selected row and column.

The X and Y addresses supplied to the 93400 and 93400B are partially decoded in a "3 of 6" code. Of the six X address lines and the six Y address lines there are always three lines HIGH and three lines LOW. There are 20 such combinations, 16 are decoded by the internal row and column decoders. The four unused combinations of 3 of 6 will not select any row or column. If there are more than three lines HIGH in either the X or Y address, then multiple row or column selection will occur. The sixteen 3 of 6 codes used by the 93400 and 93400B are generated by the 93401 decoder/driver.

Data enters and leaves the memory on a single input/output (I/O) line (pin 7). The I/O line is an open collector output, so many 93400 I/O lines can be connected together in a wired-OR configuration. Input data must be applied to the I/O lines through an open collector gate. Each I/O line requires a pull-up resistor to V_{CC}. The magnitude of the pull-up resistor is determined by the number of 93400 I/O lines tied together. The I/O of a 93400 which is not addressed will be HIGH.

Read/Write selection is determined by the state of pin 9, the active HIGH write enable. When WE is HIGH, the data on the I/O line will be written into the selected address in the 93400. When the Write Enable line is LOW, data will be read out of the addressed location.

The 93401 is a partial decoder and driver for the 93400. It accepts a 4-bit binary code on the address inputs (A_0—A_3) and produces a 3 of 6 code on the six output pins (O_0—O_5). The decoder also features four separate enables, two active HIGH and two active LOW. All four enables must be active before the decoder will produce a 3 of 6 code. Since two of the enables are HIGH and two are LOW, it is possible to route two binary coded lines to four different 93401's to get two additional bits of decoding with no extra packages.

Ordinarily in memory systems, 93400 memory devices will be arranged in a matrix of rows and columns. Each column will store a particular bit and each row of 93400's will be 256 words. A 93401 driver will be used for each row and each column in the matrix. One 93401 can drive up to 32 93400 X or Y address lines. The usual driving scheme is to connect the four LSB's of address to each of the column decoders. The next four bits of address are connected to each of the row decoders. Additional address bits are decoded to the chip selects on the row decoders. Each column decoder drives the Y address lines on up to 32 93400's in a column. Each row decoder drives the address lines on up to 32 93400's in a row.

THE THREE OF SIX CODE

The "3 of 6" code used in the 93400 and produced by the 93401 is a tradeoff between memory chip complexity and pin count. The simplest 256-bit memory chip would be a 16 by 16 matrix of storage cells, with all 16 rows and 16 column select lines brought off chip. The lowest pin count for a 256-bit memory chip would be achieved by fully decoded X and Y select lines reducing the 32 lines of the simple scheme to only 8 lines. However, full binary decoding of the X and Y lines on chip significantly increases to complexity of the memory chip. The 93400 and 93401 are designed to gain the good features of both alternatives. The 16 X and Y lines are decoded into 6 lines each, allowing the memory to fit into a 16-lead package and still keeping the memory chip fairly simple, since the 3 of 6 code does not require a complex decoder. The table on the right below shows the conversion of 4-bit binary to 3 of 6 code by the 93401, and also the internal column or row selected by the 3 of 6 to 1 of 16 decoder inside the 93400.

TTL LOAD AND DRIVE FACTORS

93400 • 93400B

INPUT	LOAD
X Lines Y Lines WE	0.33/0.125
OUTPUT	**DRIVE FACTOR**
Output I/O	Open Collector 3.1

93401

INPUT	LOAD
E_0, E_1 E_2, E_3 A_0, A_1, A_2, A_3	0.33/0.25
OUTPUT	**DRIVE FACTOR**
$O_0, O_1,$ O_2, O_3, O_4, O_5	16/6

Numerator = HIGH level load
(1 load = 0.06 mA)
Denominator = LOW level load
(1 load = 1.6 mA)

CODE CONVERSION EQUATIONS

$$O_0 = \overline{A_3}$$

$$O_1 = \overline{(A_1 + A_0)\,(\overline{A_3} + A_1)\,(\overline{A_2} + A_0)}$$

$$O_2 = \overline{(A_1 + \overline{A_0})\,(\overline{A_3} + \overline{A_0})\,(A_2 + \overline{A_1})}$$

$$O_3 = \overline{(\overline{A_1} + A_0)\,(\overline{A_3} + A_0)\,(\overline{A_2} + \overline{A_1})}$$

$$O_4 = \overline{(\overline{A_1} + \overline{A_0})\,(\overline{A_3} + \overline{A_1})\,(\overline{A_2} + \overline{A_0})}$$

$$O_5 = \overline{A_2}$$

TRUTH TABLE

BINARY INPUT TO 93401				3 OF 6 CODE OUTPUT OF 93401; INPUT TO 93400 (L = O OR X OR Y)						93400 93400B INTERNAL X OR Y ADDRESS
A_3	A_2	A_1	A_0	L_0	L_1	L_2	L_3	L_4	L_5	Row or Column
L	L	L	L	H	H	L	L	L	H	0
L	L	L	H	H	L	H	L	L	H	1
L	L	H	L	H	L	L	H	L	H	2
L	L	H	H	H	L	L	L	H	H	3
L	H	L	L	H	H	H	L	L	L	4
L	H	L	H	H	L	H	L	H	L	5
L	H	H	L	H	H	L	H	L	L	6
L	H	H	H	H	L	L	H	H	L	7
H	L	L	L	L	H	L	H	L	H	8
H	L	L	H	L	H	H	L	L	H	9
H	L	H	L	L	L	L	H	H	H	10
H	L	H	H	L	L	H	L	H	H	11
H	H	L	L	L	H	H	H	L	L	12
H	H	L	H	L	H	H	L	H	L	13
H	H	H	L	L	H	L	H	H	L	14
H	H	H	H	L	L	H	H	H	L	15

NOTE: Enables on 93401 must be LLHH. Any other state on the enable inputs causes 93401 outputs to go LOW, and addresses no internal row or column in the 93400 memory matrix.

93400 • 93400B ELECTRICAL CHARACTERISTICS (T_C = 0°C to 75°C in operation; V_{CC} = 5.0 V ±5%) (Part No. 93400XC/93400BXC)*

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS AND COMMENTS	
V_{OL}	Output LOW Voltage		0.45		0.20	0.45		0.45	Volts	I_{OL} = 5 mA	V_{CC} = 4.75 V, See Figure 3.
								0.55		I_{OL} = 10 mA	
I_{CE}	Output Leakage Current		100			100		100	µA	V_{CC} = 5.25 V, V_{CE} = 4.5 V All Inputs Grounded	
V_{IL}	Address, Write Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed LOW Input Threshold	
V_{IH}	Address, Write Input HIGH Voltage	2.0		2.0			2.0		Volts	Guaranteed HIGH Input Threshold	
I_{FI}	Data Input Forward Current		−250			−250		−250	µA	V_{CC} = 5.25 V, V_F = 0.45 V	
I_{FX}	X Address Input Forward Current		−250			−250		−250	µA	V_F = 0.45 V, V_{CC} = 5.25 V 2 other X Lines. 3 Y Lines @ 4.5 V Remaining X and Y Lines @ .45 V	
I_{FY}	Y Address Input Forward Current		−250			−250		−250	µA	V_F = 0.45 V, V_{CC} = 5.25 V 2 other Y Lines. 3 X Lines @ 4.5 V Remaining X and Y Lines @ .45 V	
I_{RX}	Address Input Leakage Current		20			20		20	µA	V_{CC} = 5.25 V, V_R = 4.5 V Other X and Y inputs grounded	
I_{RY}			20			20		20			
I_{FW}	Write Input Forward Current		−250			−250		−250	µA	V_{CC} = 5.25 V, V_F = 0.45 V	
I_{RW}	Write Input Leakage Current		20			20		20	µA	V_{CC} = 5.25 V, V_R = 4.5 V	
I_{CC}	Power Supply Current				100	140			mA	V_{CC} = 5.0 V, all inputs at ground	

93401 ELECTRICAL CHARACTERISTICS (T_C = 0°C to 75°C in operation; V_{CC} = 5.0 V ±5%) (Part No. 93401XC)*

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = 1.0 mA V_{IL} = value indicated below on this table	
V_{OL}	Output LOW Voltage		0.45		0.3	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 10 mA	
V_{IH}	Input HIGH Voltage	2.0		2.0			2.0		Volts	Guaranteed input HIGH threshold for all inputs	
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed input LOW threshold for all inputs	
I_{FA}	Add. Input Load Current		−0.4			−0.4		−0.4	mA	V_{CC} = 5.25 V	V_F = 0.45 V, V_R = 4.5 V on other inputs
I_{FE}	Enable Input Load Current		−0.4			−0.4		−0.4	mA	V_{CC} = 5.25 V	
I_{RA} & I_{RE}	Input Leakage Current		20			20		20	µA	V_{CC} = 5.25 V, V_R = 4.5 V, Gnd. on other inputs	
I_{CC}	Power Supply Current		140		120	140		140	mA	V_{CC} = 5.25 V, all inputs at ground	

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

93401 SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C) (See Fig. 2)

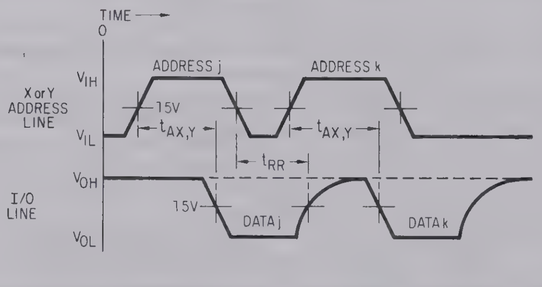
SYMBOL	PARAMETER	LIMITS C_L = 90 pF (Equiv. to 32 X Lines) TYP.	LIMITS C_L = 90 pF (Equiv. to 32 X Lines) MAX.	LIMITS C_L = 500 pF (Equiv. to 32 Y Lines) TYP.	LIMITS C_L = 500 pF (Equiv. to 32 Y Lines) MAX.	UNITS
t_A^{++}, t_A^{+-} t_A^{-+}, t_A^{--}	Delay from address going LOW or HIGH to output going LOW or HIGH	20	25	30	40	ns
t_E^{++}, t_E^{+-} t_E^{-+}, t_E^{--}	Delay from enable going active or inactive to output going HIGH or LOW	20	25	30	40	ns

93400 • 93400B SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C.) C_L = 47 pF; Equivalent to eight OR–tied 4100 outputs

SYMBOL	PARAMETER	93400 LIMITS			93400B LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{AX}	Read Access Time. Time from good X address to good data at output	30	70	100	30	100	200	ns
t_{AY}	Read Access Time. Time from good Y address to good data at output	15	45	65		45	100	ns
t_{RR}	Read Recovery Time. Time for output to go HIGH after removal of address.			100			150	ns
t_{WP}	Write Pulse Width. Width of pulse on WE required to write data into memory.	80			100			ns
t_{SH}	Data Setup Time. Time HIGH or LOW data must be present before end of write pulse to write proper data into memory.			t_{WP}+10			100	ns
t_{SL}				70 (Note 2)			70 (Note 3)	ns
t_{RH}	Data Release Time. This is the minimum set-up time. Removal of data after the release time will not affect the data written into the memory. See note 1.	0			0			ns
t_{RL}		10			10			ns
C_O	Output Capacitance		7.0			7.0		pF
C_{AX}	Input Capacitance for X address line		3.0			3.0		pF
C_{AY}	Input Capacitance for Y address line		15			15		pF
t_{AS}	Address Set Up Time. Time address must be good before end of write pulse during write operation. (See Fig. 3b)	80			80			ns
t_{AP}	Address Pulse Width. Time that address must remain good for write operation. (See Fig. 3b)	100			100			ns
t_{WR}	Write Recovery Time. Time in write-read cycle from end of write pulse to valid output data.			120			120	ns

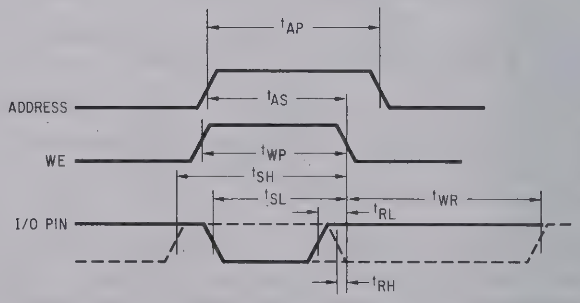
NOTES:
(1) The set up and release times define a window during which devices are responding to the data and/or address. Inputs must remain good at all times in between the set up and release time limits.
(2) Applies for write pulse less than 150 ns.
(3) Applies for write pulse more than 160 ns.

Fig. 1a—93400 TYPICAL READ CYCLE



$t_{AX,\,Y}$ is the time from a good address to good data on the output. Note that the access time may be overlapped with the recovery time to improve speed on consecutive read operations.

Fig. 1b—93400 WRITE CYCLE



The address must be maintained for 100 ns. The simplest write cycle is achieved by applying the data, then simultaneously raising the address and write pulses for 100 ns. If the write pulse width is less than 100 ns, then the address should come up at about the same time as the write pulse and should be held on after the write pulse. The address should not be applied more than 25 ns before the write pulse, because an early address will cause a read operation to begin disrupting data on the I/O lines (see t_{RR}). For a longer write pulse the address pulse may appear anytime as long as it starts before t_{AS} and lasts at least t_{AP}.

Fig. 2—93401 SWITCHING WAVEFORMS AND TEST LOAD CONDITIONS

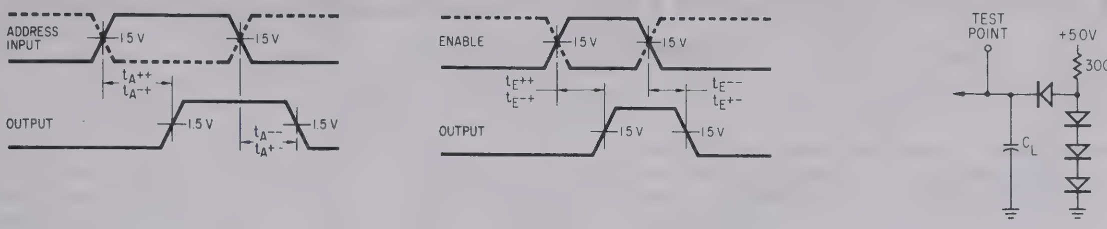
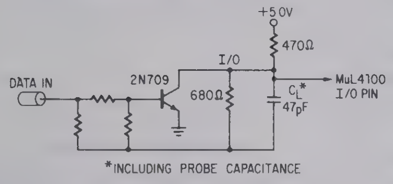

ADDRESS INPUT
1.5 V
1.5 V
t_{A++}
t_{A-+}
OUTPUT
1.5 V
1.5 V
t_{A--}
t_{A+-}
ENABLE
1.5 V
1.5 V
t_{E++}
t_{E-+}
t_{E--}
t_{E+-}
OUTPUT
1.5 V
1.5 V
TEST POINT
+5.0V
300Ω
C_L

Fig. 3
93400
TEST LOAD CONDITIONS


+5.0V
470Ω
I/O
DATA IN
2N709
680Ω
C_L*
47pF
MμL4100 I/O PIN
*INCLUDING PROBE CAPACITANCE

LOW Level ≤ 0.45 V
HIGH Level ≥ 3.0 V
Rise, Fall Time = 10 ±5 ns

Fig. 4
93400 STANDARD
INPUT PULSE

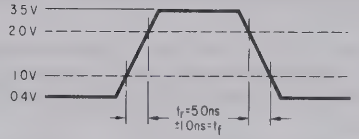
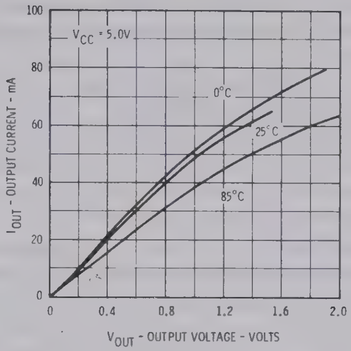

3.5 V
2.0 V
1.0 V
0.4 V
t_r=5.0ns ±1.0ns=t_f

Fig. 5
93400 • 93400B
OUTPUT CHARACTERISTICS



The timing curves in Figures 8 through 13 are obtained using the pulse shape in Figure 6 and the loading in Figure 5. In Figures 12 and 13 the C_L value in the load is varied.

Fig. 6
INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE

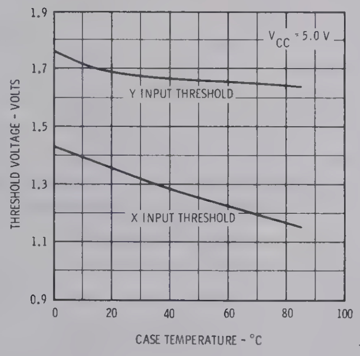


Fig. 7
X ACCESS TIME VERSUS TEMPERATURE

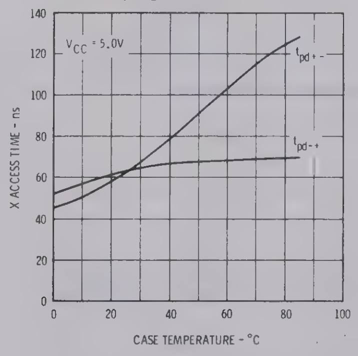


Fig. 8
Y ACCESS TIME VERSUS TEMPERATURE

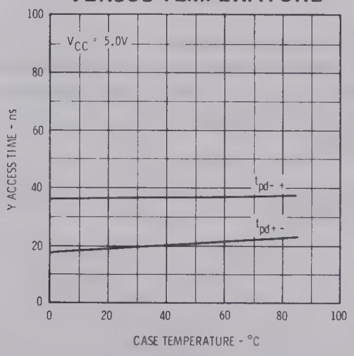


Fig. 9
MINIMUM WRITE PULSE WIDTH VERSUS TEMPERATURE

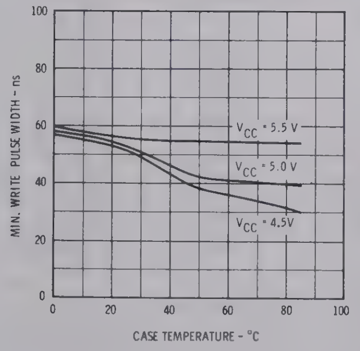


Fig. 10
X ACCESS TIME VERSUS LOAD CAPACITANCE

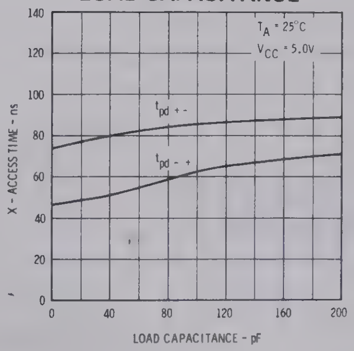
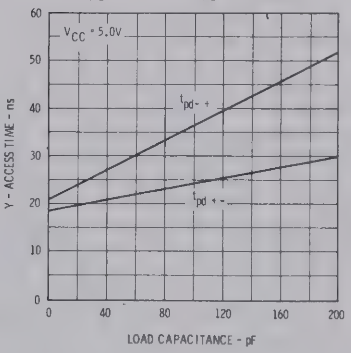


Fig. 11
Y ACCESS TIME VERSUS LOAD CAPACITANCE



TTL MEMORY 93402

16-BIT ASSOCIATIVE/CONTENT ADDRESSABLE MEMORY

FORMERLY 4102

DESCRIPTION – The 93402 is a high speed 16-Bit Associative Random Access Memory. It is a linear select 4-word by 4-bit array which performs the equality search on all bits in parallel. The 93402 is TTL compatible.

With the bit enable lines ($\overline{E}_0 - \overline{E}_3$) LOW, the outputs ($M_0 - M_3$) go HIGH if associated stored data matches the descriptor bits ($\overline{D}_0 - \overline{D}_3$). If a bit enable line is held HIGH, a match is forced on the corresponding bit in all the words regardless of the state of the descriptor bit ($\overline{D}_0 - \overline{D}_3$). An inverter is connected to the match output M_0 to give its negation $\overline{M}_0$.

A word is addressed by having an active LOW on the appropriate address line ($\overline{A}_0 - \overline{A}_3$). Any number of words may be addressed simultaneously.

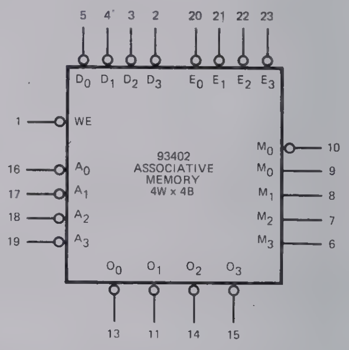
Data can be written into the memory through the data inputs ($\overline{D}_0 - \overline{D}_3$) under control of the address inputs and the appropriate bit enable ($\overline{E}_0 - \overline{E}_3$) when the write enable ($\overline{WE}$) is LOW.

Reading can occur either during an equality search or a write operation. If a single word is addressed that word will appear at the data outputs ($\overline{O}_0 - \overline{O}_3$). If multiple addressing is used, the word appearing at the data output is the AND (positive logic) or the OR (negative logic) of the addressed words.

All outputs are uncommitted collectors allowing maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93402's can be tied together. In other applications, the wired-OR is not used. In either case an external pull up resistor must be used to attain a HIGH at an output.

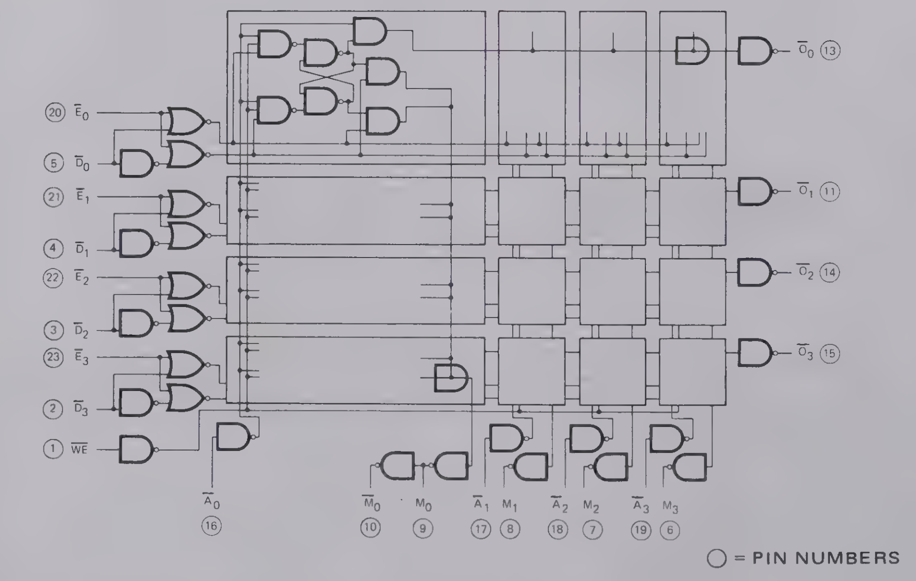
- **25 ns TYPICAL MATCH TIME**
- **MULTIPLE MATCHING AND ADDDRESSING**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR CAPABILITY**
- **LINEAR SELECT ADDRESSING**
- **BIT MASKING**

LOGIC SYMBOL

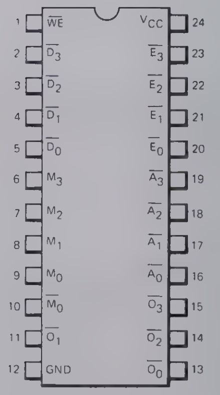

5 4 3 2 20 21 22 23
D0 D1 D2 D3 E0 E1 E2 E3
1 WE
16 A0
17 A1
18 A2
19 A3
93402 ASSOCIATIVE MEMORY 4W x 4B
M0 10
M0 9
M1 8
M2 7
M3 6
O0 O1 O2 O3
13 11 14 15

V_{CC} = Pin 24
Gnd = Pin 12

LOGIC DIAGRAM


20 E0
5 D0
21 E1
4 D1
22 E2
3 D2
23 E3
2 D3
1 WE
O0 13
O1 11
O2 14
O3 15
A0 16
M0 10
M0 9
A1 17
M1 8
A2 18
M2 7
A3 19
M3 6
○ = PIN NUMBERS

CONNECTION DIAGRAM DIP (TOP VIEW)


1 WE
2 D3
3 D2
4 D1
5 D0
6 M3
7 M2
8 M1
9 M0
10 M0
11 O1
12 GND
24 VCC
23 E3
22 E2
21 E1
20 E0
19 A3
18 A2
17 A1
16 A0
15 O3
14 O2
13 O0

LOADING RULES

	HIGH LEVEL (TTL Unit Loads)	LOW LEVEL (TTL Unit Loads)
Address	1.0	1.0
Bit Enable	1.5	1.5
Write Enable	1.5	1.5
Data Input	1.0	1.0
Data Output	Open Collector	6.2
Match Output	Open Collector	6.2

1 Unit Load (U.L.) = 60 μA HIGH/1.6 mA LOW.

The external pull-up resistor R is selected to lie in the range as shown.

$$\frac{5.1}{10 - \text{F.O.}\,(1.6)} \le R \le \frac{2.1}{NL + \text{F.O.}\,(0.06)}$$

R is in kΩ
N = number of wired-OR outputs
F.O. = number of TTL loads driven
L = Sum of all I_{CEX} of wired-OR outputs

The minimum value of R is limited by output current sinking ability. The maximum value of R is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

F.O.	Maximum number of Wired-OR's
1	66
2	52
3	38
4	24
5	10
5.7	0

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground	–0.5 V to +7.0 V
Input Pin Voltage	–0.5 V to +5.5 V
Current into Output Terminal	50 mA
Output Voltage	–0.5 V to +8.0 V

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested) (Part No. 93402XC)*

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		–1.6		–1.6		–1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FB}	Bit Enable Load Current		–2.4		–2.4		–2.4	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V
I_{FWE}	Write Enable Load Current		–2.4		–2.4		–2.4	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FI}	Data Input Load Current		–1.6		–1.6		–1.6	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RBE}	Bit Enable Input Leakage Current		90		90		90	μA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		90		90		90	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RI}	Data Input Leakage Current		60		60		60	μA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current (Note 4)		50		50		50	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25 V
$I_{CEX}\ M_0$	Output Leakage Current for M_0		110		110		110	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25 V
V_{OL}	Output LOW Voltage (Note 5)		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 10 mA One Word Addressed
V_{IL}	Input LOW Voltage (Note 6)		0.85		0.85		0.85	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input HIGH Voltage (Note 6)	2.0		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{CC}	Supply Current		125		125		125	mA	V_{CC} = 5.25 V, Worst Case

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
(4) For all outputs except M_0.
(5) For all outputs.
(6) For all inputs

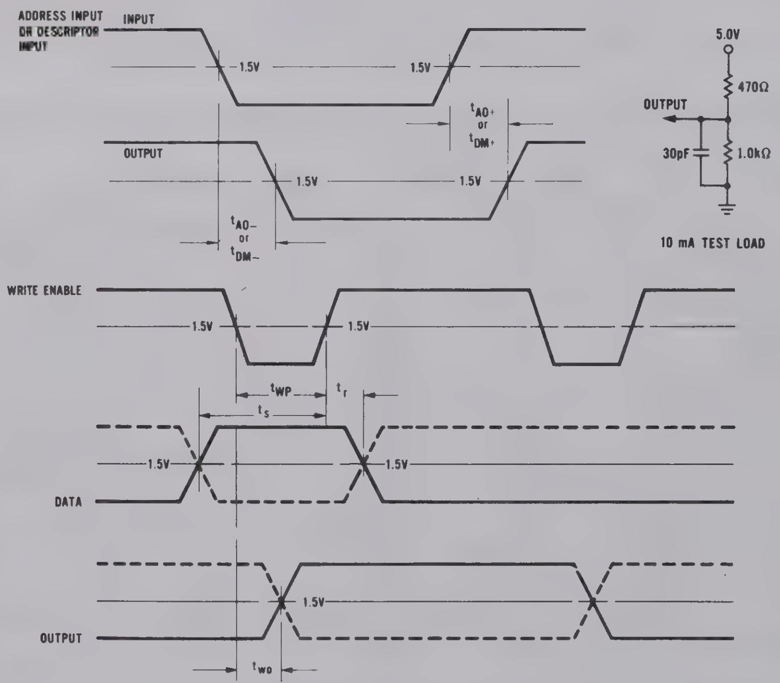
SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

SYMBOL	PARAMETER	LIMIT (ns)		LOAD	CONDITIONS	NOTE
		TYP.	MAX.		C	
t_{AO-}	Address to Output Turn-On Delay	20	30	10 mA	30 pF	1
t_{AO+}	Address to Output Turn-Off Delay	25	35	10 mA	30 pF	1
t_{DM+}	Descriptor to Output Match Turn-On Delay	25	35	10 mA	30 pF	2
t_{DM-}	Descriptor to Output Match Turn-Off Delay	30	40	10 mA	30 pF	2
t_{WP}	Write Pulse Width Required to Write	33	40	10 mA	30 pF	
t_{WO}	Write Delay	50	80	10 mA	30 pF	
t_s	Maximum Set-up Time on Data Input	33	40	10 mA	30 pF	3
t_r	Release Time (Minimum Set-up Time) on Data Input	0	19	10 mA	30 pF	3

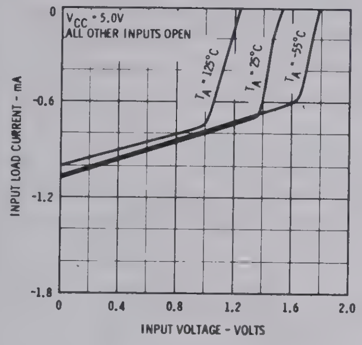
NOTES:
(1) To test t_{AO+} and t_{AO-} a LOW must be stored in the cell under test.
(2) To test t_{DM-} and t_{DM+}, a mismatch must occur in at least one bit of the word under test
(3) Setup and release times are measured with respect to the rising edge of the Write enable. To guarantee writing in the correct data, the data input must be good by t_s and remain good until after t_r.

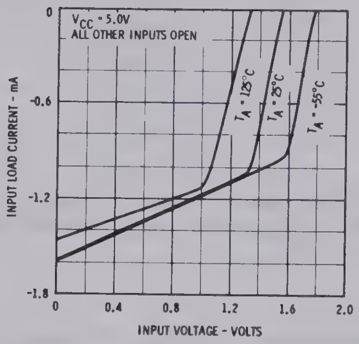
The typical capacitance of one 93402 output is 7.0 pF.

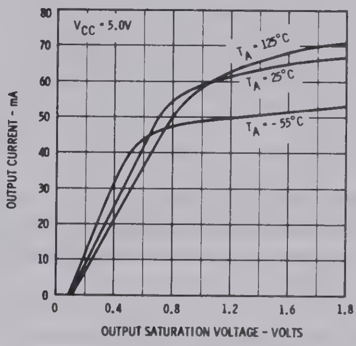
SWITCHING WAVEFORMS

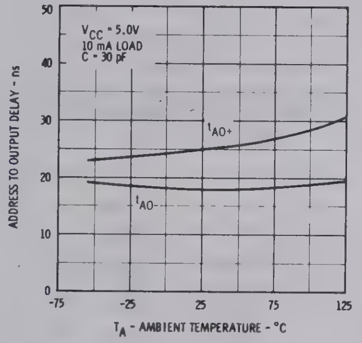

ADDRESS INPUT OR DESCRIPTOR INPUT
INPUT
1.5V
1.5V
t_{AO+} or t_{DM+}
OUTPUT
1.5V
1.5V
t_{AO-} or t_{DM-}
WRITE ENABLE
1.5V
1.5V
t_{WP}
t_r
t_s
1.5V
1.5V
DATA
1.5V
OUTPUT
t_{wo}
5.0V
470Ω
OUTPUT
30pF
1.0kΩ
10 mA TEST LOAD

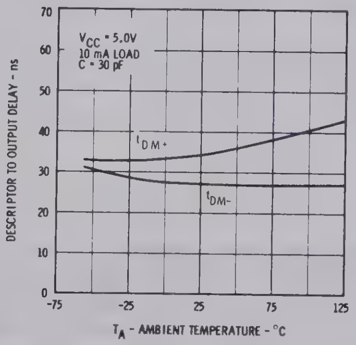
TYPICAL ELECTRICAL CHARACTERISTICS

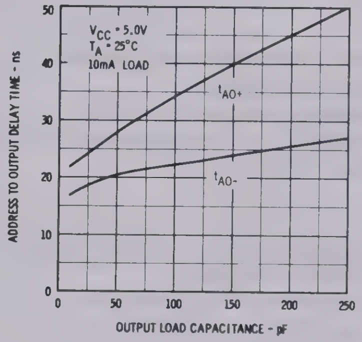

DATA AND ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

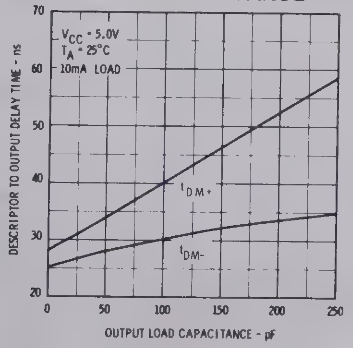

WRITE ENABLE AND BIT ENABLE INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

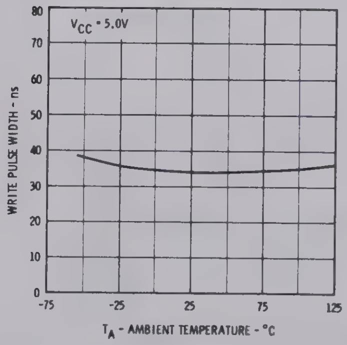

OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE ALL OUTPUTS


ADDRESS TO OUTPUT DELAY TIME VERSUS AMBIENT TEMPERATURE


DESCRIPTOR TO OUTPUT DELAY TIME VERSUS AMBIENT TEMPERATURE


ADDRESS TO OUTPUT DELAY TIME VERSUS LOAD CAPACITANCE


DESCRIPTOR TO OUTPUT DELAY TIME VERSUS LOAD CAPACITANCE


WORST CASE WRITE PULSE WIDTH VERSUS AMBIENT TEMPERATURE

TTL MEMORY 93403

64-BIT FULLY DECODED READ/WRITE MEMORY

FORMERLY 4103

DESCRIPTION — The 93403 is a high speed 64-Bit Read/Write Memory organized 16 words by four bits. Four address lines are buffered and decoded "on chip" for word selection. The 93403 is made with TTL circuitry and all inputs are equivalent to one TTL load.

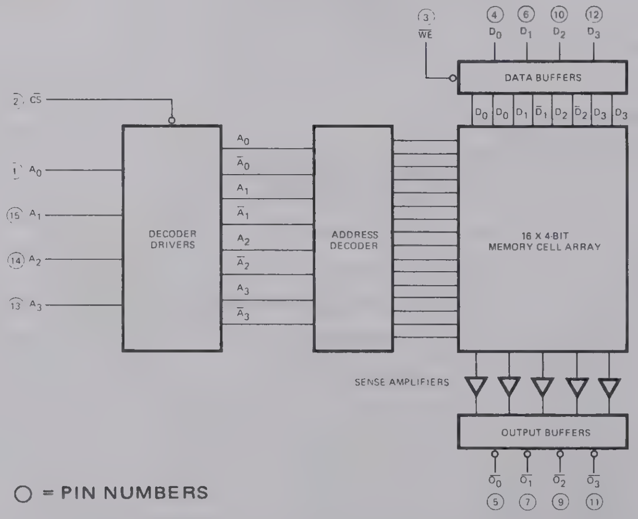
OPERATION — When the 93403 receives a LOW at the Chip Select ($\overline{CS}$) input, the binary address (A_0, A_1, A_2 and A_3) is decoded to select one of sixteen 4-bit words. If the Write Enable ($\overline{WE}$) is at a HIGH level, the contents of the selected word are non-destructively read out and the sense amplifier outputs ($\overline{O_0}$, $\overline{O_1}$, $\overline{O_2}$ and $\overline{O_3}$) reflect the state of the stored data in the four bits of the selected word. If the Write Enable is LOW, the data present on the Data Input lines (D_0, D_1, D_2 and D_3) is written into the four bits of the selected word. Note that there is inversion through the device in a read operation.

- OUTPUT WIRED-OR CAPABILITY
- ON CHIP DECODING
- NON-DESTRUCTIVE READOUT
- CHIP SELECT FOR SYSTEM WORD EXPANSION
- TTL COMPATIBLE

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

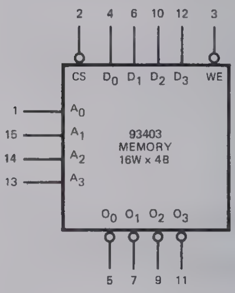
Storage Temperature	-65°C to + 150°C
Temperature (Case) Under Bias	-55°C to + 125°C
V_{CC} Pin Potential to Ground	-0.5 V to + 8.0 V
Input Pin Voltage	-1.5 V to + 5.5 V
Current Into Output Terminal	100 mA
Output Voltage (external circuit dependent)	-0.5 V to + 8.0 V

BLOCK DIAGRAM



3 WE
4 D0
6 D1
10 D2
12 D3
DATA BUFFERS
D0 D̄0 D1 D̄1 D2 D̄2 D3 D̄3
2 CS
1 A0
15 A1
14 A2
13 A3
DECODER DRIVERS
A0 Ā0 A1 Ā1 A2 Ā2 A3 Ā3
ADDRESS DECODER
16 X 4-BIT MEMORY CELL ARRAY
SENSE AMPLIFIERS
OUTPUT BUFFERS
Ō0 Ō1 Ō2 Ō3
5 7 9 11
○ = PIN NUMBERS

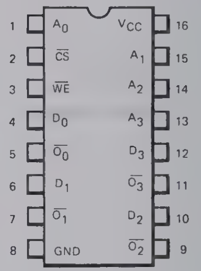
LOGIC SYMBOL



2 4 6 10 12 3
CS D0 D1 D2 D3 WE
1 A0
15 A1
14 A2
13 A3
93403 MEMORY 16W x 4B
O0 O1 O2 O3
5 7 9 11

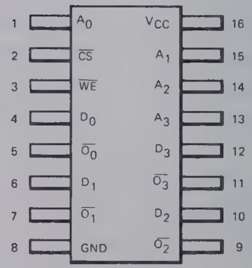
V_{CC} = Pin 16
Gnd = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 A0
2 CS
3 WE
4 D0
5 Ō0
6 D1
7 Ō1
8 GND
16 VCC
15 A1
14 A2
13 A3
12 D3
11 Ō3
10 D2
9 Ō2

FLATPAK (TOP VIEW)



1 A0
2 CS
3 WE
4 D0
5 Ō0
6 D1
7 Ō1
8 GND
16 VCC
15 A1
14 A2
13 A3
12 D3
11 Ō3
10 D2
9 Ō2

ELECTRICAL CHARACTERISTICS (T_{case} = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested) (Part No. 93403XC)

SYMBOL	TEST	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FCS}	Chip Select Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V
I_{FWE}	Write Enable Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FD}	Date Input Load Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		60		60		60	µA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		60		60		60	µA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		60		60		60	µA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		60		60		60	µA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	µA	V_{CC} = 5.25 V, V_{CEX} = 5.25V 3.0 on Chip Select
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 16 mA $\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IH}
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{CC}	Supply Current		110		110		110	mA	V_{CC} = 5.25 V, Write Enable = 3.0 V, other inputs Grounded
V_{CD}	Clamp Diode Voltage, All Inputs		-1.0		-1.0		-1.0	V	I_{CD} = -5.0 mA
BV_X	Breakdown Voltage, All Inputs	5.5		5.5		5.5		V	I_X = 1.0 mA

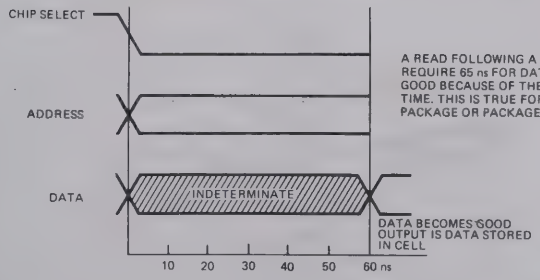
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	DEFINITION	LIMITS 25°C MIN.	TYP.	MAX.	UNITS
t_A	Read Access Time	Time From Switching Address Or Chip Select To Data At Output		45	60	ns
t_{SR}	Sense Recovery Time	Time From Switching Address Or Chip Select To Output HIGH		45	60	ns
t_{WP}	Write Pulse	Write Pulse Width - Width of Pulse Guaranteed to Write	45	30		ns
t_{WR}	Write Recovery Time	Time From Write Pulse Going HIGH to Output LOW			65	ns
t_{DH}	Data Hold Time	Time From Write Pulse Going HIGH to Change Data Or Address			5.0	ns
t_{DS}	Data Set-Up Time	Time Data Must Be Present Before Write Pulse	5.0	0		ns
t_{AS}	Address Strobe Time	Time Address Must Be Present in Order to Write	5.0	10	45	ns

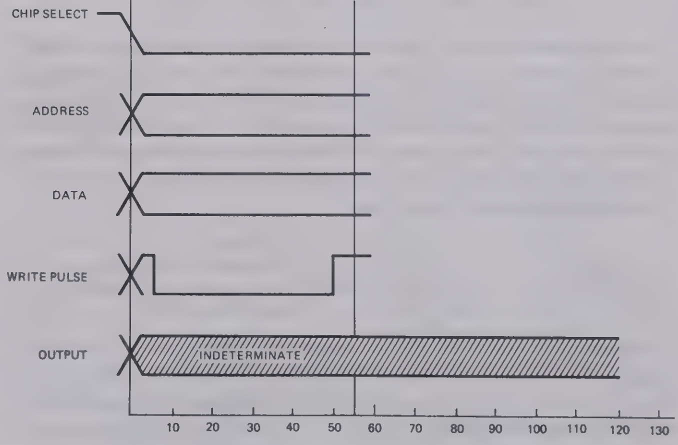
WAVEFORMS

READ MODE



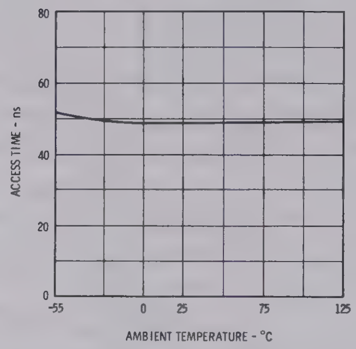
A READ FOLLOWING A WRITE WILL REQUIRE 65 ns FOR DATA TO BECOME GOOD BECAUSE OF THE WRITE RECOVERY TIME. THIS IS TRUE FOR A SINGLE PACKAGE OR PACKAGES "OR" TIED.

WRITE MODE

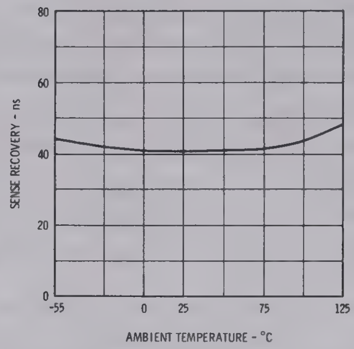


TYPICAL ELECTRICAL CHARACTERISTICS

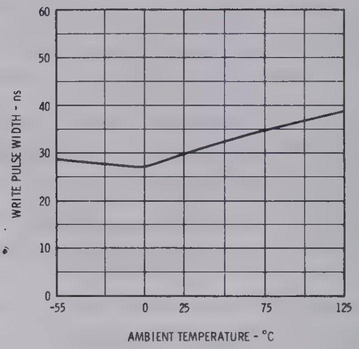
ACCESS TIME (t_A) VERSUS TEMPERATURE



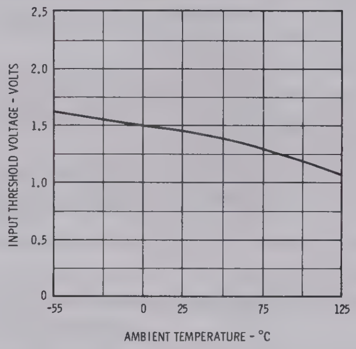
SENSE RECOVERY TIME (t_{SR}) VERSUS TEMPERATURE



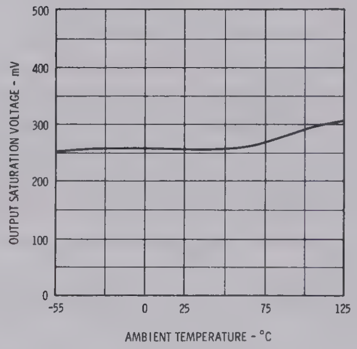
WRITE PULSE WIDTH (t_{WP}) VERSUS TEMPERATURE



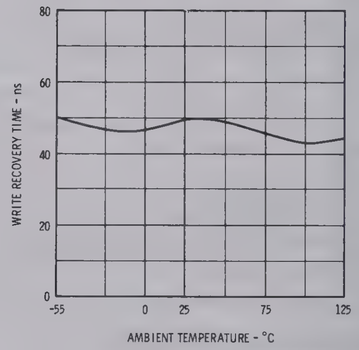
INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



OUTPUT SATURATION VOLTAGE VERSUS TEMPERATURE



WRITE RECOVERY TIME (t_{WR}) VERSUS TEMPERATURE



TTL LOADING RULES

	HIGH LEVEL	LOW LEVEL
Address	1 U. L.	1 U. L.
Chip Select	1 U. L.	1 U. L.
Write Enable	1 U. L.	1 U. L.
Data Input	1 U. L.	1 U. L.
Data Output	Open Collector	10 U. L.

1 LOW Level TTL Unit Load (U.L.) = 1.6 mA
1 HIGH Level TTL Unit Load (U.L.) = 60 μA

Uncommitted collector outputs are provided on the 93403 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93403 can be tied together. In other applications the wired-OR is not used. In either case an external pullup resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{5.05}{16 - \text{F.O.}\,(1.6)} \leq R_L \leq \frac{2.1}{N\,(0.1) + \text{F.O.}\,(0.06)}$$

R_L is in kΩ
N = number of wired-OR outputs
F.O. = number of TTL loads driven
$V_{CC} = 5.0\ \text{V} \pm 10\%$

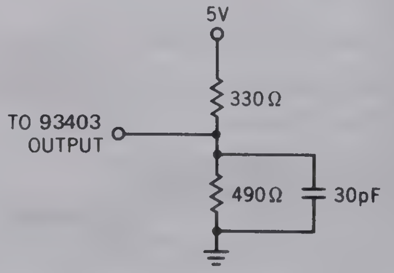
The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

TRUTH TABLE

WE	CS	OUTPUT	MODE
H	H	HIGH No Glitches	Not Read
L	H	Indeterminate Output	Not Write
H	L	Function of Data Stored in Cell	Read
L	L	Indeterminate Output	Write

SWITCHING TEST CIRCUIT

15 mA LOAD



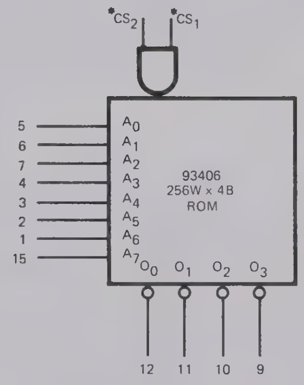
TTL MEMORY 93406
1024-BIT READ ONLY MEMORY

DESCRIPTION – The Fairchild 93406 is a 1024-bit Bipolar Read Only Memory organized 256 words by four bits. An 8-bit binary address is used to select the desired word. The four outputs are uncommitted collectors which permit "OR" tying of the outputs for expanding the memory in the word direction. The customer can specify the active level of the 2-input chip select gate. $\overline{CS}_1$ and $\overline{CS}_2$ both will be active LOW unless otherwise specified by the customer. The programmable enable feature allows expansion of the memory to 1024 words without any external gates.

The contents of the memory are mask programmed to the customers specification. The customer can specify the desired ROM code on either the 93406 Coding Form(s) or by punched cards using the 93406 Data Card Format.

- **DTL AND TTL COMPATIBLE**
- **ACCESS TIME – 50 ns MAX**
- **FULLY DECODED – ON CHIP ADDRESS DECODER AND BUFFER**
- **2 CHIP SELECT INPUTS PROVIDING EASY MEMORY EXPANSION**
- **PROGRAMMABLE CHIP SELECTS**
- **OR-TIE CAPABILITY**
- **STANDARD 16-LEAD DUAL IN-LINE PACKAGE**

LOGIC SYMBOL


*CS2
*CS1
5
6
7
4
3
2
1
15
A0
A1
A2
A3
A4
A5
A6
A7
93406
256W x 4B
ROM
O0
O1
O2
O3
12
11
10
9

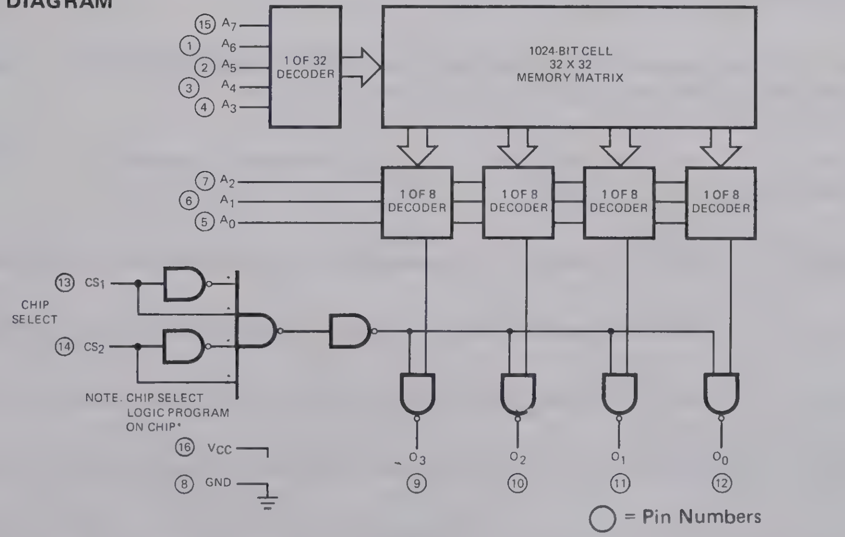
V_{CC} = PIN 16
GND = PIN 8

*Chip selects active level may be programmed per customer requirements. If not specified both CS will be active low.

PIN NAMES

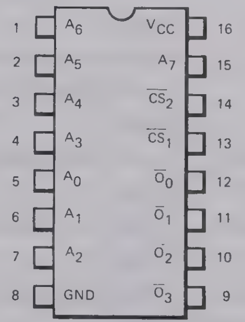
A_0 to A_7	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
$\overline{O}_0$ to $\overline{O}_3$	Data Outputs

LOGIC DIAGRAM


15 A7
1 A6
2 A5
3 A4
4 A3
1 OF 32 DECODER
1024-BIT CELL
32 X 32
MEMORY MATRIX
7 A2
6 A1
5 A0
1 OF 8 DECODER
1 OF 8 DECODER
1 OF 8 DECODER
1 OF 8 DECODER
13 CS1
CHIP SELECT
14 CS2
NOTE: CHIP SELECT LOGIC PROGRAM ON CHIP*
16 VCC
8 GND
O3 9
O2 10
O1 11
O0 12
○ = Pin Numbers

*Per customer request. Unless otherwise specified CS_1 and CS_2 will be active low.

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 A6
2 A5
3 A4
4 A3
5 A0
6 A1
7 A2
8 GND
16 VCC
15 A7
14 CS2
13 CS1
12 O0
11 O1
10 O2
9 O3

93406 DATA CARD FORMAT

The most efficient method of ordering the 93406 is to punch the desired truth table on a punched card in the format described below. Fairchild will generate mask and test program data directly from these inputs. This eliminates the chance of error when transcribing inputs from a hand written truth table.

Data should be provided on a deck of 34 standard 80 column cards containing the following information.

CARD NO. 1 — Customer Identification

Column	Content
1	Blank
2–28	Customer Name, Drawing or Specification control number.
29–32	Blank
33–39	FAIRCHILD PART NUMBER. This part number is supplied by the factory through your Fairchild sales representative.
40–64	Blank
65–72	Date
73–80	Blank

CARD NO. 2 — Chip Select Option

Column	Content
1–11	Punch "Chip Select"
12	Blank
13, 14	Punch Charts '00', '01', '10' or '11', depending on the chip select code option. (First bit represents CS_1 input, second bit represents CS_2 input. '0' = LOW, '1' = HIGH.)
15–32	Blank
33–39	Repeat FAIRCHILD PART NUMBER (This is used for positive identification).
40–80	Blank

CARDS NO. 3 through 34 — Truth Table Deck

Each card will contain instructions for the output levels for 8 input words.

Column	Content
1–7	Punch the numerals representing the first and last words on that card (i.e.: 000-007, 008-015, 016-023. . .248-255). Word order is determined by the value of the binary address — A_7 = MSB, A_0 = LSB.
8–9	Blank
10–13	Punch the desired combination of "1's" and "0's" representing the output levels for outputs O_3, O_2, O_1 and O_0 (in that order), for the first word on the card, '0' = LOW, '1' = HIGH.
14	Blank
15–18	Punch the desired combination of "1's" and "0's" representing the output levels for the second word on the card.
19	Blank
20–23	Punch the desired combination of "1's" and "0's" representing the output levels for the third word on the card.
24	Blank
25–28	Punch the desired combination of "1's" and "0's" representing the output levels for the fourth word on the card.
29	Blank
30–33	Punch the desired combination of "1's" and "0's" representing the output levels for the fifth word on the card.
34	Blank

CARDS NO. 3 through 34 – Truth Table Deck (cont'd)

Column	Content
35–38	Punch the desired combination of "1's" and "0's" representing the output levels for the sixth word on the card.
39	Blank
40–43	Punch the desired combination of "1's" and "0's" representing the output levels for the seventh word on the card.
44	Blank
45–48	Punch the desired combination of "1's" and "0's" representing the output levels for the eighth word on the card.
49	Blank
50–51	Repeat chip select code option as in columns 13 and 14 of card number 2.
52–59	Blank
60–66	Repeat FAIRCHILD PART NUMBER (this number is used for positive identificaiton).
67	Blank
68–80	Use optional.

93406 Address Scheme

The 93406 is organized 256 words by 4-bits. The words are numbered 0 through 255 and are addressed using sequential addressing of address inputs A_0 through A_7, with A_0 as the least significant digit.

	INPUTS							
WORD	Pin 15	Pin 1	Pin 2	Pin 3	Pin 4	Pin 7	Pin 6	Pin 5
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
WORD 0	0	0	0	0	0	0	0	0
WORD 1	0	0	0	0	0	0	0	1
WORD 2	0	0	0	0	0	0	1	0
WORD 3	0	0	0	0	0	0	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
WORD 255	1	1	1	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to V_{CC} Value

D C ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current			40	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25V Address any HIGH output
V_{OL}	Output LOW Voltage			0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 15 mA Address any LOW output
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.85	Volts	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current				mA	V_{CC} = 5.25 V, V_F = 0.45 V
	I_{FA} (Address Inputs)			0.8		
	I_{FCS} (Chip Select Inputs)			0.8		
I_R	Input HIGH, Current				μA	V_{CC} = 5.25 V, V_R = 4.5 V
	I_{RA} (Address Inputs)			40		
	I_{RCS} (Chip Select Input)			40		
I_{CC}	Power Supply Current		114	130	mA	V_{CC} = 5.25 V, Outputs open Inputs Grounded and Chip Selected
C_O	Output Capacitance		6.5		pF	V_{CC} = 5.0 V, V_O = 5.0 V, f = 1.0 MHz
V_{CD}	Input Clamp Diode Voltage		−0.8	−1.0	Volts	V_{CC} = 4.75 V, I_A = −5.0 mA

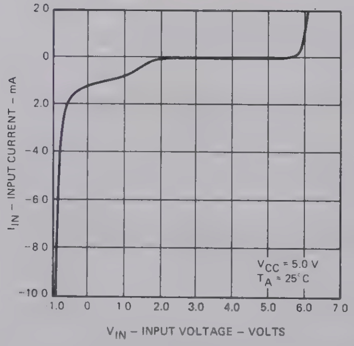
TTL LOADING RULES

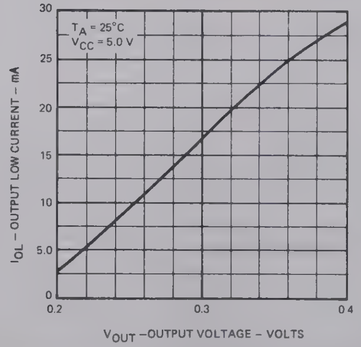
INPUT	LOADING HIGH	LOADING LOW
A_7 to A_0	1 U.L.	0.5 U.L.
CS_1, CS_2	1 U.L.	0.5 U.L.

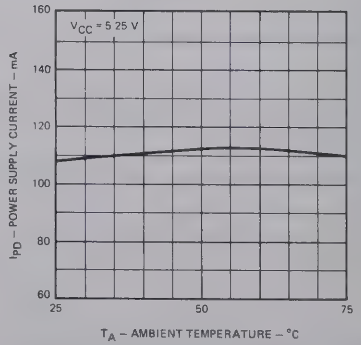
1 U.L. = 40 μA HIGH/1.6 mA LOW

OUTPUTS	DRIVE FACTOR HIGH	DRIVE FACTOR LOW
O_0 to O_3	OPEN COLLECTOR	9.3

TYPICAL ELECTRICAL CHARACTERISTICS


INPUT CURRENT VERSUS INPUT VOLTAGE


OUTPUT LOW CURRENT VERSUS OUTPUT VOLTAGE


POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 0°C to +75°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION
t_{pd++}	Propagation Delay Time, LOW to HIGH Output from Chip Select (or Address) LOW to HIGH		30	50	ns	C_L = 30 pF R_{L1} = 300Ω R_{L2} = 600Ω See Fig. 1
t_{pd+-}	Propagation Delay Time, HIGH to LOW Output from Chip Select (or Address) LOW to HIGH		30	50	ns	
t_{pd-+}	Propagation Delay Time, LOW to HIGH Output from Chip Select (or Address) HIGH to LOW		30	50	ns	
t_{pd--}	Propagation Delay Time, HIGH to LOW Output from Chip Select (or Address) HIGH to LOW		30	50	ns	

NOTE:
First + or – of t_{pd} indicates change in chip select, or address line. Second + or – indicates change in output.

"+" ≡ Low Voltage to High Voltage
"–" ≡ High Voltage to Low Voltage

NOTES:
(1) To test CS delay, apply input pulse to CS input. The word selected must contain a '0' in the bit under test.
(2) To test t_{pd++} and t_{pd--}delay, apply input pulse to the address input under test. The word selected must contain '0' when the input pulse is LOW, and a '1' when the input pulse is HIGH in the bit under test.
(3) To test t_{pd+-} and t_{pd-+} delay, apply input pulse to the address input under test. The word selected must contain a '1' when the input pulse is LOW, and a '0' when the input pulse is HIGH in the bit under test.

SWITCHING TEST OUTPUT LOAD

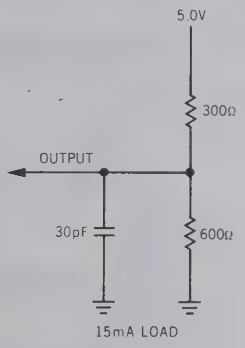
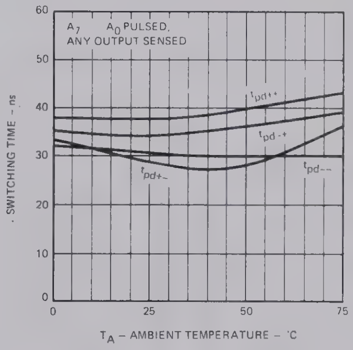
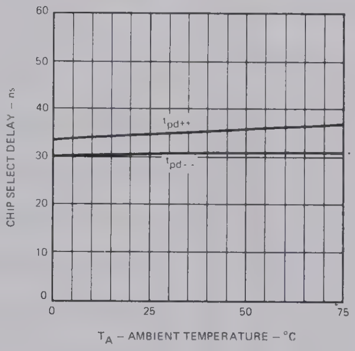

5.0V
300Ω
OUTPUT
30pF
600Ω
15mA LOAD

Fig. 1

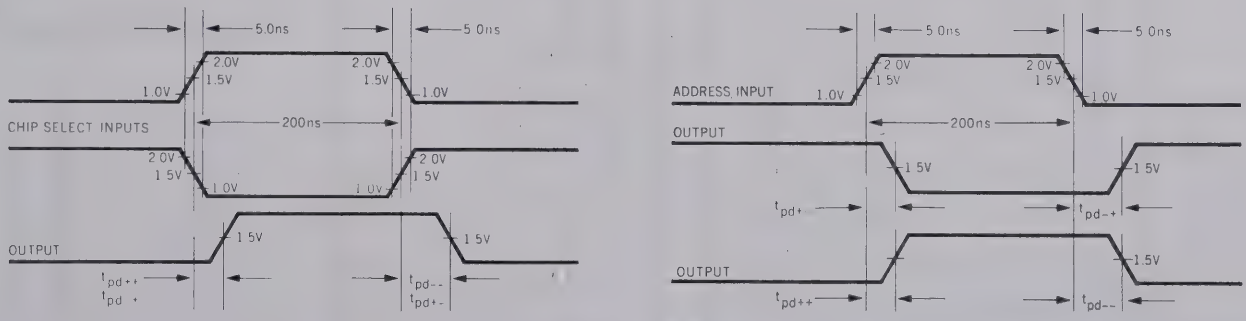
SWITCHING TIME VERSUS AMBIENT TEMPERATURE



CHIP SELECT DELAY TIME VERSUS AMBIENT TEMPERATURE (CS_1 TO O_0)



SWITCHING WAVEFORMS


5.0ns
5.0ns
2.0V
1.5V
1.0V
200ns
CHIP SELECT INPUTS
OUTPUT
1.5V
t_{pd++}
t_{pd-+}
t_{pd--}
t_{pd+-}
ADDRESS INPUT
OUTPUT
t_{pd+-}
t_{pd-+}
OUTPUT
t_{pd++}
t_{pd--}

TTL MEMORY 93406

1024-BIT READ ONLY MEMORY

CUSTOMER CODING FORM

CUSTOM ROM TRUTH TABLE

CUSTOMER ____________________ Location ____________________

Cust. P/N ____________________ Cust. Dwg. # ____________________

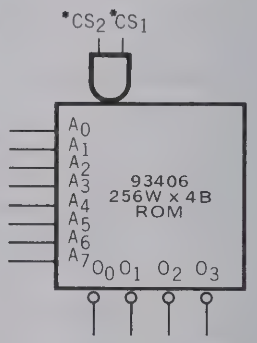
Function ____________________ SL # ____________________

Chip Select Code — CS_1 (13) = ___, CS_2 (14) = ___.*

*If not specified, ship select code will be '00'. Package pin numbers are shown in parenthesis.

Input									Output			
MSB								Word #	MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0				
0	0	0	0	0	0	0	1	1				
0	0	0	0	0	0	1	0	2				
0	0	0	0	0	0	1	1	3				
0	0	0	0	0	1	0	0	4				
0	0	0	0	0	1	0	1	5				
0	0	0	0	0	1	1	0	6				
0	0	0	0	0	1	1	1	7				
0	0	0	0	1	0	0	0	8				
0	0	0	0	1	0	0	1	9				
0	0	0	0	1	0	1	0	10				
0	0	0	0	1	0	1	1	11				
0	0	0	0	1	1	0	0	12				
0	0	0	0	1	1	0	1	13				
0	0	0	0	1	1	1	0	14				
0	0	0	0	1	1	1	1	15				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

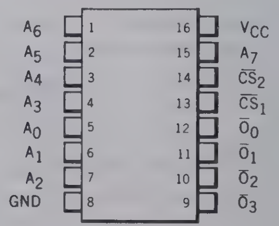
LOGIC SYMBOL


*CS2 *CS1
A0
A1
A2
A3
A4
A5
A6
A7
93406
256W x 4B
ROM
O0 O1 O2 O3

V_{CC} = PIN 16
GND = PIN 8

*Chip selects active level may be programmed per customer requirements. If not specified both CS will be active low.

CONNECTION DIAGRAM


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 C̄S̄2
13 C̄S̄1
12 Ō0
11 Ō1
10 Ō2
9 Ō3

Input								Word	Output			
MSB									MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
0	0	0	1	0	0	0	0	16				
0	0	0	1	0	0	0	1	17				
0	0	0	1	0	0	1	0	18				
0	0	0	1	0	0	1	1	19				
0	0	0	1	0	1	0	0	20				
0	0	0	1	0	1	0	1	21				
0	0	0	1	0	1	1	0	22				
0	0	0	1	0	1	1	1	23				
0	0	0	1	1	0	0	0	24				
0	0	0	1	1	0	0	1	25				
0	0	0	1	1	0	1	0	26				
0	0	0	1	1	0	1	1	27				
0	0	0	1	1	1	0	0	28				
0	0	0	1	1	1	0	1	29				
0	0	0	1	1	1	1	0	30				
0	0	0	1	1	1	1	1	31				
0	0	1	0	0	0	0	0	32				
0	0	1	0	0	0	0	1	33				
0	0	1	0	0	0	1	0	34				
0	0	1	0	0	0	1	1	35				
0	0	1	0	0	1	0	0	36				
0	0	1	0	0	1	0	1	37				
0	0	1	0	0	1	1	0	38				
0	0	1	0	0	1	1	1	39				
0	0	1	0	1	0	0	0	40				
0	0	1	0	1	0	0	1	41				
0	0	1	0	1	0	1	0	42				
0	0	1	0	1	0	1	1	43				
0	0	1	0	1	1	0	0	44				
0	0	1	0	1	1	0	1	45				
0	0	1	0	1	1	1	0	46				
0	0	1	0	1	1	1	1	47				
0	0	1	1	0	0	0	0	48				
0	0	1	1	0	0	0	1	49				
0	0	1	1	0	0	1	0	50				
0	0	1	1	0	0	1	1	51				
0	0	1	1	0	1	0	0	52				
0	0	1	1	0	1	0	1	53				
0	0	1	1	0	1	1	0	54				
0	0	1	1	0	1	1	1	55				
0	0	1	1	1	0	0	0	56				
0	0	1	1	1	0	0	1	57				
0	0	1	1	1	0	1	0	58				
0	0	1	1	1	0	1	1	59				
0	0	1	1	1	1	0	0	60				
0	0	1	1	1	1	0	1	61				
0	0	1	1	1	1	1	0	62				
0	0	1	1	1	1	1	1	63				
0	1	0	0	0	0	0	0	64				
0	1	0	0	0	0	0	1	65				
0	1	0	0	0	0	1	0	66				
0	1	0	0	0	0	1	1	67				
0	1	0	0	0	1	0	0	68				
0	1	0	0	0	1	0	1	69				
0	1	0	0	0	1	1	0	70				
0	1	0	0	0	1	1	1	71				
0	1	0	0	1	0	0	0	72				
0	1	0	0	1	0	0	1	73				
0	1	0	0	1	0	1	0	74				
0	1	0	0	1	0	1	1	75				
0	1	0	0	1	1	0	0	76				
0	1	0	0	1	1	0	1	77				
0	1	0	0	1	1	1	0	78				
0	1	0	0	1	1	1	1	79				
0	1	0	1	0	0	0	0	80				
0	1	0	1	0	0	0	1	81				
0	1	0	1	0	0	1	0	82				
0	1	0	1	0	0	1	1	83				
0	1	0	1	0	1	0	0	84				
0	1	0	1	0	1	0	1	85				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

Input									Output				Input									Output			
MSB									MSB				MSB									MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Word #	O_3	O_2	O_1	O_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Word #	O_3	O_2	O_1	O_0
0	1	0	1	0	1	1	0	86					0	1	1	1	1	0	0	1	121				
0	1	0	1	0	1	1	1	87					0	1	1	1	1	0	1	0	122				
0	1	0	1	1	0	0	0	88					0	1	1	1	1	0	1	1	123				
0	1	0	1	1	0	0	1	89					0	1	1	1	1	1	0	0	124				
0	1	0	1	1	0	1	0	90					0	1	1	1	1	1	0	1	125				
0	1	0	1	1	0	1	1	91					0	1	1	1	1	1	1	0	126				
0	1	0	1	1	1	0	0	92					0	1	1	1	1	1	1	1	127				
0	1	0	1	1	1	0	1	93					1	0	0	0	0	0	0	0	128				
0	1	0	1	1	1	1	0	94					1	0	0	0	0	0	0	1	129				
0	1	0	1	1	1	1	1	95					1	0	0	0	0	0	1	0	130				
0	1	1	0	0	0	0	0	96					1	0	0	0	0	0	1	1	131				
0	1	1	0	0	0	0	1	97					1	0	0	0	0	1	0	0	132				
0	1	1	0	0	0	1	0	98					1	0	0	0	0	1	0	1	133				
0	1	1	0	0	0	1	1	99					1	0	0	0	0	1	1	0	134				
0	1	1	0	0	1	0	0	100					1	0	0	0	0	1	1	1	135				
0	1	1	0	0	1	0	1	101					1	0	0	0	1	0	0	0	136				
0	1	1	0	0	1	1	0	102					1	0	0	0	1	0	0	1	137				
0	1	1	0	0	1	1	1	103					1	0	0	0	1	0	1	0	138				
0	1	1	0	1	0	0	0	104					1	0	0	0	1	0	1	1	139				
0	1	1	0	1	0	0	1	105					1	0	0	0	1	1	0	0	140				
0	1	1	0	1	0	1	0	106					1	0	0	0	1	1	0	1	141				
0	1	1	0	1	0	1	1	107					1	0	0	0	1	1	1	0	142				
0	1	1	0	1	1	0	0	108					1	0	0	0	1	1	1	1	143				
0	1	1	0	1	1	0	1	109					1	0	0	1	0	0	0	0	144				
0	1	1	0	1	1	1	0	110					1	0	0	1	0	0	0	1	145				
0	1	1	0	1	1	1	1	111					1	0	0	1	0	0	1	0	146				
0	1	1	1	0	0	0	0	112					1	0	0	1	0	0	1	1	147				
0	1	1	1	0	0	0	1	113					1	0	0	1	0	1	0	0	148				
0	1	1	1	0	0	1	0	114					1	0	0	1	0	1	0	1	149				
0	1	1	1	0	0	1	1	115					1	0	0	1	0	1	1	0	150				
0	1	1	1	0	1	0	0	116					1	0	0	1	0	1	1	1	151				
0	1	1	1	0	1	0	1	117					1	0	0	1	1	0	0	0	152				
0	1	1	1	0	1	1	0	118					1	0	0	1	1	0	0	1	153				
0	1	1	1	0	1	1	1	119					1	0	0	1	1	0	1	0	154				
0	1	1	1	1	0	0	0	120					1	0	0	1	1	0	1	1	155				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12	15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

TTL MEMORY 93406

Input								Word	Output			
MSB A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	MSB O_3	O_2	O_1	O_0
1	0	0	1	1	1	0	0	156				
1	0	0	1	1	1	0	1	157				
1	0	0	1	1	1	1	0	158				
1	0	0	1	1	1	1	1	159				
1	0	1	0	0	0	0	0	160				
1	0	1	0	0	0	0	1	161				
1	0	1	0	0	0	1	0	162				
1	0	1	0	0	0	1	1	163				
1	0	1	0	0	0	0	0	164				
1	0	1	0	0	1	0	1	165				
1	0	1	0	0	1	1	0	166				
1	0	1	0	0	1	1	1	167				
1	0	1	0	1	1	0	0	168				
1	0	1	0	1	0	0	1	169				
1	0	1	0	1	0	1	0	170				
1	0	1	0	1	0	1	1	171				
1	0	1	0	1	1	0	0	172				
1	0	1	0	1	1	0	1	173				
1	0	1	0	1	1	1	0	174				
1	0	1	0	1	1	1	1	175				
1	0	1	1	0	0	0	0	176				
1	0	1	1	0	0	0	1	177				
1	0	1	1	0	0	1	0	178				
1	0	1	1	0	0	1	1	179				
1	0	1	1	0	1	0	0	180				
1	0	1	1	0	1	0	1	181				
1	0	1	1	0	1	1	0	182				
1	0	1	1	0	1	1	1	183				
1	0	1	1	1	0	0	0	184				
1	0	1	1	1	0	0	1	185				
1	0	1	1	1	0	1	0	186				
1	0	1	1	1	0	1	1	187				
1	0	1	1	1	1	0	0	188				
1	0	1	1	1	1	0	1	189				
1	0	1	1	1	1	1	0	190				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

								Word	Output			
MSB A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	MSB O_3	O_2	O_1	O_0
1	0	1	1	1	1	1	1	191				
1	1	0	0	0	0	0	0	192				
1	1	0	0	0	0	0	1	193				
1	1	0	0	0	0	1	0	194				
1	1	0	0	0	0	1	1	195				
1	1	0	0	0	1	0	0	196				
1	1	0	0	0	1	0	1	197				
1	1	0	0	0	1	1	0	198				
1	1	0	0	0	1	1	1	199				
1	1	0	0	1	0	0	0	200				
1	1	0	0	1	0	0	1	201				
1	1	0	0	1	0	1	0	202				
1	1	0	0	1	0	1	1	203				
1	1	0	0	1	1	0	0	204				
1	1	0	0	1	1	0	1	205				
1	1	0	0	1	1	1	0	206				
1	1	0	0	1	1	1	1	207				
1	1	0	1	0	0	0	0	208				
1	1	0	1	0	0	0	1	209				
1	1	0	1	0	0	1	0	210				
1	1	0	1	0	0	1	1	211				
1	1	0	1	0	1	0	0	212				
1	1	0	1	0	1	0	1	213				
1	1	0	1	0	1	1	0	214				
1	1	0	1	0	1	1	1	215				
1	1	0	1	1	0	0	0	216				
1	1	0	1	1	0	0	1	217				
1	1	0	1	1	0	1	0	218				
1	1	0	1	1	0	1	1	219				
1	1	0	1	1	1	0	0	220				
1	1	0	1	1	1	0	1	221				
1	1	0	1	1	1	1	0	222				
1	1	0	1	1	1	1	1	223				
1	1	1	0	0	0	0	0	224				
1	1	1	0	0	0	0	1	225				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

TTL MEMORY 93406

Input								Word	Output			
MSB									MSB			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	#	O_3	O_2	O_1	O_0
1	1	1	0	0	0	1	0	226				
1	1	1	0	0	0	1	1	227				
1	1	1	0	0	1	0	0	228				
1	1	1	0	0	1	0	1	229				
1	1	1	0	0	1	1	0	230				
1	1	1	0	0	1	1	1	231				
1	1	1	0	1	0	0	0	232				
1	1	1	0	1	0	0	1	233				
1	1	1	0	1	0	1	0	234				
1	1	1	0	1	0	1	1	235				
1	1	1	0	1	1	0	0	236				
1	1	1	0	1	1	0	1	237				
1	1	1	0	1	1	1	0	238				
1	1	1	0	1	1	1	1	239				
1	1	1	1	0	0	0	0	240				
1	1	1	1	0	0	0	1	241				
1	1	1	1	0	0	1	0	242				
1	1	1	1	0	0	1	1	243				
1	1	1	1	0	1	0	0	244				
1	1	1	1	0	1	0	1	245				
1	1	1	1	0	1	1	0	246				
1	1	1	1	0	1	1	1	247				
1	1	1	1	1	0	0	0	248				
1	1	1	1	1	0	0	1	249				
1	1	1	1	1	0	1	0	250				
1	1	1	1	1	0	1	1	251				
1	1	1	1	1	1	0	0	252				
1	1	1	1	1	1	0	1	253				
1	1	1	1	1	1	1	0	254				
1	1	1	1	1	1	1	1	255				
15	1	2	3	4	7	6	5	Pkg. Pin #	9	10	11	12

Customers Authorizing Signature ____________________

Date ____________________

Qualified FSC Representative ____________________

Date ____________________

TTL MEMORY 93407 • 93433

16-BIT COINCIDENT SELECT READ/WRITE MEMORY

FORMERLY 5033 • 9033

DESCRIPTION – These devices are Planar* epitaxial integrated 16-bit, bit-oriented, non-destructive readout memory cells, compatible with Fairchild TTL. These memory cells, organized as 16 words by one bit, are designed for high speed scratch-pad memory applications. The 93407 and 93433 are electrically identical, but with different pin configurations. Both devices are available in two fan out options, 40 mA (A) and 20 mA (B) for Industrial/Commercial temperature range.

OPERATION – The memory cell consists of 16 RS flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "H" level (>2.1 volts) and holding the non-selected address lines at logic "L" level (<0.7 volts). As many as four locations may be addressed simultaneously without destroying stored information. The stored data and its complement at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the $\overline{S_1}$ output will be LOW and the $\overline{S_0}$ output will be HIGH. If the addressed bit location contains a "0", the $\overline{S_1}$ otuput will be HIGH and the $\overline{S_0}$ output will be LOW.

Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a HIGH level. To write a "0", the input of the "write zero" (W_0) amplifier is raised to a HIGH Level.

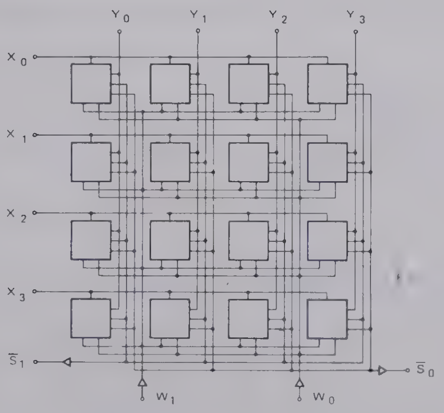
The outputs are open-collector, which may be wired OR for word expansion. (The output transistors are off when none of the bits are selected.) An external resistor should be returned to V_{CC} to pull-up the wired OR outputs.

- **TTL COMPATIBLE**
- **OUTPUT WIRED-OR CAPABILITY**
- **TRUE AND COMPLEMENTARY OUTPUTS ARE PROVIDED**
- **NON DESTRUCTIVE READ OUT**
- **FAN OUT AVAILABLE IN TWO GRADES: A = 40 mA, B = 20 mA FOR INDUSTRIAL/COMMERCIAL TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground	–0.5 V to +8.0 V
Input Pin Voltage	–1.5 V to +5.5 V
Current Into Output Terminal	100 mA
Output Voltage	–0.5 V to +8.0 V

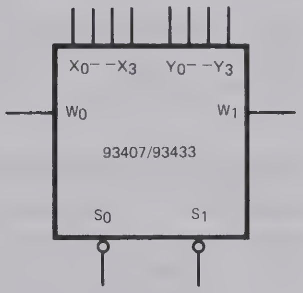
LOGIC DIAGRAM



X,Y – Address
W – Write Input
S – Sense Output

Each square represents one bit of storage.

LOGIC SYMBOL

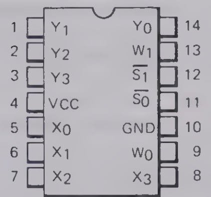


93407
V_{CC} = Pin 4
GND = Pin 10

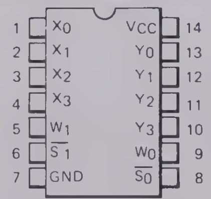
93433
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)*

93407



93433



X, Y – ADDRESS
W – WRITE INPUT
S – SENSE OUTPUT

*Pin connection is same for all packages.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%) (Part No. 93407/BXM, 93433/BXM)**

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	V_{CC} = 5.5 V, V_X = 0V, V_Y = 4.5 V, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	V_{CC} = 5.5 V, V_Y = 0 V, V_X = 4.5 V, other Y inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	V_{CC} = 5.5 V, V_X = 4.5 V, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	V_{CC} = 5.5 V, V_Y = 4.5 V, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	V_{CC} = 5.5 V, V_W = 0 V
I_{RW}	Write Input Leakage Current		100	μA	V_{CC} = 5.5 V, V_W = 4.5 V
I_{CC}	Power Supply Current		65	mA	V_{CC} = 5.5 V, All Inputs Grounded
I_{BV}	Power Supply Current at V_{CC} = 7 V		84	mA	V_{CC} = 7.0 V, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	V_{CC} = 5.5 V, V_{CEX} = 5.5 V, all inputs grounded
V_{OL}	Output LOW Voltage		0.40	V	V_{CC} = 4.5 V, One Bit Selected I_{OL} = 20 mA
$V_{XY(W)}$	Address Input Threshold to Prevent Writing		0.75	V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{XY(W)}$	Address Input Threshold to Insure Writing	2.1		V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{XY(R)}$	Address Input Threshold to Prevent Reading		0.8	V	V_{CC} = 5.0 V, other inputs grounded. Both outputs must be on HIGH state.
$V_{XY(R)}$	Address Input Threshold to Insure Reading	2.1		V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		0.8	V*	V_{CC} = 5.0 V, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume LOW state. If W_1 is pulsed, S_1 will assume LOW state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.1		V*	V_{CC} = 5.0 V, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume LOW state. If W_1 is pulsed, S_0 will assume LOW state.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%) (Part No. 93407/AXC, 93407/BXC, 93433/AXC, 93433/BXC)**

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	V_{CC} = 5.25 V, V_X = 0V, V_Y = 4.5 V, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	V_{CC} = 5.25 V, V_Y = 0 V, V_X = 4.5 V, other X inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	V_{CC} = 5.25 V, V_X = 4.5 V, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	V_{CC} = 5.25 V, V_Y = 4.5 V, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	V_{CC} = 5.25 V, V_W = 0 V
I_{RW}	Write Input Leakage Current		100	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{CC}	Power Supply Current		65	mA	V_{CC} = 5.25 V, All Inputs Grounded
I_{BV}	Power Supply Current at V_{CC} = 7 V		95	mA	V_{CC} = 7.0 V, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	V_{CC} = 5.25 V, V_{CEX} = 5.5 V, all inputs grounded
V_{OL}	Output LOW Voltage		0.45	V	V_{CC} = 4.75 V, One bit selected I_{OL} = 20 mA for IND B grade. I_{OL} = 40 mA for IND A grade.
$V_{XY(W)}$	Address Input Threshold to Prevent Writing		0.8	V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{XY(W)}$	Address Input Threshold to Insure Writing	2.0		V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{XY(R)}$	Address Input Threshold to Prevent Reading		1.0	V	V_{CC} = 5.0 V, other inputs grounded. Both outputs must be on HIGH state.
$V_{XY(R)}$	Address Input Threshold to Insure Reading	2.0		V*	V_{CC} = 5.0 V, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		1.0	V*	V_{CC} = 5.0 V, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume LOW state. If W_1 is pulsed, S_1 will assume LOW state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.0		V*	V_{CC} = 5.0 V, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume LOW state. If W_1 is pulsed, S_0 will assume LOW state.

*Amplitude of the pulse ≥2.5 V, pulse width ≥100 ns. The cell state is determined 35 ns after pulse disappears.

**X = package type; F for Flatpak, D for Ceramic Dip. See Packaging Information Section for packages available on this product.

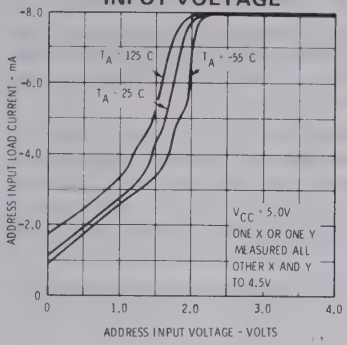
TTL LOADING RULES

	HIGH LEVEL	LOW LEVEL
Address Input	6.5 U.L.	6.5 U.L.
Write Input	1.5 U.L.	0.9 U.L.
Sense Output	Open Collector	IND A grade = 25 U.L. MIL or IND B grade = 12.5 U.L.

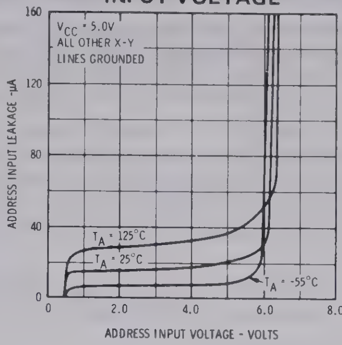
1 Unit Load (U.L.) = 60 μA HIGH/1.6 mA LOW

TYPICAL ELECTRICAL CHARACTERISTICS

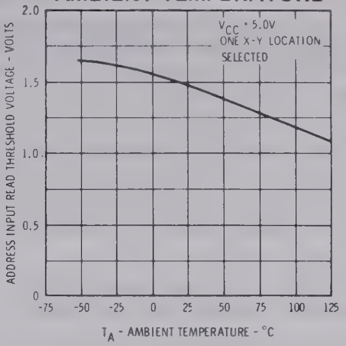
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



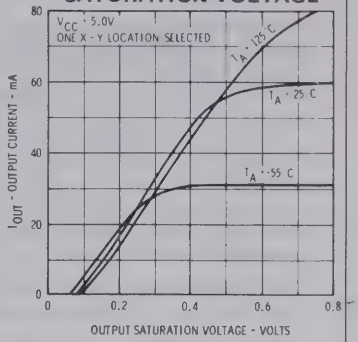
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



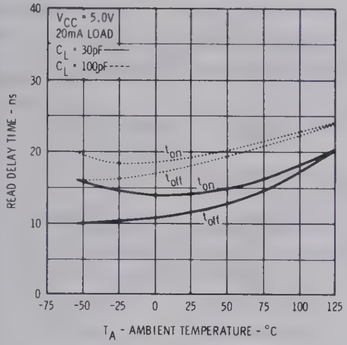
ADDRESS INPUT READ THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



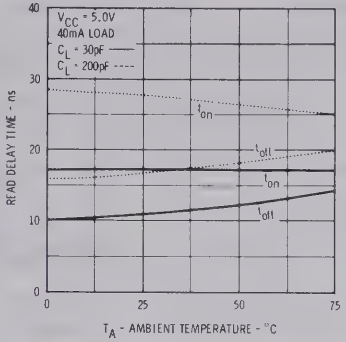
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



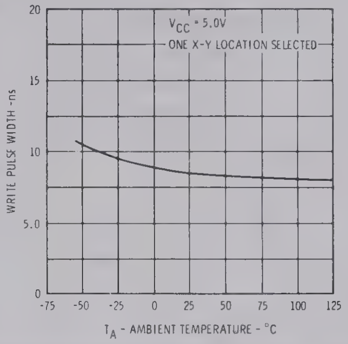
READ DELAY VERSUS AMBIENT TEMPERATURE 20 mA LOAD



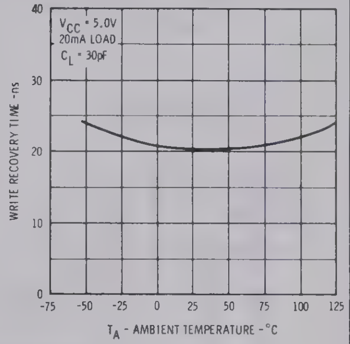
READ DELAY VERSUS AMBIENT TEMPERATURE 40 mA LOAD



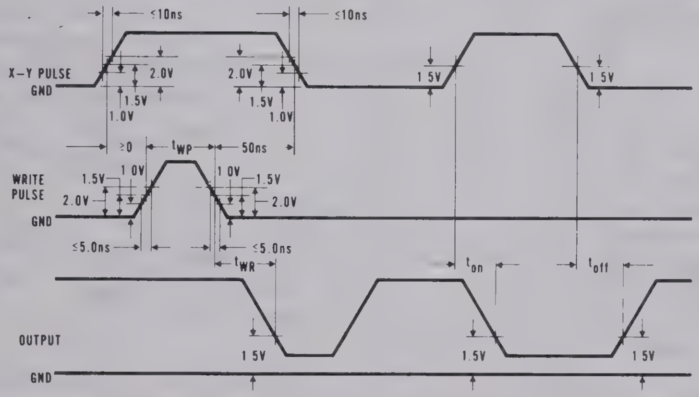
WRITE PULSE WIDTH VERSUS AMBIENT TEMPERATURE

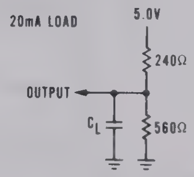


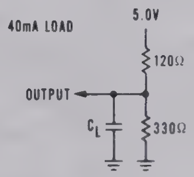
WRITE RECOVERY TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS


≤10ns
≤10ns
X–Y PULSE
GND
2.0V
1.5V
1.0V
2.0V
1.5V
1.0V
1.5V
1.5V
≥0
t_{WP}
50ns
WRITE PULSE
1.5V
1.0V
2.0V
1.0V
1.5V
2.0V
GND
≤5.0ns
≤5.0ns
t_{WR}
t_{on}
t_{off}
OUTPUT
1.5V
1.5V
1.5V
GND


20mA LOAD
5.0V
240Ω
OUTPUT
C_L
560Ω


40mA LOAD
5.0V
120Ω
OUTPUT
C_L
330Ω

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, One X-Y Location Selected.)

SYMBOL	PARAMETER	MIL B GRADE MIN.	MIL B GRADE MAX.	IND A GRADE MIN.	IND A GRADE MAX.	IND B GRADE MIN.	IND B GRADE MAX.	UNITS	CONDITIONS LOAD (mA)	CONDITIONS C_L (pF)
t_{WP}	Write Pulse Width			25				ns	40	
		25				25			20	
t_{WR}	Write Recovery Time				35			ns	40	30
			40				35		20	30
t_{on}	Turn On Delay				20			ns	40	30
					30				40	200
			25				20		20	30
			35				30		20	100
t_{off}	Turn Off Read Delay				20			ns	40	30
					30				40	200
			25				20		20	30
			35				30		20	100

APPLICATION:

A memory utilizing these memory cells may have any desired word length. The number of words in the memory is a multiple of four words. The following example of a 64 word memory illustrates how a number of 16-bit memory cells may be used to construct a typical memory.

The 64 word memory as shown in Figure A consists of groups of four memory cells. Each of the groups of four memory cells supplies one bit for each of the 64 words stored in the memory. All bits belonging to one word are stored in the same address location. Therefore, the address of a word in the memory is the address of each bit of the addressed word in the groups of four memory cells. The equal outputs of the four memory cells are tied together so that each group of four memory cells has one HIGH and one LOW level output.

The six memory address lines from an external source are decoded at the first level with two 9301 decoders. The fourth input to each of the two decoders can be used as an enable control input to the 64 word memory. If the address enable is at a LOW logic level, one and only one of the eight outputs, 0 to 7, in the illustration assumes a LOW logic level. If the address enable is at a HIGH logic level, the outputs 0 to 7 of the two decoders assume a HIGH logic level, thus none of the 64 words stored in the memory is addressed. The outputs, 0 to 7, of the two decoders serve as X-and-Y address lines. The output signals of the decoders are connected to driving transistors which provide the necessary current to address the memory cells.

The example given above is only one of the many organizations and is presented as an illustration. Obviously many address decoding schemes may be utilized depending on memory size, driver fan out, decoder fan out, wiring, heat dissipation, etc.

Figures B through D show alternative schemes to enter data into the memory cell.

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64 WORD MEMORY

Fig. A

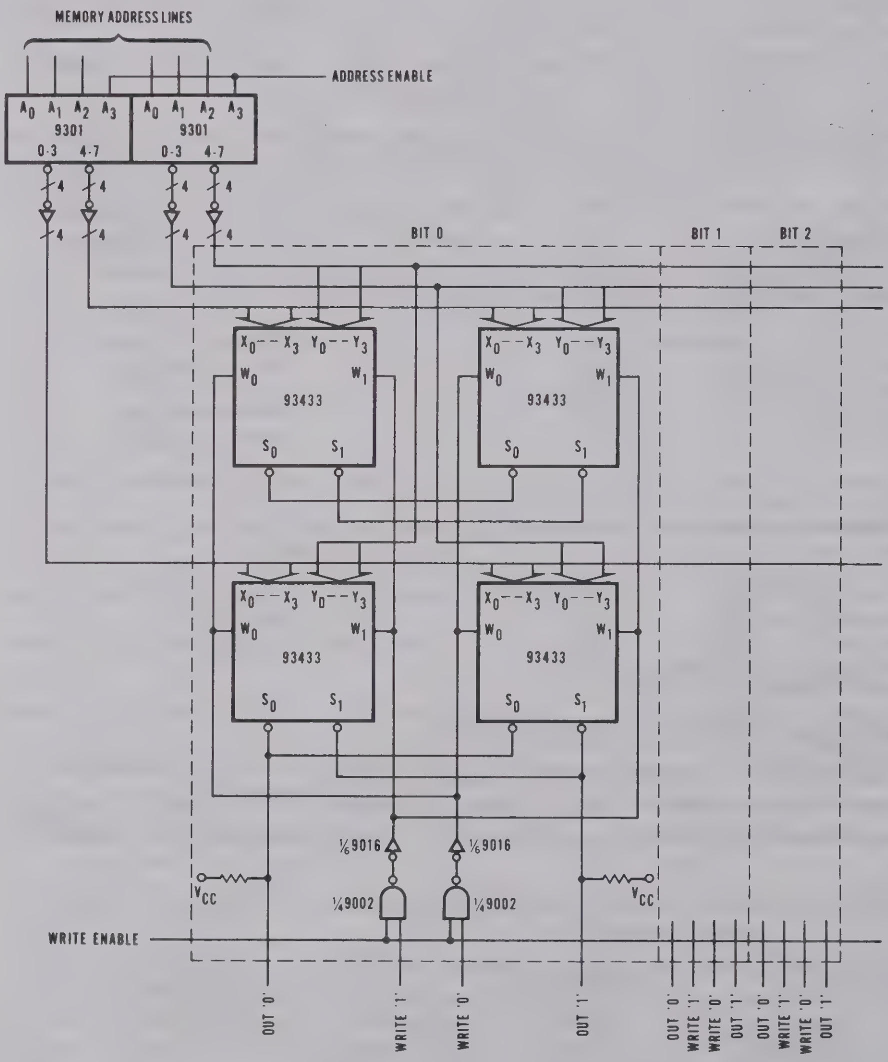

MEMORY ADDRESS LINES
ADDRESS ENABLE
A0 A1 A2 A3
9301
0-3 4-7
A0 A1 A2 A3
9301
0-3 4-7
4
BIT 0
BIT 1
BIT 2
X0 - - X3 Y0 - - Y3
W0
W1
93433
S0
S1
1/6 9016
1/6 9016
1/4 9002
1/4 9002
VCC
VCC
WRITE ENABLE
OUT '0'
WRITE '1'
WRITE '0'
OUT '1'
OUT '0'
WRITE '1'
WRITE '0'
OUT '1'
OUT '0'
WRITE '1'
WRITE '0'
OUT '1'

Fig. B

DOUBLE RAIL ACTIVE LOW INPUTS AND ENABLE

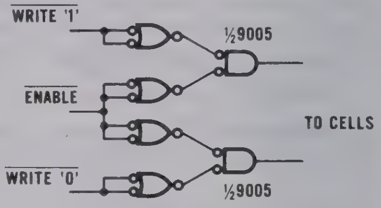

WRITE '1'
½9005
ENABLE
TO CELLS
WRITE '0'
½9005

Fig. C

SINGLE RAIL ACTIVE HIGH INPUT AND ENABLE

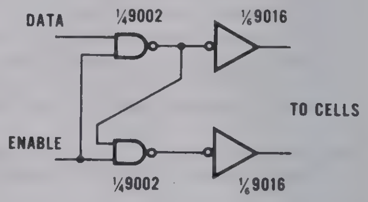
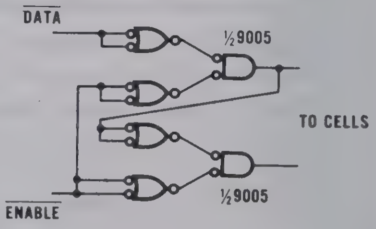

DATA
¼9002
⅙9016
TO CELLS
ENABLE
¼9002
⅙9016

Fig. D

SINGLE RAIL ACTIVE LOW INPUT AND ENABLE


DATA
½9005
TO CELLS
½9005
ENABLE

TTL ISOPLANAR MEMORY 93410 · 93410A

256-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION — The 93410 and 93410A are high speed 256 Bit TTL Random Access Memories with full decoding on chip. Each memory, organized as 256 words x 1 bit, is designed for scratch pad, buffer and distributed main memory applications. Both devices have three chip select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.

The 93410A is a high speed version of the 93410, offering a 35 ns access time.

- **ORGANIZATION – 256 WORDS X 1 BIT**
- **THREE HIGH SPEED CHIP SELECT INPUTS**
- **TYPICAL ACCESS TIME**

93410A	**Commercial**	**35 ns**
93410	**Commercial**	**45 ns**
93410	**Military**	**45 ns**

- **NON INVERTED DATA OUTPUT**
- **ON CHIP DECODING**
- **POWER DISSIPATION – 1.8 mW/BIT**
- **POWER DISSIPATION DECREASES WITH TEMPERATURE**

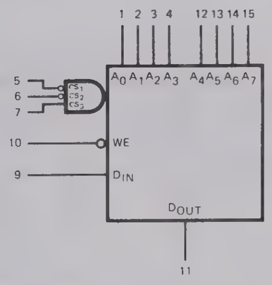
PIN NAMES		**LOADING (Notes a & b)**
$\overline{CS}_1$ $\overline{CS}_2$ CS_3	Chip Select Input	0.5 U.L.
A_0 thru A_7	Address Inputs	0.5 U.L.
D_{IN}	Data Input	0.5 U.L.
D_{OUT}	Data Output	10 U.L.
$\overline{WE}$	Write Enable	0.5 U.L.

NOTES:

a. 1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW

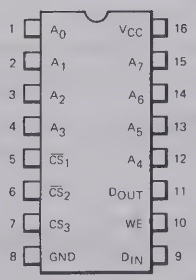
b. 10 U.L. is the output LOW drive factor. An external pull up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at $V_{out} = 0.45$ V.

LOGIC SYMBOL

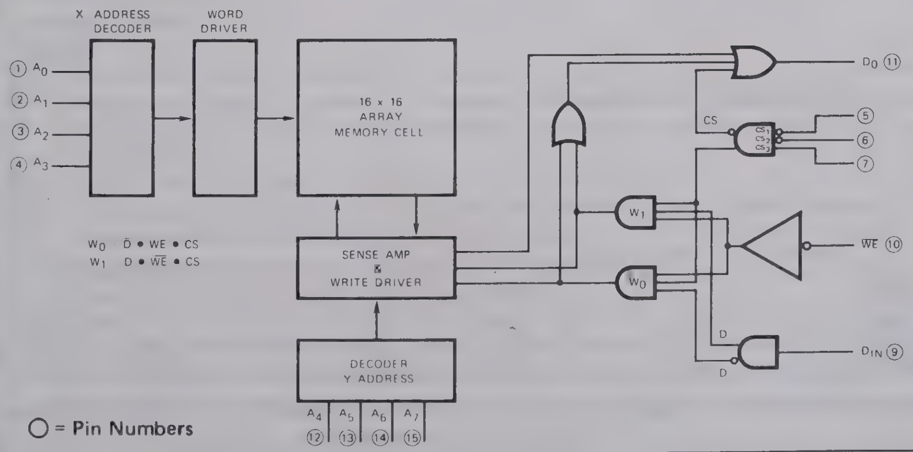

1 2 3 4
12 13 14 15
A0 A1 A2 A3 A4 A5 A6 A7
5
6
7
CS1
CS2
CS3
10
WE
9
DIN
DOUT
11

V_{CC} = Pin 16
Gnd = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)


1 A0
2 A1
3 A2
4 A3
5 CS1
6 CS2
7 CS3
8 GND
16 VCC
15 A7
14 A6
13 A5
12 A4
11 DOUT
10 WE
9 DIN

LOGIC DIAGRAM


X ADDRESS DECODER
WORD DRIVER
① A0
② A1
③ A2
④ A3
16 x 16 ARRAY MEMORY CELL
SENSE AMP & WRITE DRIVER
DECODER Y ADDRESS
A4 ⑫
A5 ⑬
A6 ⑭
A7 ⑮
W0 D̄ • WE • CS
W1 D • W̄Ē • CS
D0 ⑪
CS
CS1
CS2
CS3
⑤
⑥
⑦
W1
W0
WE ⑩
D
D
DIN ⑨
○ = Pin Numbers

FUNCTIONAL DESCRIPTION

The 93410 and 93410A are fully decoded 256-bit Random Access Memories organized 256 words by 1 bit. Bit selection is achieved by means of an 8-bit address, A_0 thru A_7.

Three chip select inputs are provided, two are active LOW ($\overline{CS}_1$ and $\overline{CS}_2$) and the third active HIGH (CS_3) for maximum logic flexibility. This permits memory array expansion up to 2048 words without the need for additional external decoders. For larger memories the fast chip select access time permits the decoding of chip select, CS, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable $\overline{WE}$ (pin 10). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93410s or 93410As can be tied together. In other applications the wired-OR is not used. In either case an external pull up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}\,(MAX)}{16 - F.O.\,(1.6)} \leqslant R_L \leqslant \frac{V_{CC}\,(MIN) - V_{OH}}{N\,(I_{CEX}) + F.O.\,(0.04)}$$

R_L is in kΩ

N = number of wired-OR outputs tied together

F.O. = number of TTL Unit Loads (U.L.) driven

I_{CEX} = Memory Output Leakage Current in mA

V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	MODE
CS			$\overline{WE}$	DI	DO	
PIN 5	PIN 6	PIN 7				
H	X	X	X	X	H	Not Selected
X	H	X	X	X	H	Not Selected
X	X	L	X	X	H	Not Selected
L	L	H	L	L	H	Write "0"
L	L	H	L	H	H	Write "1"
L	L	H	H	X	DO	Read data from addressed location

H = HIGH Voltage

L = LOW Voltage

X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	0.5 V to +5.50 V
Output Current (dc) (Output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE[4]
	MIN.	TYP.	MAX.	
93410XC, 93410AXC	4.75 V	5.0 V	5.25 V	0°C to 75°C
93410XM	4.75 V	5.0 V	5.25 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE[1] (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS[2]			UNITS	CONDITIONS	
			MIN.	TYP.[3]	MAX.			
V_{OL}	Output LOW Voltage			0.3	0.45	V		V_{CC} = MIN I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage		2.0	1.6		V		Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			1.5	0.85	V		Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current			–530	–800	μA		V_{CC} = MAX., V_{IN} = 0 V
I_{IH}	Input HIGH Current			1.0	20	μA		V_{CC} = MAX., V_{IN} = 4.5 V
I_{CEX}	Output Leakage Current			1.0	50	μA		V_{CC} = MAX., V_{OUT} = 4.5 V
V_{CD}	Input Clamp Diode Voltage			–1.0	–1.5	V		V_{CC} = MAX., I_{IN} = –10 mA
I_{CC}	Power Supply Current	93410XC		90	135	mA	$T_A \geqslant 25°C$	V_{CC} = MAX. All inputs grounded See Power Supply vs Temp. Curve
				100	140		$T_A < 25°C$	
		93410XM		90	135		$T_A \geqslant 25°C$	
				100	145		$T_A < 25°C$	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

SYMBOL	PARAMETER	93410AXC			93410XC			93410XM			UNITS	CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Access Time		20	24		25	30		25	40	ns	See Test Circuit[5]
t_{RCS}	Chip Select Recovery Time		20	25		25	32		25	40	ns	
t_{AA}	Address Access Time		35	45		45	60		45	70	ns	
WRITE MODE	DELAY TIMES											
t_{WS}	Write Disable Time	10	20	35	10	20	40	10	20	50	ns	
t_{WR}	Write Recovery Time		25	35		25	40		25	50	ns	
	INPUT TIMING REQUIREMENTS											
t_W	Minimum Write Pulse Width	30	20		30	25		40	25		ns	See Test Circuit
t_{WSD}	Data Set-up Time Prior to Write	5	0		5	0		5	0		ns	
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		ns	
t_{WSA}	Address Set-up Time	5	0		5	0		5	0		ns	
t_{WSCS}	Chip Select Set-up Time	5	0		5	0		5	0		ns	
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		ns	
C_{IN}	Input Pin Capacitance			4.0			4.0			4.0	pF	Measured with a pulse technique
C_{OUT}	Output Pin Capacitance			8.0			8.0			8.0	pF	

NOTES:

(1) Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.

(2) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(3) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

(4) Guaranteed with transverse airflow exceeding 400 linear F.P.M. and 2 minute warm up.

Typical thermal resistance values of the package are:

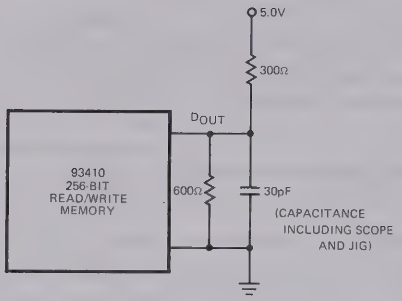
θ_{JA} (Junction to Ambient) = 50°C / W (at 400 F.P.M. Airflow)
θ_{JA} (Junction to Ambient) = 90°C / W (Still Air)
θ_{JL} (Junction to Case) = 25°C / W

The –55°C Operating Temperature relates to a –30°C worst case cold Junction Temperature.

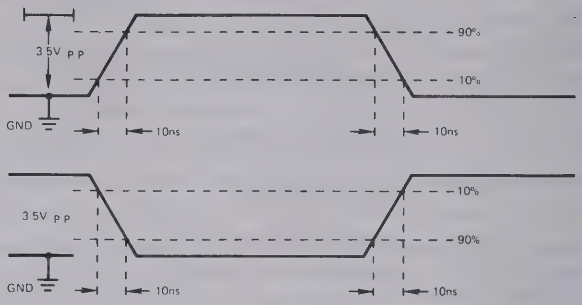
(5) The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudo random testing pattern.

93410 AC TEST LOAD AND WAVEFORM

LOADING CONDITION


5.0V
300Ω
DOUT
93410
256-BIT
READ/WRITE
MEMORY
600Ω
30pF
(CAPACITANCE
INCLUDING SCOPE
AND JIG)

INPUT PULSES

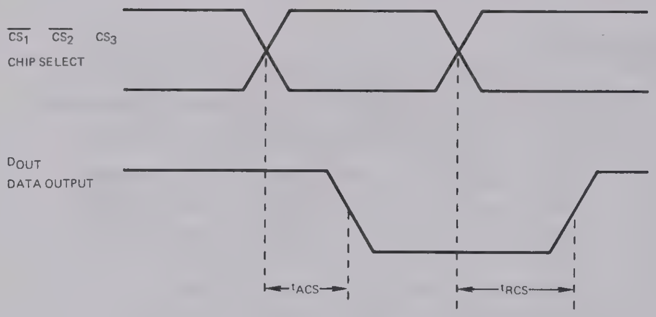

3.5V P P
GND
90%
10%
10ns
10ns
3.5V P P
GND
10%
90%
10ns
10ns

(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

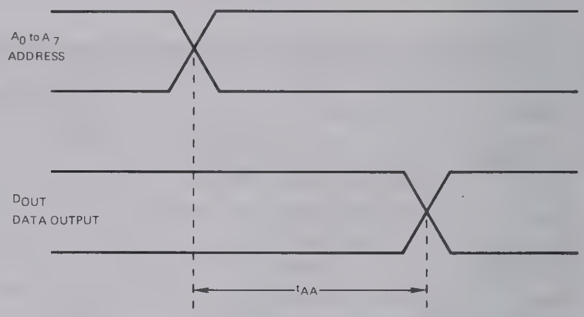
SWITCHING WAVEFORMS

READ MODE

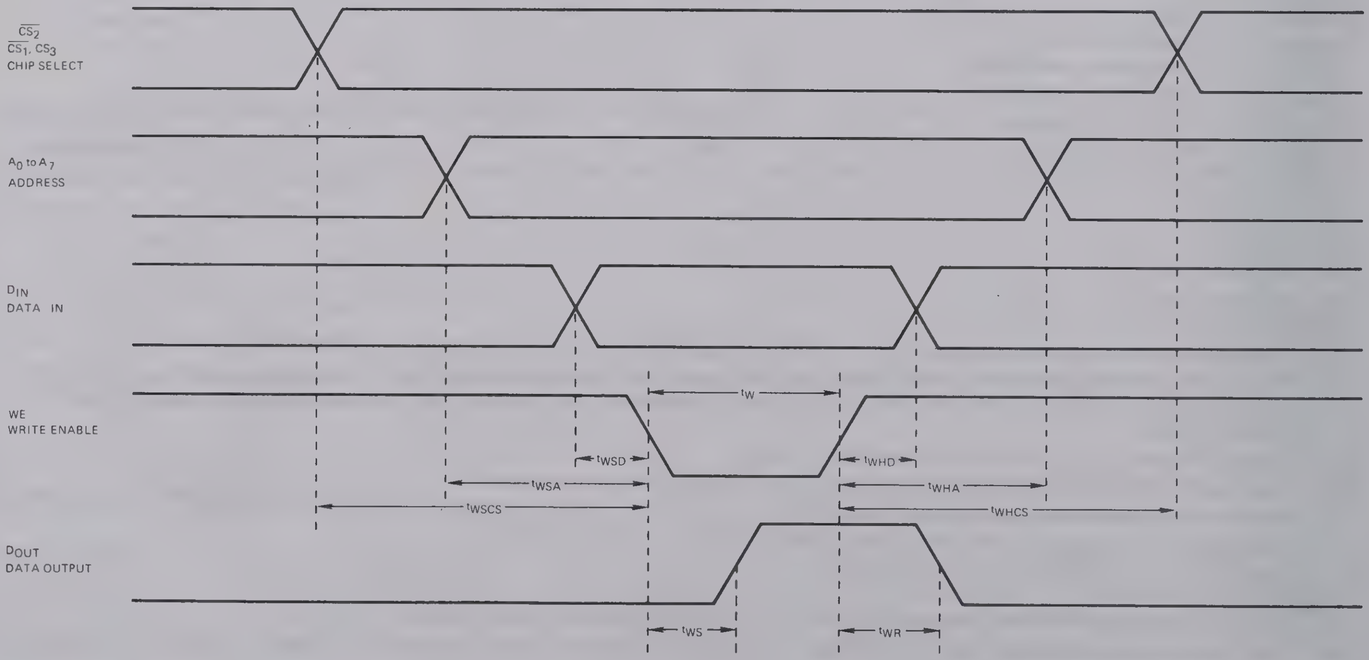
PROPAGATION DELAY FROM CHIP SELECT


$\overline{CS_1}$ $\overline{CS_2}$ CS_3
CHIP SELECT
DOUT
DATA OUTPUT
tACS
tRCS

PROPAGATION DELAY FROM ADDRESS

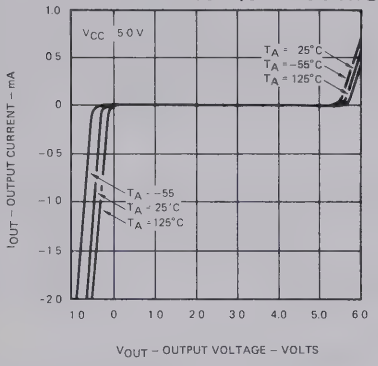

A0 to A7
ADDRESS
DOUT
DATA OUTPUT
tAA

WRITE MODE

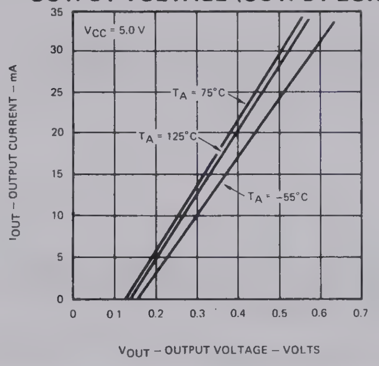

$\overline{CS_2}$
$\overline{CS_1}$, CS_3
CHIP SELECT
A0 to A7
ADDRESS
DIN
DATA IN
WE
WRITE ENABLE
tW
tWSD
tWHD
tWSA
tWHA
tWSCS
tWHCS
DOUT
DATA OUTPUT
tWS
tWR

TYPICAL ELECTRICAL CHARACTERISTICS

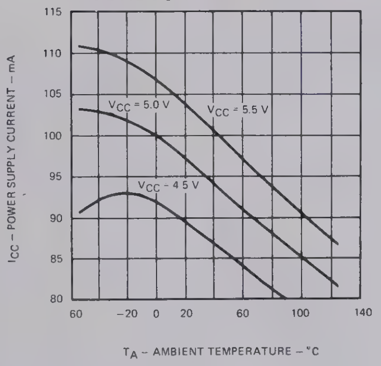
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



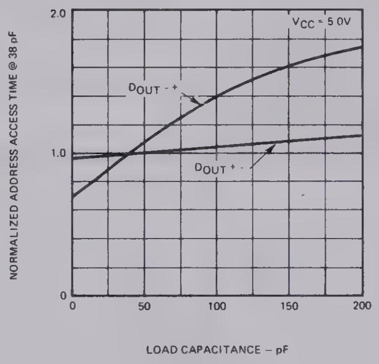
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



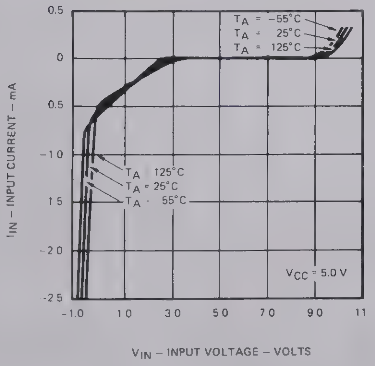
POWER SUPPLY CURRENT VERSUS TEMPERATURE



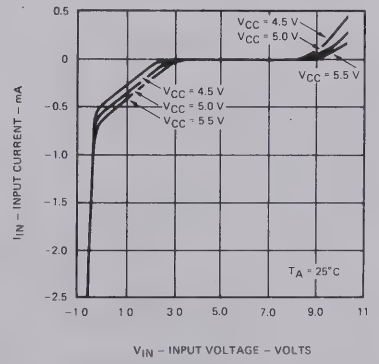
NORMALIZED ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE



TTL ISOPLANAR MEMORY 93415

1024-BIT FULLY DECODED RANDOM ACCESS MEMORY

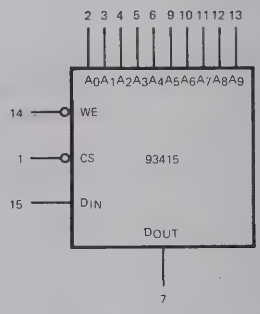
DESCRIPTION — The 93415 is a 1024-Bit Read/Write Random Access Memory organized 1024 words x 1-bit. It has a typical access time of 60 ns and is designed for buffer and control storage and high performance main memory applications.

The 93415 includes full decoding on the chip, has separate data input and data output lines and an active LOW chip select line.

The device is fully compatible with standard DTL and TTL logic families and has an uncommitted collector output for ease of memory expansion.

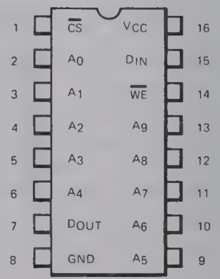
- **NON-INVERTING DATA OUTPUTS**
- **ORGANIZED 1024 WORDS X 1-BIT**
- **READ ACCESS TIME 60 ns TYP.**
- **CHIP SELECT ACCESS TIME 30 ns TYP.**
- **POWER DISSIPATION 0.5 mW/BIT TYP.**
- **INPUT LOADING 0.25 TTL UNIT LOADS**
- **UNCOMMITTED COLLECTOR OUTPUT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **TTL COMPATIBLE**

LOGIC SYMBOL


2 3 4 5 6 9 10 11 12 13
$A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9$
14
WE
1
CS
93415
15
D_{IN}
D_{OUT}
7

V_{CC} = PIN 16
GND = PIN 8

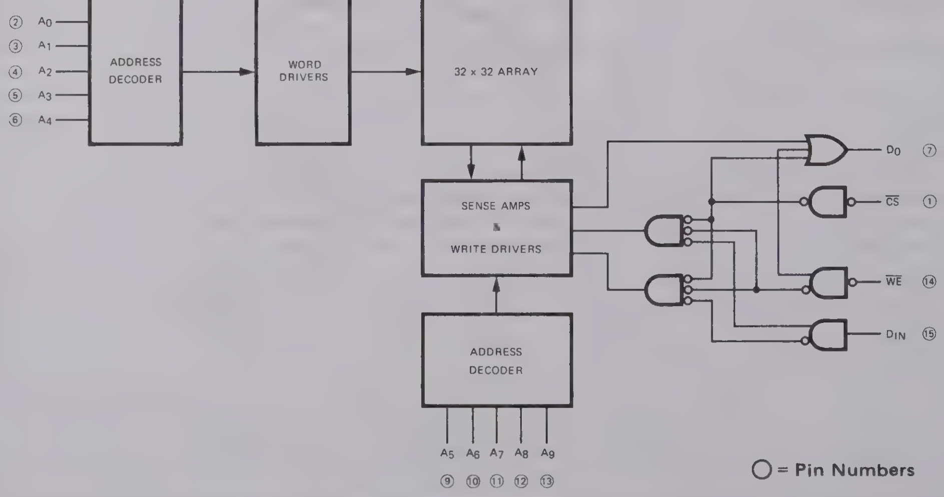
CONNECTION DIAGRAM DIP (TOP VIEW)


1 $\overline{CS}$
2 A_0
3 A_1
4 A_2
5 A_3
6 A_4
7 D_{OUT}
8 GND
16 V_{CC}
15 D_{IN}
14 $\overline{WE}$
13 A_9
12 A_8
11 A_7
10 A_6
9 A_5

PIN NAMES		LOADING
$\overline{CS}$	Chip Select	0.25 U.L.
A_0 to A_9	Address Inputs	0.25 U.L.
$\overline{WE}$	Write Enable	0.25 U.L.
D_{IN}	Data Input	0.25 U.L.
D_{OUT}	Data Output	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM


② A_0
③ A_1
④ A_2
⑤ A_3
⑥ A_4
ADDRESS DECODER
WORD DRIVERS
32 x 32 ARRAY
SENSE AMPS & WRITE DRIVERS
ADDRESS DECODER
A_5 A_6 A_7 A_8 A_9
⑨ ⑩ ⑪ ⑫ ⑬
D_O ⑦
$\overline{CS}$ ①
$\overline{WE}$ ⑭
D_{IN} ⑮
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The 93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by 1-bit. Bit selection is achieved by means of a 10-bit address A_0 to A_9.

One chip select input is provided for memory array expansion with the need for one additional external decoder. For larger memories the fast chip select access time permits the decoding of chip select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable $\overline{WE}$ (pin 14). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

Uncommitted collector outputs are provided on the 93415 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415 can be tied together. In other applications the wired-OR is not used. In either case an external pull up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}\,(\min)}{I_{OL} - F.O.\,(1.6)} \leqslant R_L \leqslant \frac{V_{CC}\,(\min) - V_{OH}}{N\,(I_{CEX}) + F.O.\,(0.04)}$$

R_L is in kΩ
N = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

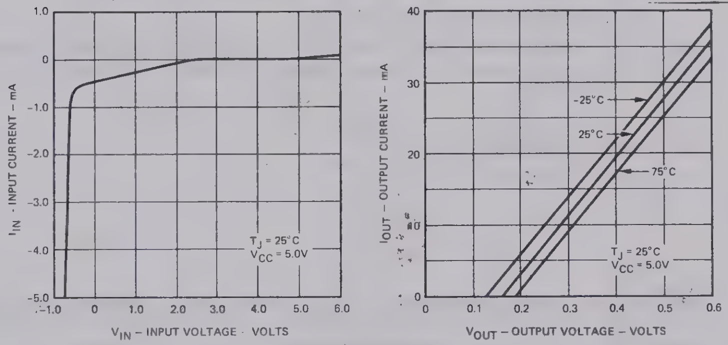
The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TABLE I — TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DI	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_0	READ

H = HIGH Voltage
L = LOW Voltage
X = Don't Care (HIGH or LOW)

TYPICAL INPUT AND OUTPUT CHARACTERISTICS



INPUT CURRENT VERSUS INPUT VOLTAGE

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to + 75°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
*Input Voltage (dc)	−0.5V to +5.5V
*Input Current (dc)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	0.5 V to +4.50V
Output Current (dc) (Output LOW)	+20 mA

*Either input voltage or input current limit is sufficient to protect the input.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (Note 4)
	MIN.	TYP.	MAX.	
93415XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

TO BE ANNOUNCED

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP. (Note 3)	MAX.			
V_{OL}	Output LOW Voltage		0.3	0.45	Volts	V_{CC} = MIN., I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		Volts	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	Volts	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	20	μA	V_{CC} = MAX., V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	50	μA	V_{CC} = MAX., V_{OUT} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	Volts	V_{CC} = MAX., I_{IN} = −10 mA	
I_{CC}	Power Supply Current		90	130	mA	$T_A \geqslant 25^\circ$C	V_{CC} = MAX., All inputs grounded
			110	150	mA	$T_A < 25^\circ$C	

NOTES:

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
4. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 fpm air flow)
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JC} (Junction to Case) = 25°C/Watt
   The 100°C Operating Temperature relates to a "worst case" junction temperature of 125°C.
5. The maximum address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.

SWITCHING CHARACTERISTICS — OVER OPERATING TEMPERATURE AND VOLTAGE RANGES

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ MODE	**DELAY TIMES**					
t_{ACS}	Chip Select Access Time		30	55	ns	See Test Circuit and Waveforms on page 9-30 (Note 5)
t_{RCS}	Chip Select Recovery Time		30	55		
t_{AA}	Address Access Time		60	90		
WRITE MODE	**DELAY TIMES**					
t_{WS}	Write Disable Time		35	45	ns	See Test Circuit and Waveforms on page 9-30
t_{WR}	Write Recovery Time		45	65		
	INPUT TIMING REQUIREMENTS					
t_W	Minimum Write Pulse Width		30	55	ns	
t_{WSD}	Data Set-Up Time Prior to Write		0	5		
t_{WHD}	Data Hold Time After Write		0	5		
t_{WSA}	Address Set-Up Time		20	35		
t_{WHA}	Address Hold Time		0	5		
t_{WSCS}	Chip Select Set-Up Time		0	5		
t_{WHCS}	Chip Select Hold Time		0	5		
C_{IN}	Input Pin Capacitance		4	5	pF	
C_{OUT}	Output Pin Capacitance		7	8		

TTL MEMORY 93434

256-BIT READ-ONLY MEMORY

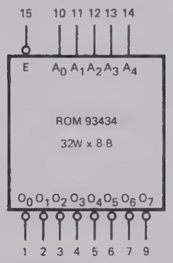
FORMERLY 9034

DESCRIPTION — The Fairchild 93434 is a 256-Bit bipolar TTL Read-Only Memory. The memory is organized as 32 words of eight bits each. The words are selected through five address lines. The eight outputs of the words are uncommitted collectors which may be wired-OR with the outputs of other ROMs. An Enable input is provided for additional decoding flexibility. A HIGH on the Enable input forces all outputs to be HIGH.

The contents of the memory are permanently programmed to customer order. A customer order form is available on request.

- **TTL COMPATIBLE**
- **OUTPUT WIRED-OR CAPABILITY**
- **SINGLE TTL LOAD INPUTS**
- **INPUT CLAMP DIODES**

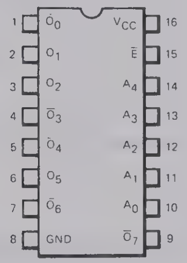
LOGIC SYMBOL



15
10 11 12 13 14
E
A0 A1 A2 A3 A4
ROM 93434
32W x 8-B
O0 O1 O2 O3 O4 O5 O6 O7
1 2 3 4 5 6 7 9

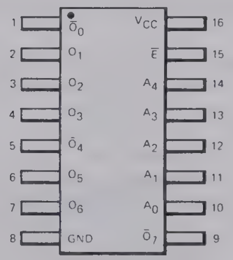
V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



1 Ō0
2 O1
3 O2
4 Ō3
5 Ō4
6 O5
7 Ō6
8 GND
VCC 16
Ē 15
A4 14
A3 13
A2 12
A1 11
A0 10
Ō7 9

FLATPAK (TOP VIEW)

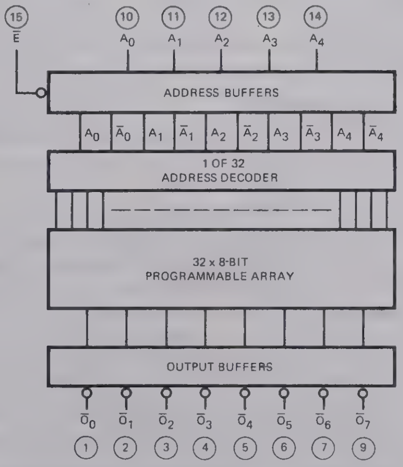


1 Ō0
2 O1
3 O2
4 O3
5 Ō4
6 O5
7 O6
8 GND
VCC 16
Ē 15
A4 14
A3 13
A2 12
A1 11
A0 10
Ō7 9

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5V to +8.0V
Input Pin Voltage	−1.5V to 5.5V
Current Into Output Terminal	100 mA
Output Voltages	−0.5 V to V_{CC} Value

LOGIC DIAGRAM



15 Ē
10 A0
11 A1
12 A2
13 A3
14 A4
ADDRESS BUFFERS
A0 Ā0 A1 Ā1 A2 Ā2 A3 Ā3 A4 Ā4
1 OF 32 ADDRESS DECODER
32 x 8-BIT PROGRAMMABLE ARRAY
OUTPUT BUFFERS
Ō0 Ō1 Ō2 Ō3 Ō4 Ō5 Ō6 Ō7
1 2 3 4 5 6 7 9

ELECTRICAL CHARACTERISTICS (T_A = –55°C to +125°C, V_{CC} = 5.0 V ±10%) (units are pulse tested) (Part No. 93434XM)*

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		–55°C		+25°C		+125°C			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_{FA}	Address Input Load Current		–1.6		–1.6		–1.6	mA	V_{CC} = 5.5 V V_A = 0.4 V
I_{FE}	Enable Input Load Current		–1.6		–1.6		–1.6	mA	V_{CC} = 5.5 V V_E = 0.4 V
I_{RA}	Address Input Leakage Current		100		100		100	µA	V_{CC} = 5.5 V V_A = 4.5 V
I_{RE}	Enable Input Leakage Current		100		100		100	µA	V_{CC} = 5.5 V V_E = 4.5 V
I_{CEX}	Output Leakage Current		200		200		200	µA	V_{CC} = 5.5 V V_{CEX} = 5.5 V Enable input to 2.0V
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V I_{OUT} = 10 mA The word containing a "0" bit is selected when performing this test.
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	V	V_{CC} = 5.5 V Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	V_{CC} = 4.5 V Enable input grounded. Monitor appropriate output to guarantee this test.
I_{CC}	Power Supply Current		80		80		80	mA	V_{CC} = 5.5 V All inputs grounded

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (units are pulse tested) (Part No. 93434XC)*

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		0°C		+25°C		+75°C			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_{FA}	Address Input Load Current		–1.6		–1.6		–1.6	mA	V_{CC} = 5.25 V V_A = 0.45 V
I_{FE}	Enable Input Load Current		–1.6		–1.6		–1.6	mA	V_{CC} = 5.25 V V_E = 0.45 V
I_{RA}	Address Input Leakage Current		100		100		100	µA	V_{CC} = 5.25 V V_A = 4.5 V
I_{RE}	Enable Input Leakage Current		100		100		100	µA	V_{CC} = 5.25 V V_E = 4.5 V
I_{CEX}	Output Leakage Current		200		200		200	µA	V_{CC} = 5.25 V V_{CEX} = 5.25 V Enable input to 2.0 V
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V I_{OUT} = 10 mA The word containing a "0" bit is selected when performing this test.
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	V_{CC} = 5.25 V Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	V_{CC} = 4.75 V Enable input grounded. Monitor appropriate output to guarantee this test.
I_{CC}	Power Supply Current		80		80		80	mA	V_{CC} = 5.25 V All inputs grounded

*X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

SWITCHING TIME CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{++}	Enable and Address Delay		*	50	ns	10 mA load. See Note 1.
t_{--}	Enable and Address Delay		*	50	ns	10 mA load. See Note 1.
t_{+-}	Address Delay		*	50	ns	10 mA load. See Note 2.
t_{-+}	Address Delay		*	50	ns	10 mA load. See Note 2.

*See Typical Electrical Characteristics curves.

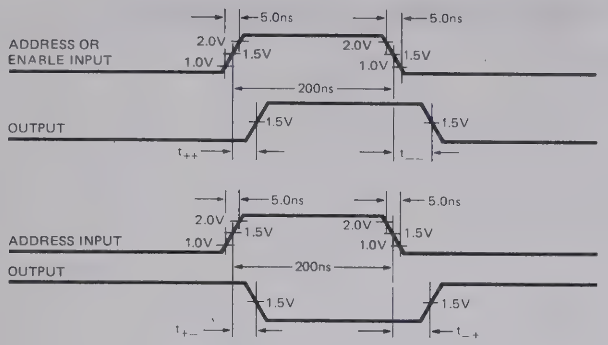
NOTES:

(1) To test Enable delay, apply input pulse to Enable input. The word selected must contain a "0" in the bit under test.

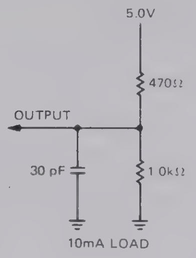
To test Address delay, the enable input must be low. Apply the input pulse to the Address input under test. The words selected must contain a "1" when input pulse is low and a "0" when input pulse is high in the bit under test.

(2) To test Address delay, the Enable input must be low. Apply the input pulse to the Address input under test. The words selected must contain a "0" when input pulse is low and a "1" when input pulse is high in the bit under test.

SWITCHING TIME TEST CONDITIONS AND WAVEFORMS


5.0ns
5.0ns
ADDRESS OR
ENABLE INPUT
2.0V
1.0V
1.5V
2.0V
1.0V
1.5V
200ns
OUTPUT
1.5V
1.5V
t++
t− −
5.0ns
5.0ns
2.0V
ADDRESS INPUT
1.0V
1.5V
2.0V
1.0V
1.5V
OUTPUT
200ns
1.5V
1.5V
t+−
t−+

SWITCHING TEST OUTPUT LOAD


5.0V
470Ω
OUTPUT
30 pF
1.0kΩ
10mA LOAD

LOADING RULES

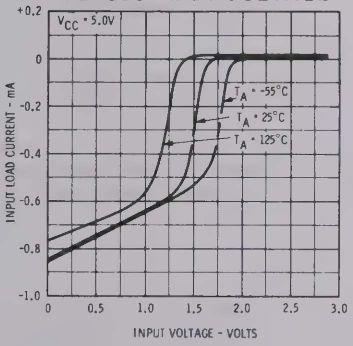
TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOADING	OUTPUTS	DRIVE FACTOR
LOW Level	1.7 U.L.	All outputs	$\frac{\text{Open Collector}}{6.25}$ U.L.
HIGH Level	1.0 U.L.		

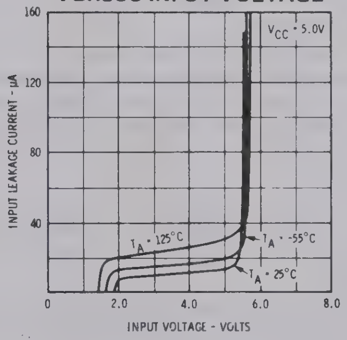
1 LOW Level TTL Unit Load (U.L.) = 1.6 mA
1 HIGH Level TTL Unit Load (U.L.) = 60 μA

TYPICAL ELECTRICAL CHARACTERISTICS

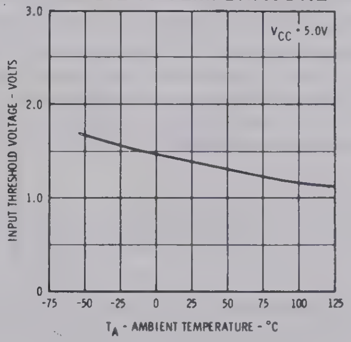
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



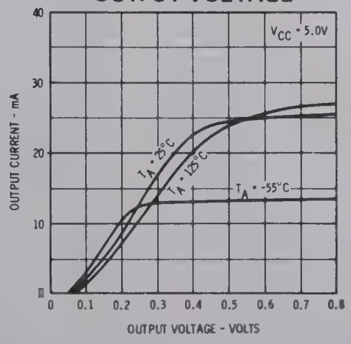
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



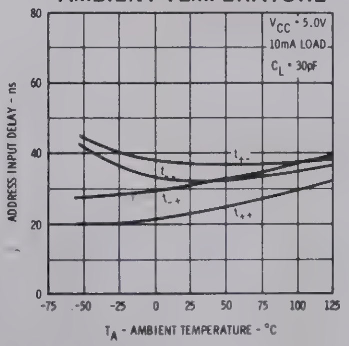
INPUT THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



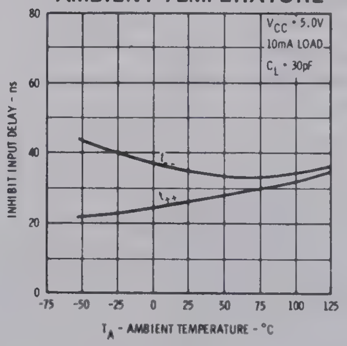
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



ADDRESS INPUT DELAY VERSUS AMBIENT TEMPERATURE



ENABLE INPUT DELAY VERSUS AMBIENT TEMPERATURE



TTL MEMORY 93435

64-BIT LINEAR SELECT READ/WRITE MEMORY

FORMERLY 9035

DESCRIPTION – The 93435 is a high speed 64-Bit Read/Write Memory Cell designed for use in high speed scratch pad memories. It is a linear select 16 word by 4-bit array.

The 93435 is available in the hermetically sealed 36-lead ceramic Dual In-Line package and will operate over the temperature range from −55°C to +125°C.

OPERATION – In addition to 16 address inputs, 4 data outputs, and 4 data inputs, the 93435 has a chip select and a write enable. When the chip select is HIGH, a word may be addressed by a HIGH on one of the address inputs. Data is written into the addressed word location only when the write enable is held LOW. While the address is present, the outputs continuously show the contents of the word selected. Readout is non-destructive.

Up to four words may be addressed and read simultaneously with the OR function of each bit appearing at the outputs. Data can be written into two locations simultaneously.

Uncommitted collector outputs are provided on the 93435 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93435's can be tied together. In other applications the wired-OR is not used. In either case an external pullup resistor of value R must be used to provide a HIGH at the output when it is off. Any value of R within the range specified below may be used.

$$\frac{5.1}{10 - \text{F.O.}\ (1.6)} \le R \le \frac{2.1}{N(0.1) + \text{F.O.}\ (0.06)}$$

R is in kΩ
N = number of wired-OR outputs
F.O. = number of TTL loads driven

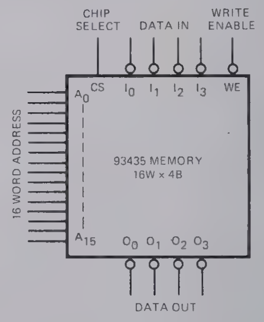
The minimum value of R is limited by output current sinking ability. The maximum value of R is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

- **35 ns MAXIMUM ACCESS TIME – 20 ns TYPICAL**
- **CHIP SELECT AND WRITE ENABLES**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR CAPABILITY**
- **LINEAR SELECT**
- **ON CHIP ADDRESS LINE BUFFERING**
- **TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

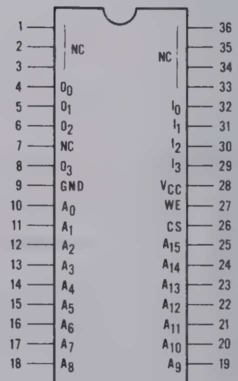
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +7.0 V
Input Pin Voltage	−0.5 V to +5.5 V
Current into Output Terminal	50 mA
Output Voltage	−0.5 V to +8.0 V

LOGIC SYMBOL


CHIP SELECT
DATA IN
WRITE ENABLE
CS
I0
I1
I2
I3
WE
A0
16 WORD ADDRESS
93435 MEMORY
16W × 4B
A15
O0
O1
O2
O3
DATA OUT

CONNECTION DIAGRAM

DIP (TOP VIEW)


1
2
3
NC
4 O0
5 O1
6 O2
7 NC
8 O3
9 GND
10 A0
11 A1
12 A2
13 A3
14 A4
15 A5
16 A6
17 A7
18 A8
36
35
34
33
NC
32 I0
31 I1
30 I2
29 I3
28 VCC
27 WE
26 CS
25 A15
24 A14
23 A13
22 A12
21 A11
20 A10
19 A9

NC = No Internal Connection

LOADING RULES

	HIGH LEVEL (TTL Unit Loads)	LOW LEVEL (TTL Unit Loads)
Address	1.67	1
Chip Select	26.7	1 (see note 1)
Write Enable	1.67	1
Data Input	3.34	2
Data Output	Open Collector	6.2

1 LOW Level TTL Unit Load = 1.6 mA
1 HIGH Level TTL Unit Load = 60 μA

ELECTRICAL CHARACTERISTICS (T_A = −55°C to 125°C, V_{CC} = 5.0 V ± 10%) (units are pulse tested) (Part No. 93435XM)*

SYMBOL	PARAMETER	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C		+125°C			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_A = 0.4 V
I_{FCS}	Chip Select Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_{CS} = 0.4 V See Note 1
I_{FWE}	Write Enable Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_W = 0.4 V
I_{FD}	Data Input Load Current		−3.2		−3.2		−3.2	mA	V_{CC} = 5.5 V, V_D = 0.4 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.5 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.5 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.5 V Write Enable Input Grounded
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 10 mA One Word Addressed
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	Volts	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input HIGH Voltage	2.1		2.0		2.0		Volts	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		118		118		118	mA	V_{CC} = 5.5 V, One Word Addressed

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ± 5%) (units are pulse tested) (Part No. 93435XC)*

SYMBOL	PARAMETER	LIMITS						UNITS	CONDITIONS
		0 C		+25°C		+75°C			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FCS}	Chip Select Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V See Note 1
I_{FWE}	Write Enable Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FD}	Data Input Load Current		−3.2		−3.2		−3.2	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RCS}	Chip Select Input Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RWE}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25 V Write Enable Input Grounded
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 10 mA One Word Addressed
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	Volts	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		Volts	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		124		124		124	mA	V_{CC} = 5.25 V, One Word Addressed

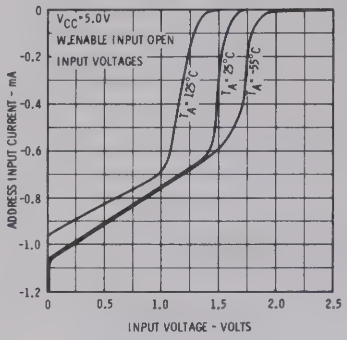
*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTE:

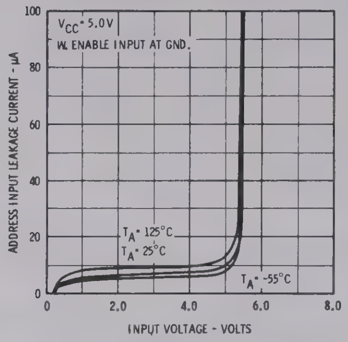
(1) I_{FCS} increases by 1.6 mA for each address input held at a logic 1.

TYPICAL ELECTRICAL CHARACTERISTICS

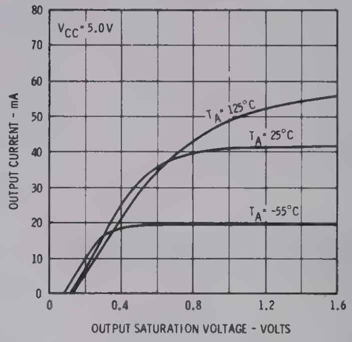
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



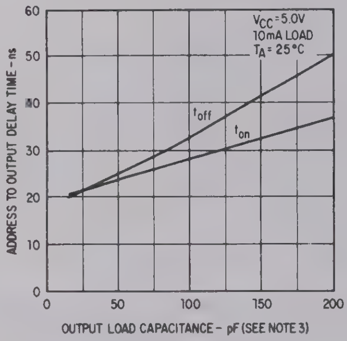
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



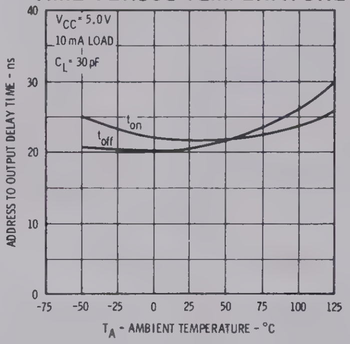
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



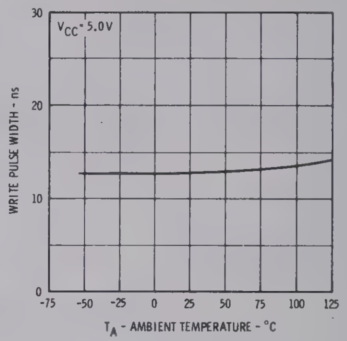
ADDRESS TO OUTPUT DELAY TIME VERSUS OUTPUT LOAD CAPACITANCE



ADDRESS TO OUTPUT DELAY TIME VERSUS TEMPERATURE



WRITE PULSE WIDTH VERSUS TEMPERATURE

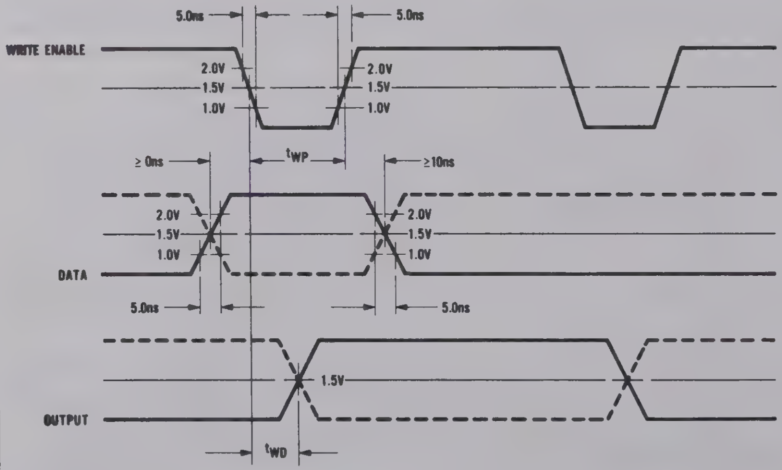


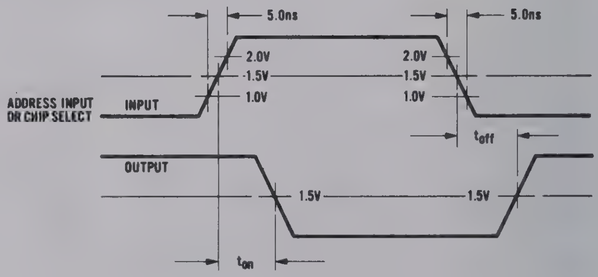
SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

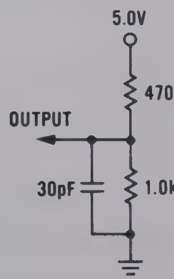
SYMBOL	PARAMETER	LIMIT (ns)			CONDITION		
		MIN.	TYP.	MAX.	LOAD	C	NOTE
t_{on}	Address to Output Turn-On Delay	10	22	35	10 mA	30 pF	1
t_{off}	Address to Output Turn-Off Delay	10	20	35	10 mA	30 pF	1
t_{WP}	Write Pulse Width Required to Write	25	15		10 mA	30 pF	2
t_{WD}	Write Delay	10	30	50	10 mA	30 pF	2

NOTES:

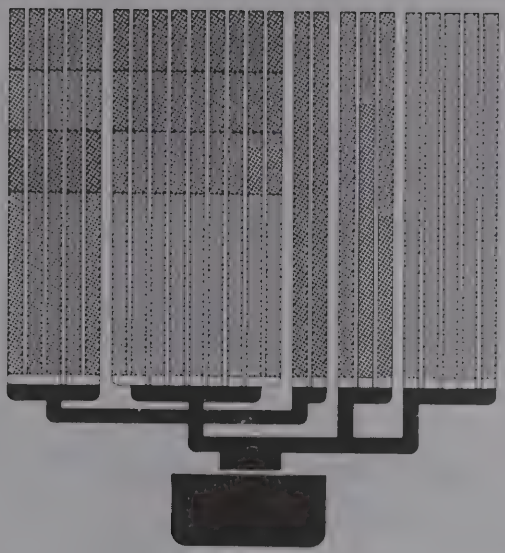
(1) To test t_{on} and t_{off}, a LOW must be stored in the cell under test.
(2) One word is selected during the test.
(3) The typical capacitance of one 93435 output is 7.0 pF.


5.0ns
5.0ns
WRITE ENABLE
2.0V
1.5V
1.0V
2.0V
1.5V
1.0V
t_{WP}
≥ 0ns
≥10ns
DATA
2.0V
1.5V
1.0V
2.0V
1.5V
1.0V
5.0ns
5.0ns
OUTPUT
1.5V
t_{WD}


5.0ns
5.0ns
ADDRESS INPUT OR CHIP SELECT
INPUT
2.0V
1.5V
1.0V
2.0V
1.5V
1.0V
t_{off}
OUTPUT
1.5V
1.5V
t_{on}


5.0V
470Ω
OUTPUT
30pF
1.0kΩ

10 mA TEST LOAD



Packaging Information

PACKAGING INFORMATION

Fairchild digital integrated circuits may be ordered using a simplified purchasing code in which the package style is defined as follows:

PACKAGE STYLE

D = Dual In-Line — Ceramic (Hermetic)
P = Dual In-Line — Plastic
F = Flat Package

9310 D C
Device Type — Package Style — Temperature Range

In order to accommodate varying die sizes (SSI, MSI, etc), numbers of pins (14, 16, 24, etc.), and package outlines, a number of different package forms are required in each of these three categories.

The following lists indicate the specific package dimensions currently used for each device type. The detailed outline corresponding to each package code is shown at the end of this section.

DEVICE	MILITARY (M) –55° to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0° to +70°/75°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
4100 (see 93400)						
4101 (see 93401)						
4102 (see 93402)						
4103 (see 93403)						
4106 (see 93406)						
5033 (see 93407)						
5400	6A	3I	7400	6A	9A	3I
5401	6A	3I	7401	6A	9A	3I
5402	6A	3I	7402	6A	9A	3I
5403	6A	3I	7403	6A	9A	3I
5404	6A	3I	7404	6A	9A	3I
5405	6A	3I	7405	6A	9A	3I
5406	6A	3I	7406	6A	9A	3I
5407	6A	3I	7407	6A	9A	3I
5408	6A	3I	7408	6A	9A	3I
5409	6A	3I	7409	6A	9A	3I
5410	6A	3I	7410	6A	9A	3I
5411	6A	3I	7411	6A	9A	3I
5412	6A	3I	7412	6A	9A	3I
5413	6A	3I	7413	6A	9A	3I
5416	6A	3I	7416	6A	9A	3I
5417	6A	3I	7417	6A	9A	3I
5420	6A	3I	7420	6A	9A	3I
5423	6B	4L	7423	6B	9B	4L
5425	6A	3I	7425	6A	9A	3I
5426	6A		7426	6A	9A	3I
5427	6A	3I	7427	6A	9A	3I
5430	6A	3I	7430	6A	9A	3I
5432	6A	3I	7432	6A	9A	3I
5437	6A	3I	7437	6A	9A	3I
5438	6A	3I	7438	6A	9A	3I
5439	6A	3I	7439	6A	9A	3I
5440	6A	3I	7440	6A	9A	3I
			7441	6B	9B	4L
5442	6B	4L	7442	6B	9B	4L
5443	6B	4L	7443	6B	9B	4L
5444	6B	4L	7444	6B	9B	4L

PACKAGING INFORMATION

DEVICE	MILITARY (M) −55° to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0° to +70°/75°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
5445	7B	4L	7445	7B	9B	4L
5446	7B	4L	7446	7B	9B	4L
5447	7B	4L	7447	7B	9B	4L
5448	7B	4L	7448	7B	9B	4L
5449		3I	7449			3I
5450	6A	3I	7450	6A	9A	3I
5451	6A	3I	7451	6A	9A	3I
5453	6A	3I	7453	6A	9A	3I
5454	6A	3I	7454	6A	9A	3I
5460	6A	3I	7460	6A	9A	3I
5470	6A	3I	7470	6A	9A	3I
5472	6A	3I	7472	6A	9A	3I
5473	6A	3I	7473	6A	9A	3I
5474	6A	3I	7474	6A	9A	3I
5475	6B	4L	7475	6B	9B	4L
5476	6B	4L	7476	6B	9B	4L
5477		3I	7477			3I
5480	6A	3I	7480	6A	9A	3I
5482	6A	3I	7482	6A	9A	3I
5483	6B	4L	7483	6B	9B	4L
5486	6A	3I	7486	6A	9A	3I
5490	6A	3I	7490	6A	9A	3I
5491	6A	3I	7491	6A	9A	3I
5492	6A	3I	7492	6A	9A	3I
5493	6A	3I	7493	6A	9A	3I
5494	6B	4L	7494	6B	9B	4L
5495	6A	3B	7495	6A	9A	3B
5496	7B	4L	7496	7B	9B	4L
54104	6A	3I	74104	6A	9A	3I
54105	6A	3I	74105	6A	9A	3I
54107	6A		74107	6A	9A	
54121	6A	3I	74121	6A	9A	3I
			74141	6B	9B	
54145	7B	4L	74145	7B	9B	4L
54150	6N	4M	74150	6N		4M
54151	7B	4L	74151	7B	9B	4L
54152	7A	3B	74152	7A	9A	3B
54153	7B	4L	74153	7B	9B	4L
54164	7A	3B	74164	7A	9A	3B
54165	7B	4L	74165	7B	9B	4L
54180	7A	3B	74180	7A	9A	3B
54181	6N	4M	74181	6N		4M
54182	7B	4L	74182	7B	9B	4L
54190	7B	4L	74190	7B	9B	4L
54191	7B	4L	74191	7B	9B	4L
54192	7B	4L	74192	7B	9B	4L
54193	7B	4L	74193	7B	9B	4L
54196	7A	3B	74196	7A	9A	3B
54197	7A	3B	74197	7A	9A	3B
54198	6N	4M	74198	6N		4M
54H00	6A	3I	74H00	6A	9A	3I

PACKAGING INFORMATION

DEVICE	MILITARY (M) −55° to +125°C		DEVICE	COMMERCIAL (C)/INDUSTRIAL 0° to +70°/75°C		
	CERAMIC DIP (D)	FLATPAK (F)		CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
54H01	6A	3I	74H01	6A	9A	3I
54H04	6A	3I	74H04	6A	9A	3I
54H05	6A	3I	74H05	6A	9A	3I
54H08	6A	3I	74H08	6A	9A	3I
54H10	6A	3I	74H10	6A	9A	3I
54H11	6A	3I	74H11	6A	9A	3I
54H20	6A	3I	74H20	6A	9A	3I
54H21	6A	3I	74H21	6A	9A	3I
54H22	6A	3I	74H22	6A	9A	3I
54H30	6A	3I	74H30	6A	9A	3I
54H40	6A	3I	74H40	6A	9A	3I
54H50	6A	3I	74H50	6A	9A	3I
54H51	6A	3I	74H51	6A	9A	3I
54H52	6A	3I	74H52	6A	9A	3I
54H53	6A	3I	74H53	6A	9A	3I
54H54	6A	3I	74H54	6A	9A	3I
54H55	6A	3I	74H55	6A	9A	3I
54H60	6A	3I	74H60	6A	9A	3I
54H61	6A	3I	74H61	6A	9A	3I
54H62	6A	3I	74H62	6A	9A	3I
54H71	6A	3I	74H71	6A	9A	3I
54H72	6A	3I	74H72	6A	9A	3I
54H73	6A	3I	74H73	6A	9A	3I
54H74	6A	3I	74H74	6A	9A	3I
54H76	6B	4L	74H76	6B	9B	4L
54H78	6A	3I	74H78	6A	9A	3I
54H87	7A	3B	74H87	7A		3B
54H101	6A	3I	74H101	6A	9A	3I
54H102	6A	3I	74H102	6A	9A	3I
54H103	6A	3I	74H103	6A	9A	3I
54H106	6B	4L	74H106	6B	9B	4L
54H108	6A	3I	74H108	6A	9A	3I
54H183	7A	3B	74H183	7A		3B
54S00	6A	3I	74S00	6A		3I
54S03	6A	3I	74S03	6A		3I
54S04	6A	3I	74S04	6A		3I
54S05	6A	3I	74S05	6A		3I
54S20	6A	3I	74S20	6A		3I
54S22	6A	3I	74S22	6A		3I
54S40	6A	3I	74S40	6A		3I
54S64	6A	3I	74S64	6A		3I
54S65	6A	3I	74S65	6A		3I
54S74	6A	3I	74S74	6A		3I
54S112	6B	4L	74S112	6B		4L
54S113	6A	3I	74S113	6A		3I
54S114	6A	3I	74S114	6A		3I
54S140	6A	3I	74S140	6A		3I
55107	6A		75107	6A	9A	
55108	6A		75108	6A	9A	
55109	6A		75109	6A	9A	
55110			75110	6A	9A	
			75450	6A		

PACKAGING INFORMATION

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL 0°C to +70°C/75°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
9000	6A	3I	6A		3I
9001	6A	3I	6A		3I
9002	6A	3I	6A		3I
9003	6A	3I	6A		3I
9004	6A	3I	6A		3I
9005	6A	3I	6A		3I
9006	6A	3I	6A		3I
9007	6A	3I	6A		3I
9008	6A	3I	6A		3I
9009	6A	3I	6A		3I
9012	6A	3I	6A		3I
9014	6B	4L	6B		4L
9015	6B	4L	6B		4L
9016	6A	3I	6A		3I
9017	6A	3I	6A		3I
9020	7B	4L	7B		4L
9022	7B	4L	7B		4L
9024	7B	4L	7B		4L
9033 (see 93433)					
9034 (see 93434)					
9035 (see 93435)					
9H00	6A	3I	6A	9A	3I
9H01	6A	3I	6A	9A	3I
9H04	6A	3I	6A	9A	3I
9H05	6A	3I	6A	9A	3I
9H08	6A	3I	6A	9A	3I
9H10	6A	3I	6A	9A	3I
9H11	6A	3I	6A	9A	3I
9H20	6A	3I	6A	9A	3I
9H21	6A	3I	6A	9A	3I
9H22	6A	3I	6A	9A	3I
9H30	6A	3I	6A	9A	3I
9H40	6A	3I	6A	9A	3I
9H50	6A	3I	6A	9A	3I
9H51	6A	3I	6A	9A	3I
9H52	6A	3I	6A	9A	3I
9H53	6A	3I	6A	9A	3I
9H54	6A	3I	6A	9A	3I
9H55	6A	3I	6A	9A	3I
9H60	6A	3I	6A	9A	3I
9H61	6A	3I	6A	9A	3I
9H62	6A	3I	6A	9A	3I
9H71	6A	3I	6A	9A	3I
9H72	6A	3I	6A	9A	3I
9H73	6A	3I	6A	9A	3I
9H74	6A	3I	6A	9A	3I
9H76	6B	4L	6B	9B	4L
9H78	6A	3I	6A	9A	3I
9H101	6A	3I	6A	9A	3I
9H102	6A	3I	6A	9A	3I
9H103	6A	3I	6A	9A	3I

PACKAGING INFORMATION

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL 0°C to +70°C/75°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
9H106	6B	4L	6B	9B	4L
9H108	6A	3I	6A	9A	3I
9L00	6A	3I	6A		3I
9L04	6A	3I	6A		3I
9L24	7B	4L	7B		4L
9L54	6A	3I	6A		3I
9L86	6A	3I	6A		3I
9N00	6A	3I	6A	9A	3I
9N01	6A	3I	6A	9A	3I
9N02	6A	3I	6A	9A	3I
9N03	6A	3I	6A	9A	3I
9N04	6A	3I	6A	9A	3I
9N05	6A	3I	6A	9A	3I
9N06	6A	3I	6A	9A	3I
9N07	6A	3I	6A	9A	3I
9N08	6A	3I	6A	9A	3I
9N09	6A	3I	6A	9A	3I
9N10	6A	3I	6A	9A	3I
9N11	6A	3I	6A	9A	3I
9N12	6A	3I	6A	9A	3I
9N13	6A	3I	6A	9A	3I
9N16	6A	3I	6A	9A	3I
9N17	6A	3I	6A	9A	3I
9N20	6A	3I	6A	9A	3I
9N23	6B	4L	6B	9B	4L
9N25	6A	3I	6A	9A	3I
9N26	6A	3I	6A	9A	3I
9N27	6A	3I	6A	9A	3I
9N30	6A	3I	6A	9A	3I
9N32	6A	3I	6A	9A	3I
9N37	6A	3I	6A	9A	3I
9N38	6A	3I	6A	9A	3I
9N39	6A	3I	6A	9A	3I
9N40	6A	3I	6A	9A	3I
9N50	6A	3I	6A	9A	3I
9N51	6A	3I	6A	9A	3I
9N53	6A	3I	6A	9A	3I
9N54	6A	3I	6A	9A	3I
9N60	6A	3I	6A	9A	3I
9N70	6A	3I	6A	9A	3I
9N72	6A	3I	6A	9A	3I
9N73	6A	3I	6A	9A	3I
9N74	6A	3I	6A	9A	3I
9N76	6B	4L	6B	9B	4L
9N86	6A	3I	6A	9A	3I
9N107	6A	3I	6A	9A	3I
9S00	6A	3I	6A		3I
9S03	6A	3I	6A		3I
9S04	6A	3I	6A		3I
9S04A	6A	3I	6A		3I
9S05	6A	3I	6A		3I
9S05A	6A	3I	6A		3I

PACKAGING INFORMATION

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL 0°C to +70°C/75°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
9S20	6A	3I	6A		3I
9S22	6A	3I	6A		3I
9S40	6A	3I	6A		3I
9S64	6A	3I	6A		3I
9S65	6A	3I	6A		3I
9S74	6A	3I	6A		3I
9S109	6B	4L	6B		4L
9S112	6B	4L	6B		4L
9S113	6A	3I	6A		3I
9S114	6A	3I	6A		3I
9S140	6A	3I	6A		3I
9300	7B	4L	7B		4L
93H00	7B	4L	7B		4L
9301	7B	4L	7B		4L
9302	7B	4L	7B		4L
9304	6B	4L	6B		4L
9305	7A	3B	7A		3B
9307	6B	4L	6B		4L
9308	6N	4M	6N	9N	4M
9309	6B	4L	6B		4L
9310	7B	4L	7B		4L
9311	6N	4M	6N	9N	4M
9312	7B	4L	7B		4L
9313	7B	4L	7B		4L
9314	7B	4L	7B		4L
9315	6B	4L	6B	9B	4L
9316	7B	4L	7B		4L
9317B	7B	4L	7B		4L
9317C	7B	4L	7B		4L
9318	7B	4L	7B		4L
9321	7B	4L	7B		4L
9322	7B	4L	7B		4L
9324	7B	4L	7B		4L
9328	7B	4L	7B		4L
9334	7B	4L	7B		4L
9338	7B	4L	7B		4L
9340	6N	4M	6N	9N	4M
9341	6N	4M	6N	9N	4M
9342	7B	4L	7B		4L
9344	6N	4M	6N	9N	4M
9345	7B	4L	7B	9B	4L
9348	7B	4L	7B		4L
9350			7A		
9352	6B	4L	6B	9B	4L
9353	6B	4L	6B	9B	4L
9354	6B	4L	6B	9B	4L
9356			7A		
9357A	7B	4L	7B	9B	4L
9357B	7B	4L	7B	9B	4L
9358	7B	4L	7B	9B	4L
9359		3I			3I

PACKAGING INFORMATION

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL 0°C to +70°C/75°C		
	CERAMIC	FLATPAK (F) DIP (D)	CERAMIC	PLASTIC DIP (D)	FLATPAK (F) DIP (P)
9360	7B	4L	7B	9B	4L
9366	7B	4L	7B	9B	4L
93H72	7B	4L	7B		4L
9375	6B	4L	6B	9B	4L
9377		3I			3I
9380	6A	3I	6A	9A	3I
9382	6A	3I	6A	9A	3I
9383	6B	4L	6B	9B	4L
9386	7A	3B	7A		3B
93H87	7A	3B	7A		3B
9390	6A	3B	6A	9A	3B
9391	6A	3I	6A	9A	3I
9392	6A	3B	6A	9A	3B
9393	6A	3B	6A	9A	3B
9394	6B	4L	6B	9B	4L
9395	6A	3I	6A	9A	3I
9396	7B	4L	7B	9B	4L
93141			6B	9B	
93145	7B	4L	7B	9B	4L
93150	6N	4M	6N	9N	4M
93151	7B	4L	7B	9B	4L
93152	7A	3B	7A	9A	3B
93153	7B	4L	7B	9B	4L
93164	7A	3B	7A	9A	3B
93165	7B	4L	7B	9B	4L
93180	7A	3B	7A	9A	3B
93H183	7A	3B	7A		3B
93190	7B	4L	7B	9B	4L
93191	7B	4L	7B	9B	4L
93196	7A	3B	7A	9A	3B
93197	7A	3B	7A	9A	3B
93198	6N	4M	6N	9N	4M
93400			7B		
93400B			7B		
93401			7B		
93402			6N		
93403			7B		4L
93406			7K		
93407/A			6A		3I
93407/B	6A	3I	6A		3I
93410	7K		7K		
93410A			7K		
93415			7K		
93433/A			6A		3I
93433/B	6A	3I	6A		3I
93434	7B		7B		
93435	7U		7U		
93L00	7B	4L	7B		4L
93L01	7B	4L	7B		4L
93L08	6N	4M	6N		4M
93L09	6B	4L	6B		4L
93L10	7B	4L	7B		4L
93L11	6N	4M	6N		4M
93L12	7B	4L	7B		4L

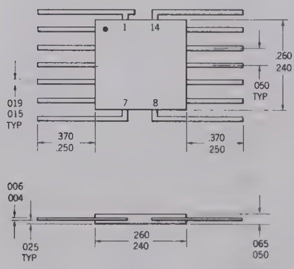
PACKAGING INFORMATION

DEVICE	MILITARY (M) −55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL 0°C to +70°C/75°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
93L14	7B	4L	7B		4L
93L16	7B	4L	7B		4L
93L18	7B	4L	7B		4L
93L21	7B	4L	7B		4L
93L22	7B	4L	7B		4L
93L24	7B	4L	7B		4L
93L28	7B	4L	7B		4L
93L40	6N	4M	6N		4M
93S00	7B	4L	7B		4L
93S05	7A	3B	7A		3B
93S10	7B	4L	7B		4L
93S12	7B	4L	7B		4L
93S16	7B	4L	7B		4L
93S41	6N	4M	6N		4M
93S42	7B	4L	7B		4L
93S62	7A	3B	7A		3B
9600	6A	3I	6A	9A	3I
9601	6A	3I	6A	9A	3I
9602	6B	4L	6B		4L
96L02	6B	4L	6B		4L
9603	6A	3I	6A	9A	3I
9614	7B	4L	7B		4L
9615	7B	4L	7B		4L
9616			6A		
9617			6A		
9620	6A	3I	6A		3I
9621	6A	3I	6A		3I
9622	6A	3I	6A		3I
9624	6A	3I	6A		3I
9625	6A	3I	6A		3I
9644	7B		7B		

PACKAGE PHYSICAL DIMENSIONS

3B

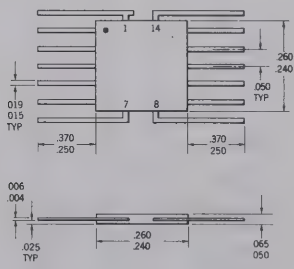
in accordance with
JEDEC (TO-86) outline
14 Lead MSI Cerpak


1
14
7
8
.260
240
050
TYP
019
015
TYP
370
.250
.370
250
006
004
025
TYP
260
240
065
050

NOTES. All dimensions in inches
Leads are gold-plated kovar
Package weight is 0 26 gram
Lead 1 orientation may be either tab or dot

3I

in accordance with
JEDEC (TO-86) outline
14 Lead Cerpak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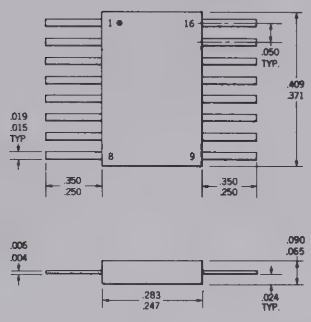
14
7
8
.260
.240
.050
TYP
019
015
TYP
.370
.250
.370
250
006
.004
.025
TYP
.260
.240
065
050

NOTES· All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram
Lead 1 orientation may be either tab or dot

PACKAGE PHYSICAL DIMENSIONS

16 Lead Cerpak

4L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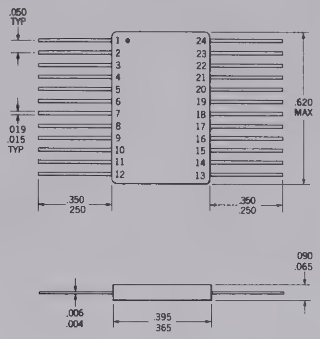
16
8
9
.050
TYP.
.409
.371
.019
.015
TYP
.350
.250
.350
.250
.006
.004
.090
.065
.283
.247
.024
TYP.

NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

24 Lead BeO Cerpak

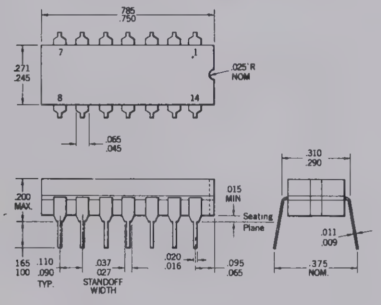
4M


.050
TYP
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
.620
MAX
019
.015
TYP
.350
250
.350
.250
090
.065
.006
.004
.395
365

NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram

in accordance with JEDEC (TO-116) outline 14 Lead SSI Dual In-line

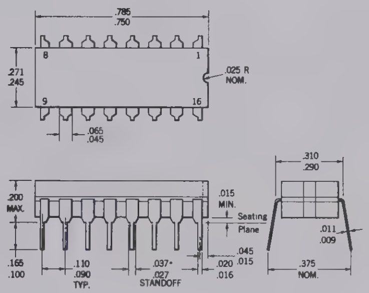
6A


785
.750
7
1
8
14
.271
.245
.025'R
NOM
.065
.045
.310
.290
.200
MAX.
.015
MIN
Seating
Plane
.011
.009
165
100
.110
.090
TYP.
.037
027
STANDOFF
WIDTH
.020
.016
.095
.065
.375
NOM.

NOTES: All dimensions in inches
Leads are intended for insertion in hole
rows on .300" centers
They are purposely shipped with "positive"
misalignment to facilitate insertion
Board-drilling dimensions should equal your
practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

16 Lead SSI Dual In-line

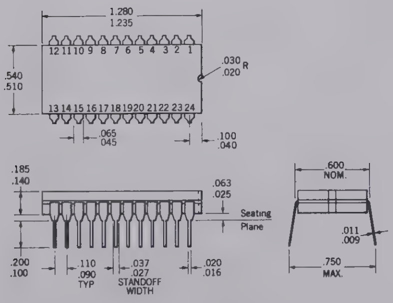
6B


.785
.750
8
1
9
16
.271
.245
.025 R
NOM.
.065
.045
.310
.290
.200
MAX.
.015
MIN.
Seating
Plane
.011
.009
.045
.015
.165
.100
.110
.090
TYP.
.037*
.027
STANDOFF
.020
.016
.375
NOM.

NOTES All dimensions in inches
Leads are intended for insertion in hole
rows on 300" centers
They are purposely shipped with "positive"
misalignment to facilitate insertion
Board-drilling dimensions should equal your
practice for 020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The 0371/ 027 dimension does not apply
to the corner leads

24 Lead MSI Dual In-line

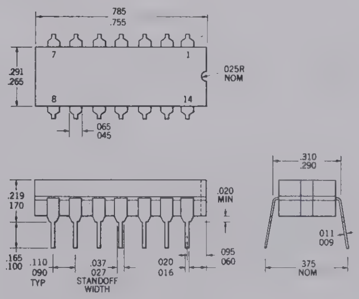
6N


1.280
1.235
12 11 10 9 8 7 6 5 4 3 2 1
13 14 15 16 17 18 19 20 21 22 23 24
.030
.020
R
.540
.510
.065
045
.100
.040
.185
.140
.063
.025
Seating
Plane
.600
NOM.
.011
.009
.200
.100
.110
.090
TYP
.037
.027
STANDOFF
WIDTH
.020
.016
.750
MAX.

NOTES: All dimensions in inches
Leads are intended for insertion in hole
rows on 600" centers
They are purposely shipped with "positive"
misalignment to facilitate insertion
Leads are tin-plated kovar
Package weight is 6.5 grams

Similar* to JEDEC (TO-116) outline 14 Lead MSI Dual In-line

7A

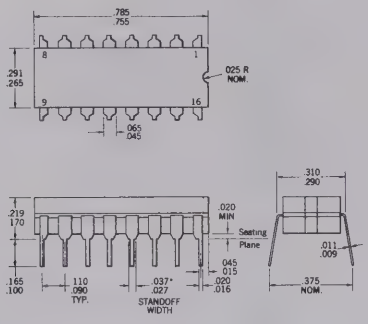

785
.755
7
1
8
14
.291
.265
025R
NOM
065
045
.310
.290
.219
170
.020
MIN
011
009
.165
.100
.110
090
TYP
.037
027
STANDOFF
WIDTH
020
016
095
060
375
NOM

NOTES: All dimensions in inches
Leads are intended for insertion in hole
rows on 300" centers
They are purposely shipped with "positive"
misalignment to facilitate insertion
Board-drilling dimensions should equal your
practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*Similar to JEDEC TO-116 except for
package width

PACKAGE PHYSICAL DIMENSIONS

7B

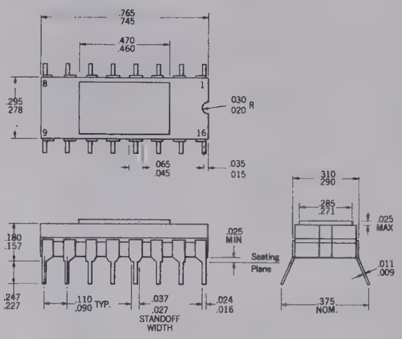
16 Lead MSI Dual In-line


.785
.755
8
1
.291
.265
.025 R
NOM.
9
16
.065
.045
.310
.290
.219
.170
.020
MIN
Seating
Plane
.011
.009
.045
.015
.165
.100
.110
.090
TYP.
.037*
.027
STANDOFF
WIDTH
.020
.016
.375
NOM.

NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .037 dimension does not apply to the corner leads

7K

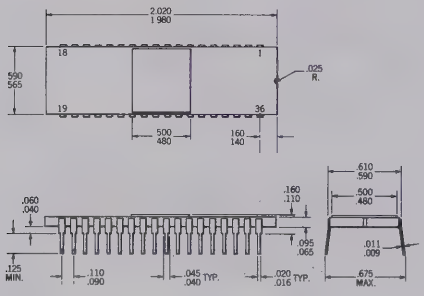
16 Lead Dual In-line (Metal Cap)


.765
.745
.470
.460
8
1
.295
.278
.030
.020
R
9
16
.065
.045
.035
.015
.310
.290
.285
.271
.025
MAX
.180
.157
.025
MIN
Seating
Plane
.011
.009
.247
.227
.110
.090
TYP.
.037
.027
STANDOFF
WIDTH
.024
.016
.375
NOM.

NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are gold-plated kovar
Low temperature seal
Package weight is 1.3 grams

7U

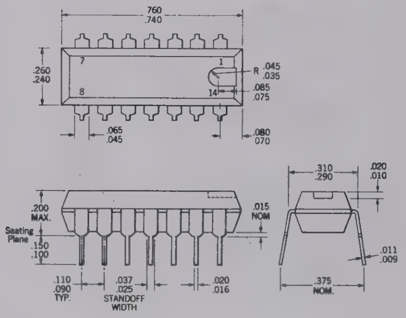
36 Lead Side Brazed Dual In-line


2.020
1.980
18
1
.590
.565
.025
R.
19
36
.500
.480
.160
.140
.610
.590
.500
.480
.060
.040
.160
.110
.095
.065
.011
.009
.125
MIN.
.110
.090
.045
.040
TYP.
.020
.016
TYP.
.675
MAX.

NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are gold-plated kovar
Package weight is 6.2 grams

9A

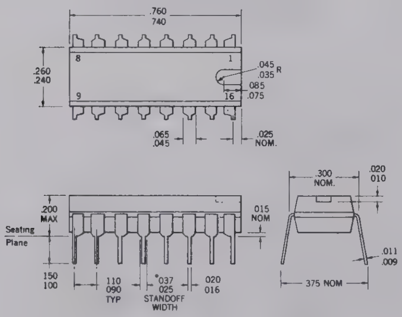
in accordance with JEDEC (TO-116) outline 14 Lead Silicone Dual In-line


.760
.740
7
1
.260
.240
R
.045
.035
.085
.075
8
14
.065
.045
.080
.070
.310
.290
.020
.010
.200
MAX.
.015
NOM
Seating
Plane
.150
.100
.011
.009
.110
.090
TYP.
.037
.025
STANDOFF
WIDTH
.020
.016
.375
NOM.

NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 grams

9B

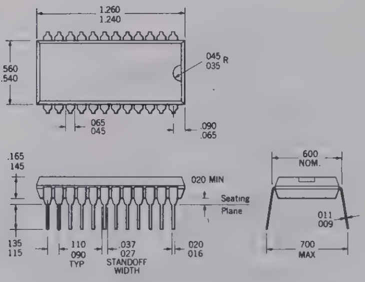
16 Lead Silicone Dual In-line


.760
.740
8
1
.260
.240
.045
.035
R
.085
.075
9
16
.065
.045
.025
NOM.
.300
NOM.
.020
.010
.200
MAX
.015
NOM
Seating
Plane
.011
.009
.150
.100
.110
.090
TYP
*.037
.025
STANDOFF
WIDTH
.020
.016
.375 NOM

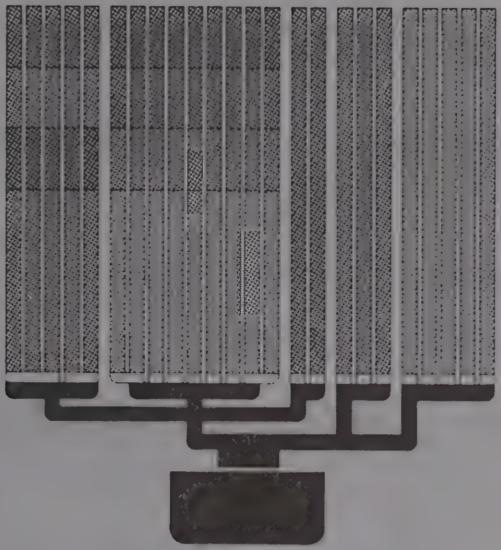
NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 grams
*The .0371/.027 dimension does not apply to the corner leads

9N

24 Lead Plastic MSI Dual In-line


1.260
1.240
.045
.035
R
.560
.540
.065
.045
.090
.065
.165
.145
.020 MIN
Seating
Plane
.600
NOM.
.011
.009
.135
.115
.110
.090
TYP
.037
.027
STANDOFF
WIDTH
.020
.016
.700
MAX

NOTES: All dimensions in inches
Leads are intended for insertion in hole rows on .600" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Leads are tin-plated kovar
Package weight is 2.7 grams



Industry Cross Reference Guide

11

12

INDUSTRY TTL CROSS REFERENCE GUIDE

The following charts indicate the recommended Fairchild replacement for the most popular TTL devices in use today.
Two categories of replacement are given.

1. Pin for Pin Replacement

Function and pin configuration are identical, however some small differences in the electrical or mechanical specification or method of test may exist.

2. Functional Equivalent

Device performing similar function, but with different pin outs, or organization.

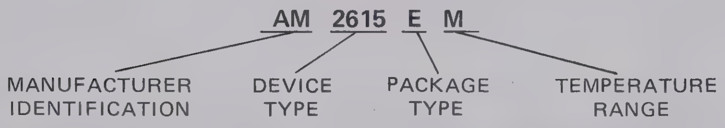
Exact interchangability in every application is not guaranteed. Before specifying a substitute, the user should compare the most recent data and device parameters from both sources of supply.

Cross reference information is provided for the following manufacturers.

- Advanced Micro Devices
- Computer Microtechnology
- Intel
- ITT
- Motorola
- National
- Philips
- Signetics
- Texas Instruments

AMD — ADVANCED MICRO DEVICES

DEVICE ORDER NUMBER FORMAT



PACKAGE CROSS REFERENCE

PACKAGE	AMD	FAIRCHILD
Dual In-Line Ceramic	U7B, E,F,G, U6N, U6B, U6A	D
Dual In-Line Plastic	U6E, U6M, A,B,C	P
Flatpak	U4L, U4M, U3I, M,N,P	F

TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE	AMD	FAIRCHILD
COMMERCIAL 0°C to +70°C/75°C	C, 59X	C
MILITARY −55°C to +125°C	M, 51X	M

AMD	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	AMD	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	AMD	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
2501		9366	9306	9306		9324	9324	
2505		9344	9308	9308		93L24	93L24	
2506		9341	93L08	93L08		9328	9328	
2600		9600	9309	9309		93L28	93L28	
2602		9602	93L09	93L09		9338	9338	
26L02		96L02	9310	9310		93L38		9338
2614		9614	93L10	93L10		9340	9340	
2615		9615	9311	9311		93L40	93L40	
2700		93410	93L11	93L11		9341	9341	
3101	93403		9312	9312		93L41		9341
31L01		93403	93L12	93L12		9342	9342	
54181	9341		9314	9314		9600	9600	
54182	9342		93L14	93L14		9601	9601	
9300	9300		9316	9316		9602	9602	
93L00	93L00		93L16	93L16		96L02	96L02	
9301	9301		9318	9318		9614	9614	
93L01	93L01		93L18	93L18		9620	9620	
9304	9304		9322	9322		9621	9621	
			93L22	93L22				

CMI – COMPUTER MICROTECHNOLOGY INC.

DEVICE ORDER NUMBER FORMAT

CM 2150

CM: MANUFACTURER IDENTIFICATION

2150: DEVICE TYPE

CMI	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
2100	93403	
2150	93410	
2800		93406
2850	93406	

INTEL

DEVICE ORDER NUMBER FORMAT

P 3102

P: PACKAGE TYPE

3102: DEVICE TYPE

PACKAGE CROSS REFERENCE

PACKAGE	INTEL	FAIRCHILD
Dual In-Line Ceramic	C	D
Dual In-Line Plastic	P	P

INTEL	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	INTEL	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	INTEL	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
3101	93403		3106		93410	3202	93401	
3101A		93403	3106A		93410	3205		9301
3102	93400		3107		93410	3404		9314
3104	93402		3107A		93410	3301	93406	

ITT SEMICONDUCTORS

DEVICE ORDER NUMBER FORMAT

MIC 9300 I D

MIC: MANUFACTURER IDENTIFICATION

9300: DEVICE TYPE

I: TEMPERATURE RANGE

D: PACKAGE TYPE

PACKAGE CROSS REFERENCE

PACKAGE	ITT	FAIRCHILD
Dual In-Line Ceramic	D	D
Dual In-Line Plastic	—	P
Flatpak	B	F

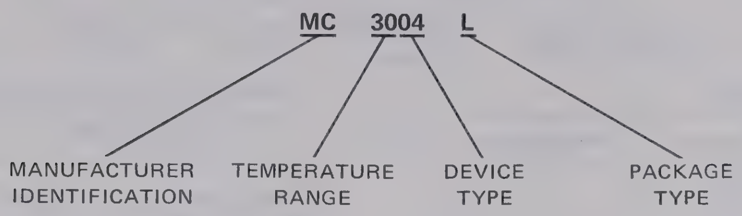
TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE	ITT	FAIRCHILD
COMMERCIAL 0°C to +70°C/75°C	5	C
MILITARY −55°C to +125°C	1	M

ITT	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	ITT	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	ITT	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
5033	93407	93433	9008	9008		9033	93433	93407
9000	9000		9009	9009		9300	9300	
9001	9001		9014	9014		9301	9301	
9002	9002		9015	9015		9304	9304	
9003	9003		9016	9016		9309	9309	
9004	9004		9017	9017		9312	9312	
9005	9005		9022	9022		9316	9316	
9006	9006		9024	9024		9601	9601	
9007	9007							

MOTOROLA

DEVICE ORDER NUMBER FORMAT



PACKAGE CROSS REFERENCE

PACKAGE	MOTOROLA	FAIRCHILD
Dual In-Line Ceramic	L	D
Dual In-Line Plastic	P	P
Flatpak	F	F

TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE	MOTOROLA	FAIRCHILD
COMMERICAL 0°C to +70°C/75°C	30,40,72,74,83	C
MILITARY −55°C to +125°C	31,43,82,54,93	M

MOTOROLA	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	MOTOROLA	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	MOTOROLA	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
5400 54H00 7400 74H00	See T.I. Cross Reference		3025		9H40, 74H40	4018		9316
			3026		9H40, 74H40	4021		9324
			3030	9H60, 74H60		4022		9324
			3031	9H52, 74H52		4023		9305
3000	9H00, 74H00		3032	9H53, 74H53		4026		9304
3001	9H08, 74H08		3033	9H54, 74H54		4027		9304
3002		9N02, 7402, 9015	3034	9H55, 74H55		4028		9341
3003		9N32, 7432	3054	9H71, 74H71		4032		9342
3004	9H01, 74H01		3055	9H72, 74H72		4035		9314
3005	9H10, 74H10		3060		9H74, 74H74	4037		9314
3006	9H11, 74H11		3061	9S114	9H78, 74H78	4039		9307
3007		9N12, 7412	3062	9S113	9H103, 74H103	4064	93403	
3008	9H04, 74H04		3063	9H73, 74H73		7242	9386	
3009	9H05, 74H05		4000		9309	8242	9386	
3010	9H20, 74H20		4001		93434	8300	9300	
3011	9H21, 74H21		4002(MCM)	93434		8301	9301	
3012	9H22, 74H22		4004	93407	93433	8304	9304	
3015		9H30, 74H30	4005	93407	93433	8308	9308	
3016	9H30, 74H30		4006		9321	8309	9309	
3018	9H62, 74H62		4007		9321	8310	9310	
3019	9H61, 74H61		4008		9348	8311	9311	
3020	9H50, 74H50		4010		9348	8312	9312	
3021		9N86, 7486	4012		9300, 93H72	8316	9316	
3022		9014	4015		93174	8328	9328	
3023	9H51, 74H51		4016		9310	8601	9601	
3024	9H40, 74H40							

NATIONAL

DEVICE ORDER NUMBER FORMAT

DM 8213 D

MANUFACTURER IDENTIFICATION
TEMPERATURE RANGE
DEVICE TYPE
PACKAGE TYPE

PACKAGE CROSS REFERENCE

PACKAGE	NATIONAL	FAIRCHILD
Dual In-Line Ceramic	D	D
Dual In-Line Plastic	N	P
Flatpak	F	F

TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE	NATIONAL	FAIRCHILD
COMMERCIAL 0°C to + 70°C/75°C	8,74	C
MILITARY –50°C to + 125°C	7,54	M

NATIONAL	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	NATIONAL	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	NATIONAL	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
5400	See T.I. Cross Reference		8290	93196		8533	9393	
54H00			8291	93197		8550	9375	
7400			8300	9300		8551		9314
74H00			8309	9309		8560	9360	
8200		9324	8310	9310		8563	9366	
8210		9312	8311	9311		8570	93164	
8211		9312	8312	9312		8580	9395	
8213	9311		8316	9316		8582		93410
8220		9348	8322	9322		8588	93434	
8223		9321	8520		9305	8590	93165	
8280	93176		8530	9390		8601	9601	
8281	93177		8532	9392		8602	9602	
8283	9383							

PHILIPS

DEVICE ORDER NUMBER FORMAT

FJH 341

TTL FAMILY DESIGNATION
CIRCUIT FUNCTION
DEVICE NUMBER
TEMPERATURE RANGE

PACKAGE CROSS REFERENCE

PACKAGE	PHILIPS	FAIRCHILD
Dual In-Line Ceramic	—	D
Dual In-Line Plastic	A, B	P
Flatpak	—	F

TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE	PHILIPS	FAIRCHILD
COMMERCIAL 0°C to +70°C/75°C	1	C
MILITARY –55°C to + 125°C	2	M

PHILIPS	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	PHILIPS	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	PHILIPS	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
FJH101	9N30, 7430		FJH261	9352, 7442		FJJ131	9N74, 7474	
FJH111	9N20, 7420		FJH291	9N03, 7403		FJJ141	9390, 7490	9350
FJH121	9N10, 7410		FJH301	9N26, 7426		FJJ151	9391, 7491	
FJH131	9N00, 7400		FJH311		9N01, 7401	FJJ181	9375, 7475	
FJH141	9N40, 7440		FJH321		9N05, 7405	FJJ191	9N76, 7476	
FJH151	9N50, 7450		FJH331		9348	FJJ211	9393, 7493	9356
FJH161	9N51, 7451		FJH341	9311		FJJ251	9392, 7492	
FJH171	9N53, 7453		FJH351	9312		FJJ261	9N107, 74107	
FJH181	9N54, 7454		FJH391	9322		FJJ321	9300	
FJH191	9380, 7480		FJH401	9309		FJJ401	93191	
FJH201	9382, 7482		FJH431		9311	FJJ411	9366	
FJH211	9383, 7483		FJH441	93151	9312	FJK101	9603, 74121	
FJH221	9N02, 7402		FJH451	9341		FJL101	9315, 7441	
FJH231	9N01, 7401		FJH491		9321	FJY101	9N60, 7460	
FJH241	9N04, 7404		FJJ101	9N70, 7470		FJQ101		9338
FJH251	9N05, 7405		FJJ111	9N72, 7472		FJQ111	93403	
			FJJ121	9N73, 7473		FJR101	93434	

SIGNETICS

DEVICE ORDER NUMBER FORMAT

N 8252 B

TEMPERATURE RANGE
DEVICE TYPE
PACKAGE TYPE

PACKAGE CROSS REFERENCE

PACKAGE	SIGNETICS	FAIRCHILD
Dual In-Line Ceramic	E, F, Y	D
Dual In-Line Plastic	A, B, N	P
Flatpak	J, Q, P, R	F

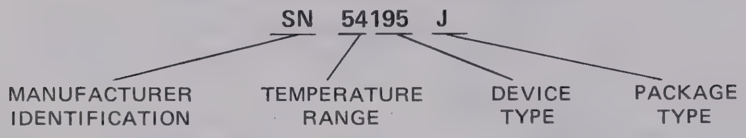
TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE	SIGNETICS	FAIRCHILD
COMMERCIAL 0°C to +70°C/75°C	N	C
MILITARY −55°C to +125°C	S	M

SIGNETICS	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	SIGNETICS	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	SIGNETICS	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
5400	See T.I. Cross Reference		8252	9301		8808		9N30, 7430
54H00			8260		9341	8815		9N25, 7425
54S00			8261		9342	8816		9N20, 7420
7400			8262		9348	8821		9N76, 7476
74H00			82S62	93S62		8822		9N73, 7473
74S00			8263		9309	8824		9N76, 7476
8206		93410	82S63		9309	8825		9N70, 7470
8207		93410	8264		9309	8827		9N73, 7473
8220		93402	82S64		9309	8828		9N74, 7474
8223		93434	8266		9322	8829		9N72, 7472
8224	93434		8267		9322	8840		9N50, 7450
8225	93403		8268		9380	8848		9N53, 7453
8226		93406	8269		9324	8855		9N40, 7440
8229		93406	8270	93178	93H72	8870		9N10, 7410
8230	9312		8271	93179	93H72	8880		9N00, 7400
82S30	93S12		8275		9314	8881		9N01, 7401
8231	9313		8276		9391	8885		9N02, 7402
82S31		9313	8277	9328		8H16		9H20, 74H20
8232		9312	8280	93176	9310	8H20		9H106
82S32		9312	8281	93177	9316	8H21		9H108
8233		9322	8284		93191	8H22		9H108
82S33		9322	8285		93190	8H70		9H10
8234		9322	8288		9392	8H90		9H00
82S34		9322	8290	93196	9310	8T01		9315
8235		9322	82S90		93S10	8T04		9307
82S35		9322	8291	93197	9316	8T05		9307
8241		9N86, 7486	82S91		93S16	8T06		9307
82S41		9N86, 7486	8292		93L10	8T15		9616
8242	9386		8293		93L16	8T16		9617
82S42		9386	8806		9N60, 7460	8T22	9601	

TEXAS INSTRUMENTS

DEVICE ORDER NUMBER FORMAT



PACKAGE CROSS REFERENCE

PACKAGE	T.I.	FAIRCHILD
Dual In-Line Ceramic	J	D
Dual In-Line Plastic	N	P
Flatpak	T, W	F

TEMPERATURE RANGE CROSS REFERENCE

TEMPERATURE RANGE	T.I.	FAIRCHILD
COMMERCIAL 0°C to +75°C/75°C	74, 75	C
MILITARY −55°C to +125°C	54, 55	M

T.I.	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	T.I.	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT	T.I.	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
5400	5400, 9N00	9002	54S20	54S20, 9S20		54H51	54H51, 9H51	
54H00	54H00, 9H00		54H21	54H21, 9H21		54H52	54H52, 9H52	
54L00		9L00	54H22	54H22, 9H22		5453	5453, 9N53	9008
54S00	54S00, 9S00		54S22	54S22, 9S22		54H53	54H53, 9H53	
5401	5401, 9N01	9012	5423	5423, 9N23		5454	5454, 9N54	9008
54H01	54H01, 9H01		5425	5425, 9N25		54H54	54H54, 9H54	
5402	5402, 9N02	9015	5426	5426, 9N26		54H55	54H55, 9H55	
5403	5403, 9N03	9012	5427	5427, 9N27		5460	5460, 9N60	9006
54S03	54S03, 9S03		5430	5430, 9N30	9007	54H60	54H60, 9H60	
5404	5404, 9N04	9016	54H30	54H30, 9H30		54H61	54H61, 9H61	
54H04	54H04, 9H04		5432	5432, 9N32		54H62	54H62, 9H62	
54L04		9L04	5437	5437, 9N37		54S64	54S64, 9S64	
54S04	54S04, 9S04	9S04A	5438	5438, 9N38		54S65	54S65, 9S65	
5405	5405, 9N05	9017	5439	5439, 9N39		5470	5470, 9N70	9001
54H05	54H05, 9H05		5440	5440, 9N40	9009	54H71	54H71, 9H71	
54S05	54S05, 9S05	9S05A	54H40	54H40, 9H40		5472	5472, 9N72	9000
5406	5406, 9N06		54S40	54S40, 9S40		54H72	54H72, 9H72	
5407	5407, 9N07		5441	9315		5473	5473, 9N73	9020
5408	5408, 9N08		5442	5442, 9352	9301	54H73	54H73, 9H73	
54H08	54H08, 9H08		54L42		93L01	5474	5474, 9N74	9024
5409	5409, 9N09		5443	5443, 9353	9311	54H74	54H74, 9H74	9024
5410	5410, 9N10	9003	5444	5444, 9354	9311	54L74		9L24
54H10	54H10, 9H10		5445	5445, 9345		54S74	54S74, 9S74	
5411	5411, 9N11		5446A	5446, 9357A	9317C	5475	5475, 9375	9314
54H11	54H11, 9H11		5447A	5447, 9357B	9317B	5476	5476, 9N76	9022
5412	5412, 9N12		5448	5448, 9358	9307	54H76	54H76, 9H76	
5413	5413, 9N13		5449	5449, 9359	9307	5477	5477, 9377	9314
5416	5416, 9N16		5450	5450, 9N50	9005	54H78	54H78, 9H78	
5417	5417, 9N17		54H50	54H50, 9H50		5480	5480, 9380	9304
5420	5420, 9N20	9004	5451	5451, 9N51	9005	5481	93407	
54H20	54H20, 9H20							

T.I.	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
5482	5482, 9382	9304
5483	5483, 9383	9340
5484		93433
5485		9324
54L85		93L24
5486	5486, 9N86	9014
54L86		9L86
54H87	54H87, 93H87	
5488A	93434	
5489	93403	
5490	5490, 9390	9350
54L90		93L10
5491	5491, 9391	
5492	5492, 9392	9305
5493	5493, 9393	9356
54L93		93L16
5494	5494, 9394	9300
5495A	5495, 9395	9300
54L95		93L00
5496	5496, 9396	
54L99		93L00
54100		9308
54H101	54H101, 9H101	
54H102	54H102, 9H102	
54H103	54H103, 9H103	
54104	9000	
54105	9001	
54H106	54H106, 9H106	
54107	54107, 9N107	
54H108	54H108, 9H108	
54110		9001
54S112	54S112, 9S112	
54S113	54S113, 9S113	
54S114	54S114, 9S114	
54121	54121, 9603	
54122		9601
54123		9602
54S140	54S140, 9S140	
54145	54145, 93145	
54150	54150, 93150	
54151	54151, 93151	9312
54S151		93S12
54152	54152, 93152	9312
54153	54153, 93153	9309
54L153		93L09
54154	9311	
54155		9321
54157	9322	
54160	9310	
54161	9316	
54162		9310
54163		9316
54164	54164, 93164	
54165	54165, 93165	
54166	54166, 93166	
54170		9338
54172		9338
54176	54176, 93176	
54177	54177, 93177	
54178	54178, 93178	
54179	54179, 93179	
54180	54180, 93180	9348
54180	54180, 93180	9348
54181	54181, 9341	
54S181	54S181, 93S41	
54182	54182, 9342	
54S182	54S182, 93S42	
54H183	54H183, 93H183	9304
54184	93434	
54185	93434	
54187	93406	
54190	54190, 93190	
54191	54191, 93191	
54192	54192, 9360	
54193	54193, 9366	
54194		93H72
54195	9300	
54S195	93S00	
54196	54196, 93196	9310
54197	54197, 93197	9316
54198	54198, 93198	
54200		93410
54201		93410
7400	7400, 9N00	9002
74H00	74H00, 9H00	
74L00		9L00
74S00	74S00, 9S00	
7401	7401, 9N01	9012
74H01	74H01, 9H01	
7402	7402, 9N02	9015
7403	7403, 9N03	9012
74S03	74S03, 9S03	
7404	7404, 9N04	9016
74H04	74H04, 9H04	
74L04		9L04
74S04	74S04, 9S04	9S04A
7405	7405, 9N05	9017
74H05	74H05, 9H05	
74S05	74S05, 9S05	9S05A
7406	7406, 9N06	
7407	7407, 9N07	
7408	7408, 9N08	
74H08	74H08, 9H08	
7409	7409, 9N09	
7410	7410, 9N10	9003
74H10	74H10, 9H10	
7411	7411, 9N11	
74H11	74H11, 9H11	
7412	7412, 9N12	
7413	7413, 9N13	
7416	7416, 9N16	
7417	7417, 9N17	
7420	7420, 9N20	9004
74H20	74H20, 9H20	
74S20	74S20, 9S20	
74H21	74H21, 9H21	
74H22	74H22, 9H22	
74S22	74S22, 9S22	
7423	7423, 9N23	
7425	7425, 9N25	
7426	7426, 9N26	
7427	7427, 9N27	
7430	7430, 9N30	9007
74H30	74H30, 9H30	
7432	7432, 9N32	
7437	7437, 9N37	
7438	7438, 9N38	
7439	7439, 9N39	
7440	7440, 9N40	9009
74H40	74H40, 9H40	
74S40	74S40, 9S40	
7441A	9315	
7442	7442, 9352	9301
74L42		93L01
7443	7443, 9353	9311
7444	7444, 9354	9311
7445	7445, 9345	
7446A	7446, 9357A	9317C
7447A	7447, 9357B	9317B
7448	7448, 9358	9307
7449	7449, 9359	9307
7450	7450, 9N50	9005
74H50	74H50, 9H50	
7451	7451, 9N51	9005
74H51	74H51, 9H51	
74H52	74H52, 9H52	
7453	7453, 9N53	9008
74H53	74H53, 9H53	
7454	7454, 9N54	9008
74H54	74H54, 9H54	
74H55	74H55, 9H55	

T.I.	FAIRCHILD PIN FOR PIN REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
7460	7460, 9N60	9006
74H60	74H60, 9H60	
74H61	74H61, 9H61	
74H62	74H62, 9H62	
74S64	74S64, 9S64	
74S65	74S65, 9S65	
7470	7470, 9N70	9001
74H71	74H71, 9H71	
7472	7472, 9N72	9000
74H72	74H72, 9N72	
7473	7473, 9N73	9020
74H73	74H73, 9H73	
7474	7474, 9N74	
74H74	74H74, 9H74	9024
74L74		9L24
74S74	74S74, 9S74	
7475	7475, 9375	9314
7476	7476, 9N76	9022
74H76	74H76, 9H76	
7477	7477, 9377	9314
74H78	74H78, 9H78	
7480	7480, 9380	9304
7481	93407	
7482	7482, 9382	9304
7483	7483, 9383	9340
7484		93433
7485		9324
74L85		93L24
7486	7486, 9N86	9014
74L86		9L86
74H87	74H87, 93H87	
7488A	93434	
7489	93403	
7490	7490, 9390	9350
74L90		93L10
7491	7491, 9391	
7492	7492, 9392	
7493	7493, 9392	9356
74L93		93L16
7494	7494, 9394	9300
7495A	7495, 9395	9300
74L95		93L00
7496	7496, 9396	
74L99		93L00
74100		9308
74H10	74H101, 9H101	
74H10	74H102, 9H102	
74H10	74H103, 9H103	
74104	9000	
74105	9001	
74H106	74H106, 9H106	
74107	74107, 9N107	9020
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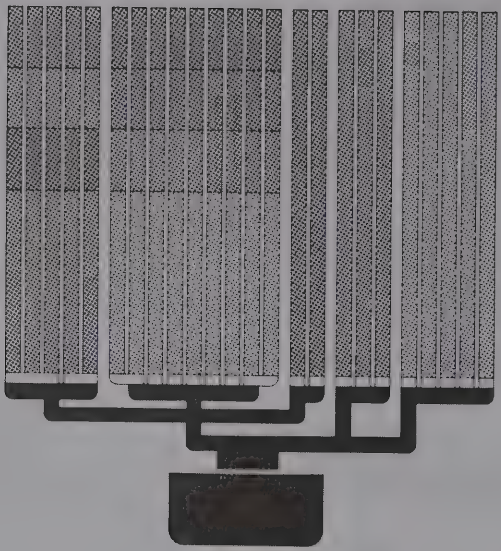
74S109	74S109, 9S109	
74110		9001
74S112	74S112, 9S112	
74S113	74S113, 9S113	
74S114	74S114, 9S114	
74121	74121, 9603	
74122		9601
74123		9602
74S140	74S140, 9S140	
74141	74141, 93141	
74145	74145, 93145	
74150	74150, 93150	
74151	74151, 93151	9312
74S151		93S12
74152	74152, 93152	9312
74153	74153, 93153	9309
74L153		93L09
74154	9311	
74155		9321
74157	9322	
74160	9310	
74161	9316	
74162		9310
74163		9316
74164	74164, 93164	
74165	74165, 93165	
74166	74166, 93166	
74170		9338
74172		9338
74176	74176, 93176	
74177	74177, 93177	
74178	74178, 93178	
74179	74179, 93179	
74180	74180, 93180	9348
74181	74181, 9341	
74S181	74S181, 93S41	
74182	74182, 9342	
74S182	74S182, 93S42	
74H183	74H183, 93H183	9304
74184	93434 (Option)	
74185	93434 (Option)	
74187	93406	
74190	74190, 93190	
74191	74191, 93191	
74192	74192, 9360	
74193	74193, 9366	
74194		93H72
74195	9300	
74S195	93S00	
74196	74196, 93196	9310
74197	74197, 93197	9316
74198	74198, 93198	
74200		93410
74201		93410



Other Fairchild Digital Families And Application Notes

LIST OF OTHER FAIRCHILD DIGITAL PRODUCTS AND APPLICATION NOTES

In addition to TTL, Fairchild also manufactures other digital logic integrated circuit families. Further information on these other products is available on request from:

Fairchild Semiconductor
P.O. BOX 880A
Mountain View, California 94040
Att. Distribution Services

CTL–COMPLEMENTARY TRANSISTOR LOGIC

9952 Series (CTL I)

9030	8-Bit Memory Cell
9952	Dual 2-Input NOR Gate
9953	AND/OR Gate
9954	AND/OR Gate
9955	AND/OR Gate
9956	Dual 2-Input Buffer
9957	Flip-Flop
9964	AND/OR Gate
9965	AND/OR Gate
9966	AND/OR Gate
9967	Flip-Flop
9968	Dual High Speed Latch
9971	AND/OR Gate
9972	AND/OR Gate

9852 Series (CTL II)

9801	Dual Gated Phase Splitter NOR/OR
9806	Hex Inverter NOR/OR
9816	Hex Restorer (Buffer) AND/OR Gate
9820	100 Ω Line Receiver
9821	100 Ω Line Driver
9822	Dual Full Adder/Subtractor
9823	Carry Lookahead Logic for 9822
9824	4-Bit Comparator
9828	Dual JK-D Flip-Flop
9834	Quad Latch (with output gating)
9838	1-of-8 Decoder
9852	Dual 2-Input Inverter NOR/OR
9853	2-2-3-Input AND/OR Gate
9854	Dual 4-Input AND/OR Gate
9855	Single 8-Input AND/OR Gate
9856	Dual 2-Input Restorer (Buffer) AND/OR Gate
9863	9874 (minus 2 kΩ resistors) AND/OR Gate
9864	3-1-3-Input AND/OR Gate
9865	Quad 1-Input AND/OR Gate
9866	Quad 2-Input (one pair or tied) AND/OR Gate
9871	Quad 2-Input (pairs or tied) AND/OR Gate
9872	9866 (minus 2 K Input resistors) AND/OR Gate
9874	3-2-2-2-Input AND/OR Gate
9875	4-3-3-Input AND/OR Gate
9877	Micro Operator
9881	8-Input Multiplexer
9883	8-Input Priority Encoder

DTL–DIODE TRANSISTOR LOGIC

9930 Series

9930	Dual 4-Input Extendable NAND Gate
9932	Quad 2-Input Extendable NAND Buffer Gate
9933	Extender
9935	Extendable Hex Inverter
9936	Hex Inverter
9937	Hex Inverter
9941	Monostable Multivibrator
9944	Quad 2-Input Extendable NAND Buffer Gate (Open Collector)
9945	RS Flip-Flop
9946	Quad 2-Input NAND Gate
9948	RS Flip-Flop
9949	Quad 2-Input NAND Gate
9950	ac Coupled RS Flip-Flop
9951	Monostable Multivibrator
9961	Dual 4-Input Extendable NAND Gate
9962	Triple 3-Input NAND Gate
9963	Triple 3-Input NAND Gate
9135	Hex Inverter (Open Collector)
9157	Quad 2-Input Buffered NAND Gate
9158	Quad 2-Input Power NAND Gate
9093	Dual JK Flip-Flop
9094	Dual JK Flip-Flop
9097	Dual JK Flip-Flop
9099	Dual JK Flip-Flop
9109	High Voltage Hex Inverter
9110	High Voltage Hex Inverter
9111	RS Flip-Flop
9112	High Voltage Hex Inverter

1800 Series

1800	Dual 5-Input NAND Gate
1801	Dual 5-Input NAND Gate
1802	Single 8-Input NAND Gate
1803	Single 8-Input NAND Gate
1804	Single 10-Input NAND Gate
1805	Single 10-Input NAND Gate
1806	Quad 2-Input AND Gate
1807	Quad 2-Input AND Gate
1808	Quad 2-Input OR Gate
1809	Quad 2-Input OR Gate
1810	Quad 2-Input NOR Gate
1811	Quad 2-Input NOR Gate
1812	Quad 2-Input Exclusive OR Gate
1813	Quad Latch
1814	Quad Latch

ECL – EMITTER COUPLED LOGIC

9500 Series

95H00	4-Bit Universal Register
9502	Dual 4-Input OR/NOR Gate (2.4 ns)
95H02	High Speed 9502 (1.6 ns)
9503	Triple 2-Input OR/NOR Gate (2.4 ns)
95H03	High Speed 9503 (1.6 ns)
9504	Quad 2-Input NOR Gate (2.4 ns)
95H04	High Speed 9504 (1.6 ns)
9505	Quad OR/AND Gate
9507	Quad AND/NAND Gate
95H10	Synchronous Decade Counter
95H16	Synchronous Binary Counter
95H22	High Input Z 95H02
95L22	Low Power 9502 (20 mW, 2 ns)
95H23	High Input Z 95H03
95L23	Low Power 9503 (20 mW, 2 ns)
95H24	High Input Z 95H04
95L24	Low Power 9504 (20 mW, 2 ns)
9528	160 MHz "Dual D" Flip-Flop
95H28	220 MHz 9528
95H29	210 MHz JK Flip-Flop
9534	Quad Latch
9538	2 Line/8 Line Decoder
*95H39	8-Bit Multiport Memory
95H41	4-Bit ALU
*95H42	Lookahead Unit for 95H41
95H55	5-Bit Comparator
9578	Quad Exclusive-OR Gate/4-Bit Comparator
9579	Quad 2-Input Multiplexer
9580	Triple 2-Input Multiplexer
9581	8-Input Multiplexer
9582	Multifunction Receiver/Schmitt Trigger
95H84	2-Bit Adder/Subtractor
95H90	250 MHz Prescaler (divide by 10/11)
9595	ECL – TTL Converter
95400	64-Bit RAM – 16X4
95401	16-Bit RAM – 16X1
95410	256-Bit RAM – 256X1

95100 Series

*95101	Dual 2-Wide OR-AND/NAND Gate
95102	Dual OR/NOR Gate
95103	Triple OR/NOR Gate
95104	Quad OR/NOR Gate
*95105	4-Wide OR-AND/NAND Gate
*95106	Dual 3-Input, 3-Output OR Gate
*95108	Quad 1-Input OR/NOR Gate
*95109	Dual 3-Input, 3-Output NOR Gate
95110	Synchronous Decade Counter
95116	Synchronous Hexadecimal Counter
95128	Dual D Flip-Flop
95129	JK Flip-Flop
*95134	Quad Latch
*95138	1-of-8 Decoder
95141	4-Bit ALU/Function Generator
*95178	Quad Exclusive OR
*95179	Quad 2-Input Multiplexer
*95180	Triple 2-Input Multiplexer
*95196	Quad ECL–TTL Level Converter
*95197	Quad TTL–ECL Level Converter

RTL – RESISTOR TRANSISTOR LOGIC

9900 Series

9900	Buffer
9901	Counter Adapter
9902	Flip-Flop
9903	3-Input NOR Gate
9904	Half Adder
9905	Half Shift Register
9906	Half Shift Register
9907	4-Input Gate
9908	Adder
9909	Buffer
9910	Dual Gate
9911	Dual Gate W/Inverter
9912	Half Adder
9913	Type D F/F
9914	Dual 2-Input NOR Gate
9915	Dual 3-Input NOR Gate
9921	Expander
9923	JK Flip-Flop
9926	JK Flip-Flop
9927	Quad Inverter
9974	JK Flip-Flop

CμL (RTL) – COUNTING MICROLOGIC

9958	Decade Counter
9959	4-Bit Latch
9960	Decoder/Driver
9989	Binary Counter

TTL APPLICATIONS NOTE INDEX

The following Applications notes provide further information on many of the devices described in this catalog. New Application notes are prepared often. Check Fairchild Application Index, published quarterly, for the most up to date listing.

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305	9348 12-Input Parity Checker/Generator

*To be announced.

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